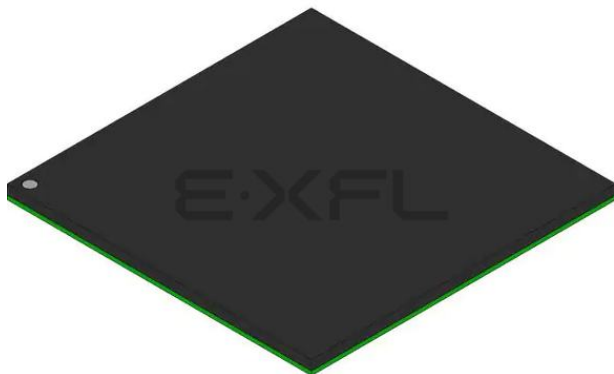




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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc852tcvr80a

12 Bus Signal Timing

The maximum bus speed that the MPC852T supports is 66 MHz. [Table 7](#) shows the frequency ranges for standard part frequencies.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core	40	50	40	66.67
Bus	40	50	40	66.67

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core	40	50	40	66.67	40	80	40	100
Bus 2:1	20	25	20	33.33	20	40	20	50

[Table 9](#) provides the bus operation timing for the MPC852T at 33, 40, 50, and 66 MHz.

The timing for the MPC852T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT) See Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	−2	+2	−2	+2	−2	+2	−2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK ¹	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns

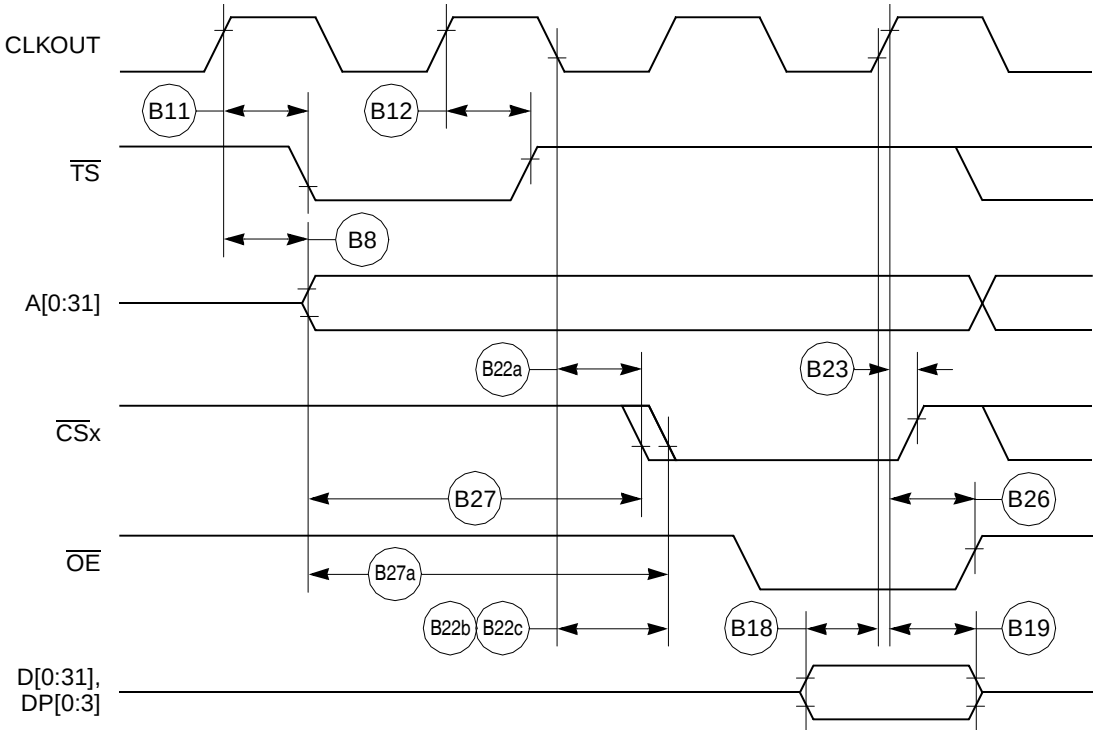


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Figure 18 provides the timing for the external bus that the UPM controls.

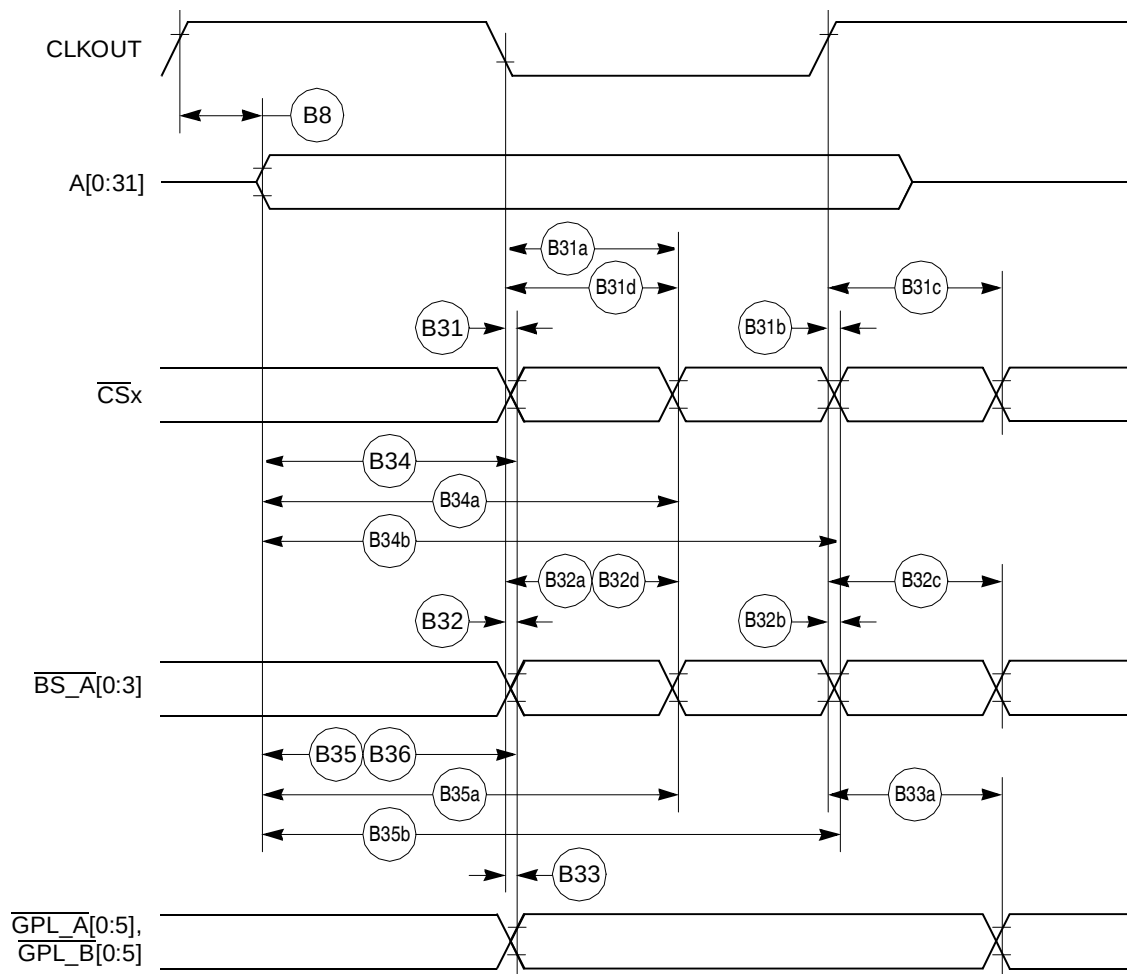


Figure 18. External Bus Timing (UPM Controlled Signals)

Figure 26 provides the PCMCIA access cycle timing for the external bus read.

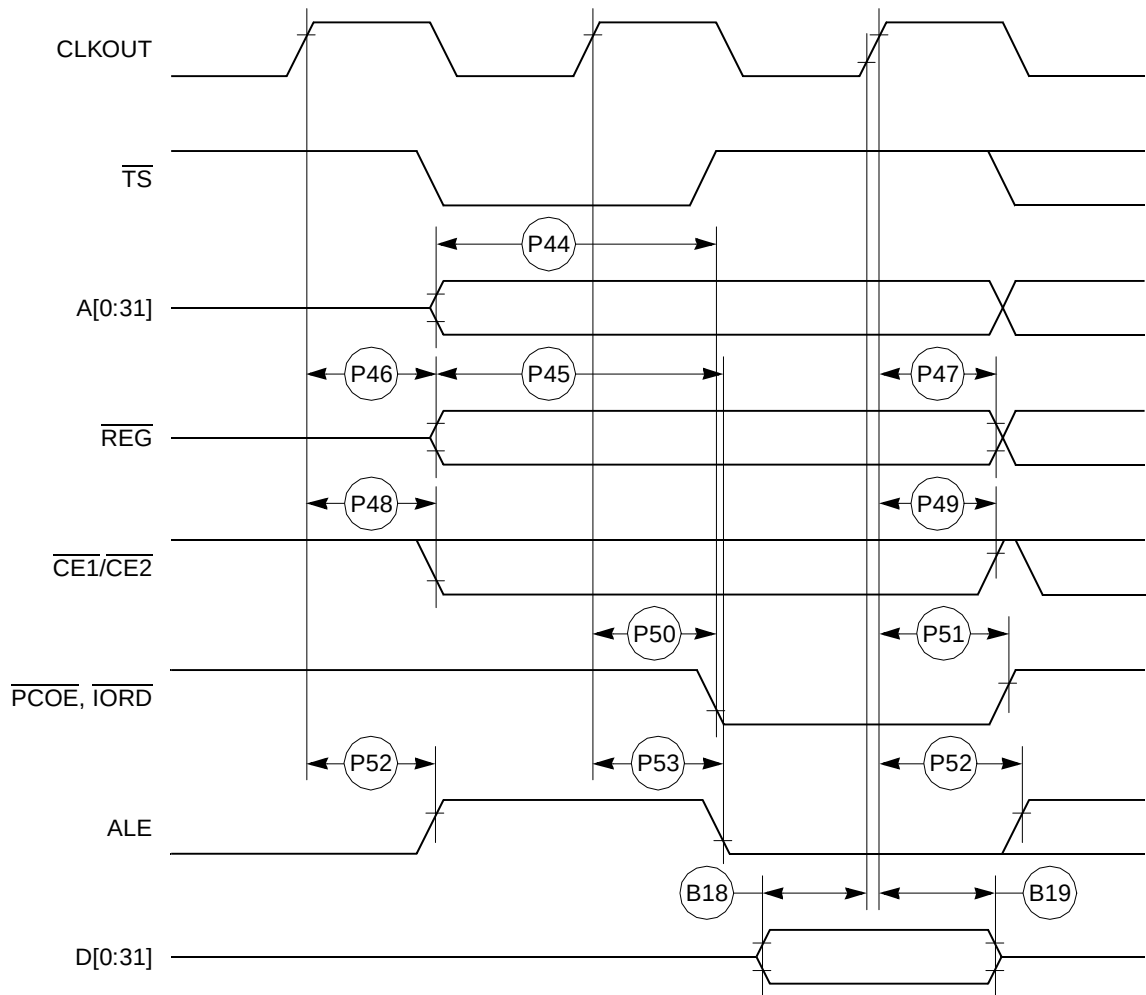


Figure 26. PCMCIA Access Cycles Timing External Bus Read

Table 14 shows the reset timing for the MPC852T.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J82	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J83	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J84	$\overline{\text{RSTCONF}}$ pulse width (MIN = $17.00 \times B1$)	515.20	—	425.00	—	340.00	—	257.60	—	ns
J85	—	—	—	—	—	—	—	—	—	—
J86	Configuration data to HRESET rising edge set up time (MIN = $15.00 \times B1 + 50.00$)	504.50	—	425.00	—	350.00	—	277.30	—	ns
J87	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = $0.00 \times B1 + 350.00$)	350.00	—	350.00	—	350.00	—	350.00	—	ns
J88	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J89	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J90	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J91	$\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J92	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J93	DSDI, DSCK set up (MIN = $3.00 \times B1$)	90.90	—	75.00	—	60.00	—	45.50	—	ns
J94	DSDI, DSCK hold time (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J95	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = $8.00 \times B1$)	242.40	—	200.00	—	160.00	—	121.20	—	ns

Figure 35 provides the reset timing for the debug port configuration.

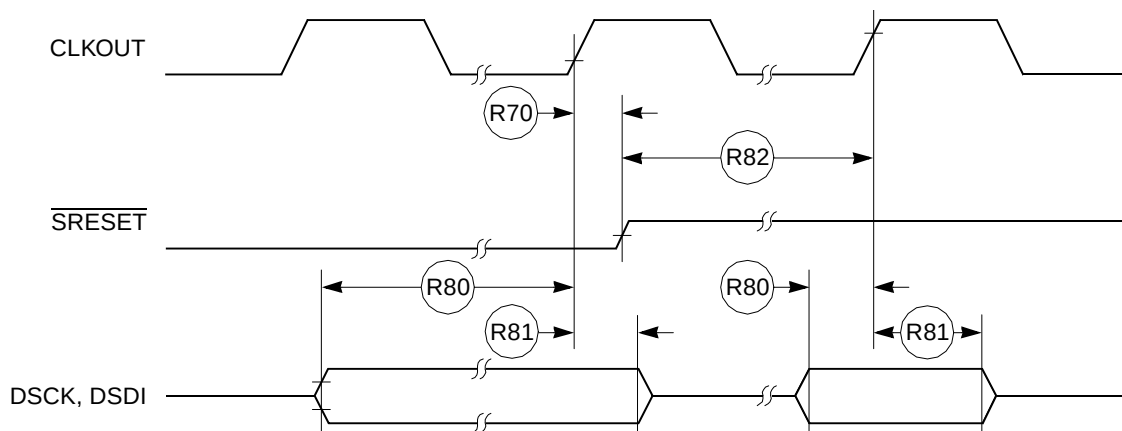


Figure 35. Reset Timing—Debug Port Configuration

13 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC852T shown in Figure 36 through Figure 39.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

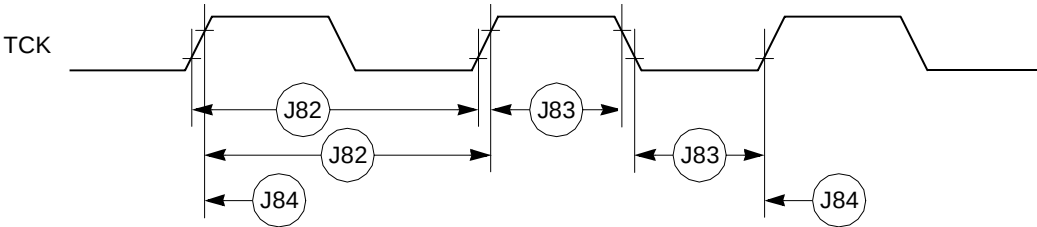


Figure 36. JTAG Test Clock Input Timing

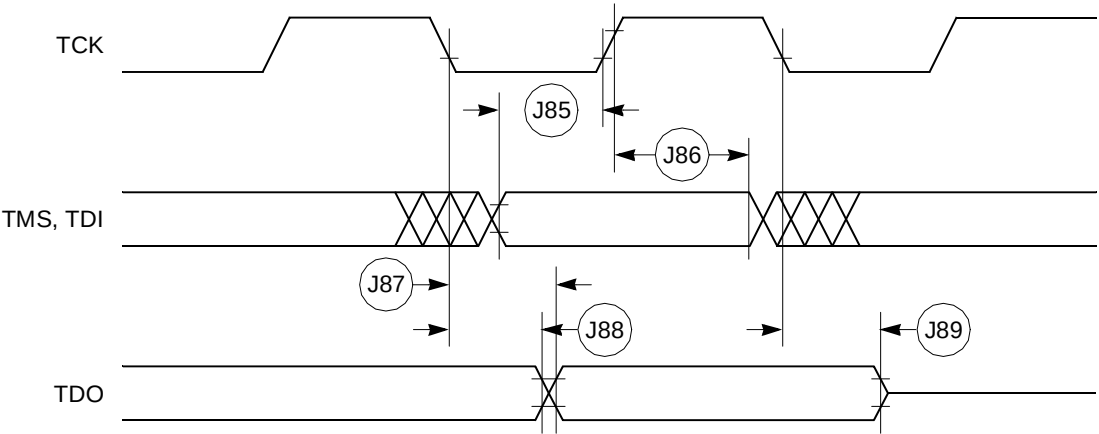


Figure 37. JTAG Test Access Port Timing Diagram

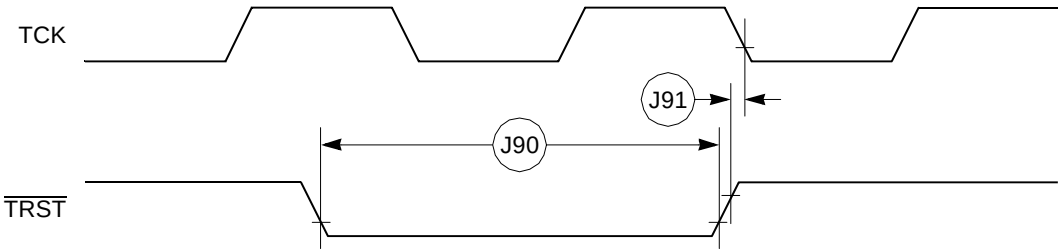


Figure 38. JTAG $\overline{\text{TRST}}$ Timing Diagram

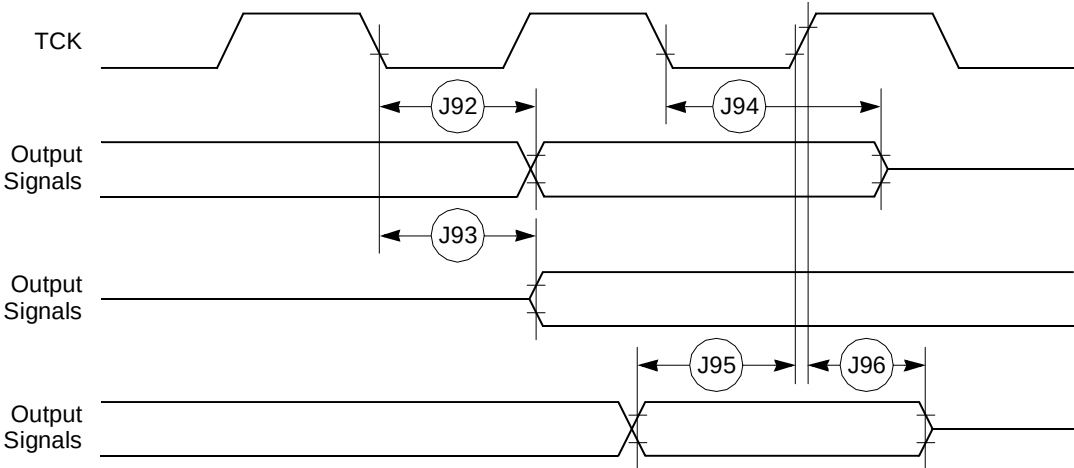


Figure 39. Boundary Scan (JTAG) Timing Diagram

14.2 IDMA Controller AC Electrical Specifications

Table 17 provides the IDMA controller timings as shown in Figure 41 through Figure 44.

Table 17. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high ¹	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

¹ Applies to high-to-low mode (EDM = 1).

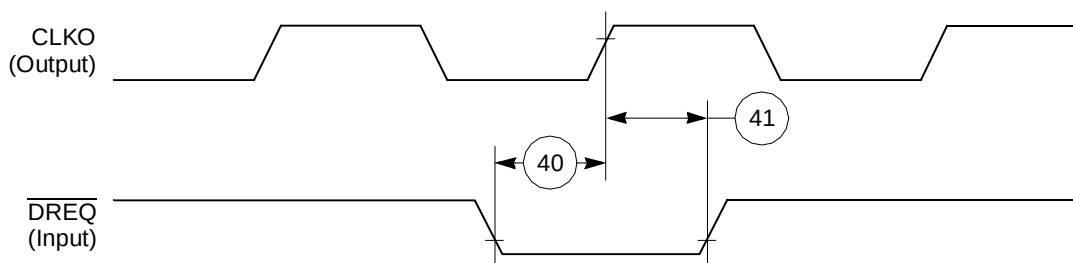


Figure 41. IDMA External Requests Timing Diagram

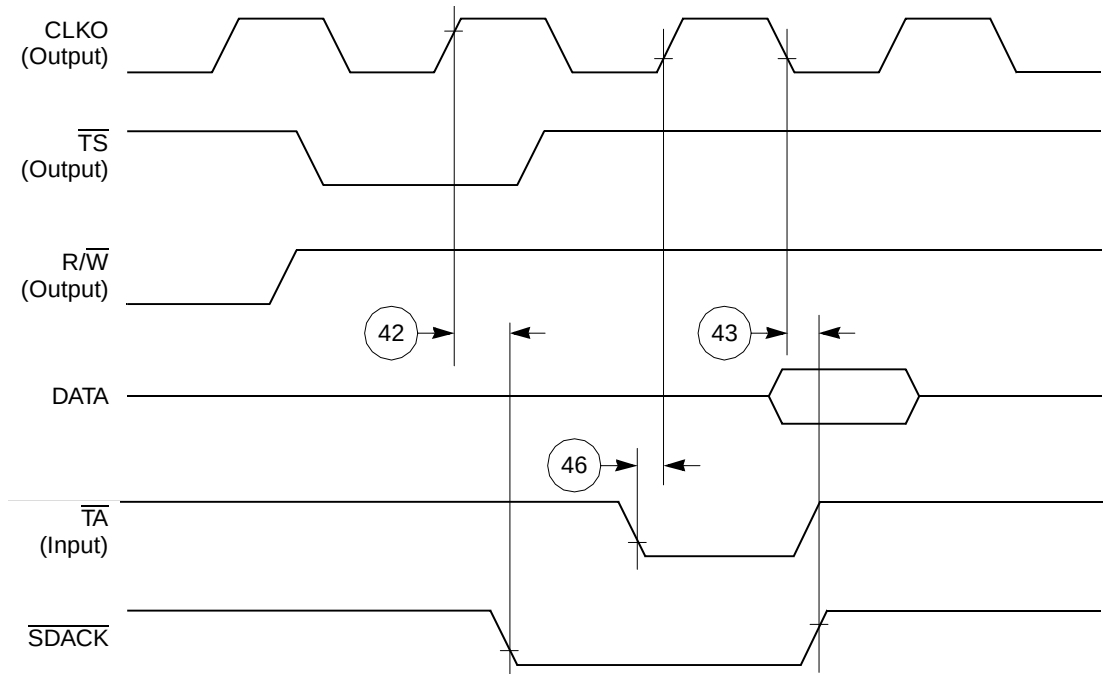


Figure 42. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

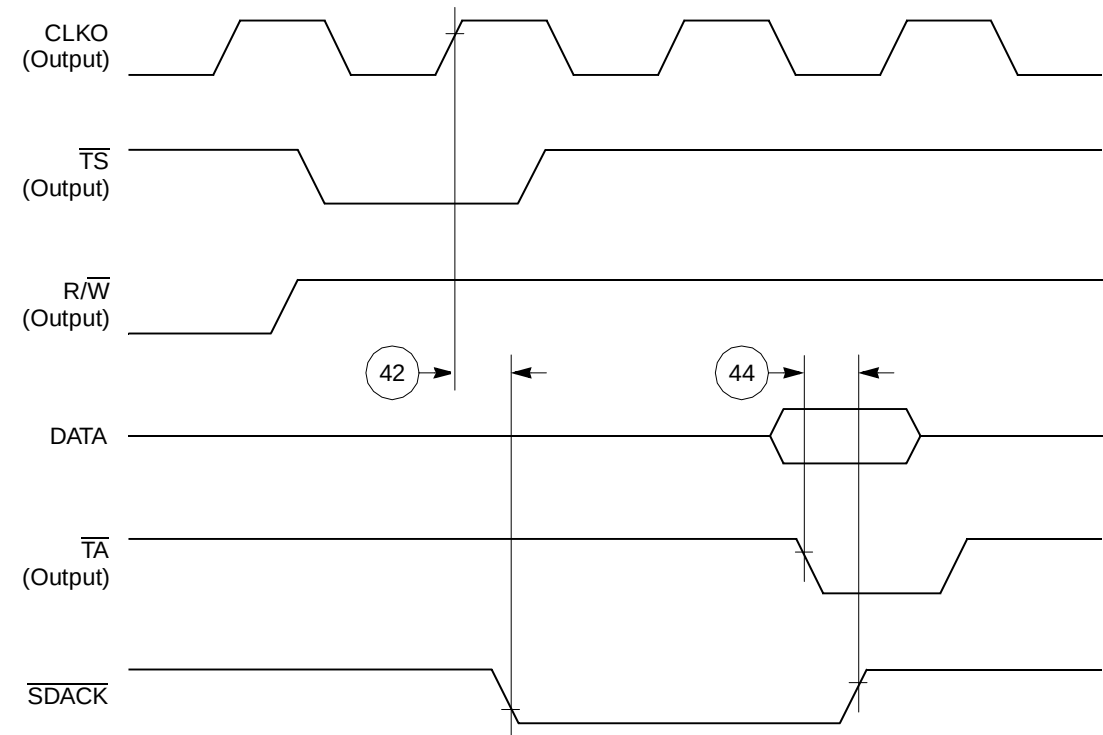


Figure 43. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Internally-Generated $\overline{\text{TA}}$

Table 20. NMSI External Clock Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
107	RXD3 hold time from RCLK3 rising edge ²	5.00	—	ns
108	$\overline{\text{CD3}}$ setup Time to RCLK3 rising edge	5.00	—	ns

¹ The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge ²	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

¹ The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

14.7 SPI Master AC Electrical Specifications

Table 23 provides the SPI master timings as shown in Figure 55 and Figure 56.

Table 23. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t _{cyc}
161	MASTER clock (SCK) high or low time	2	512	t _{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

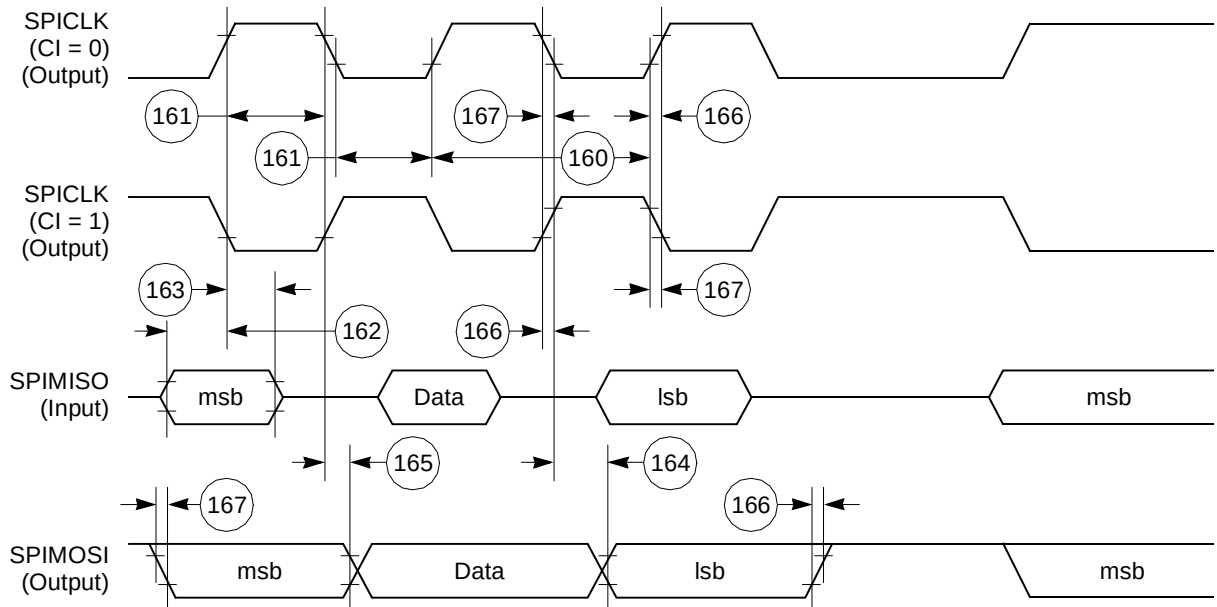


Figure 55. SPI Master (CP = 0) Timing Diagram

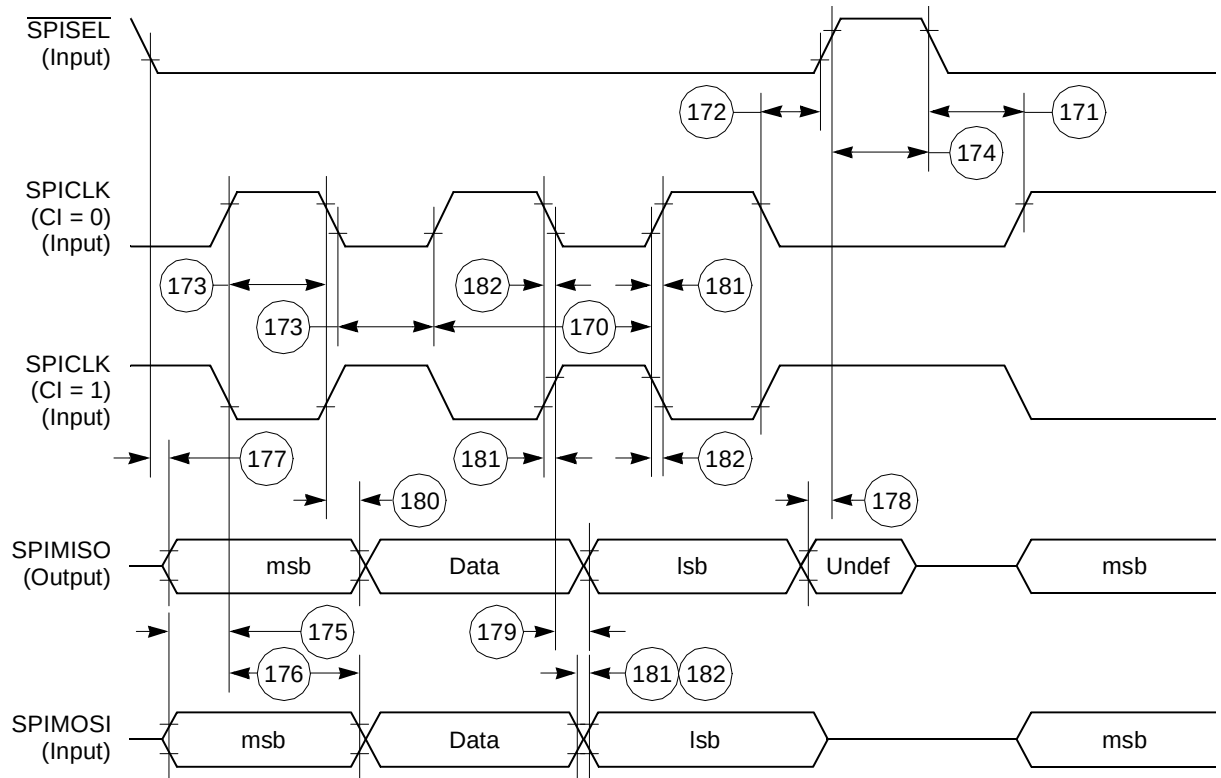


Figure 57. SPI Slave (CP = 0) Timing Diagram

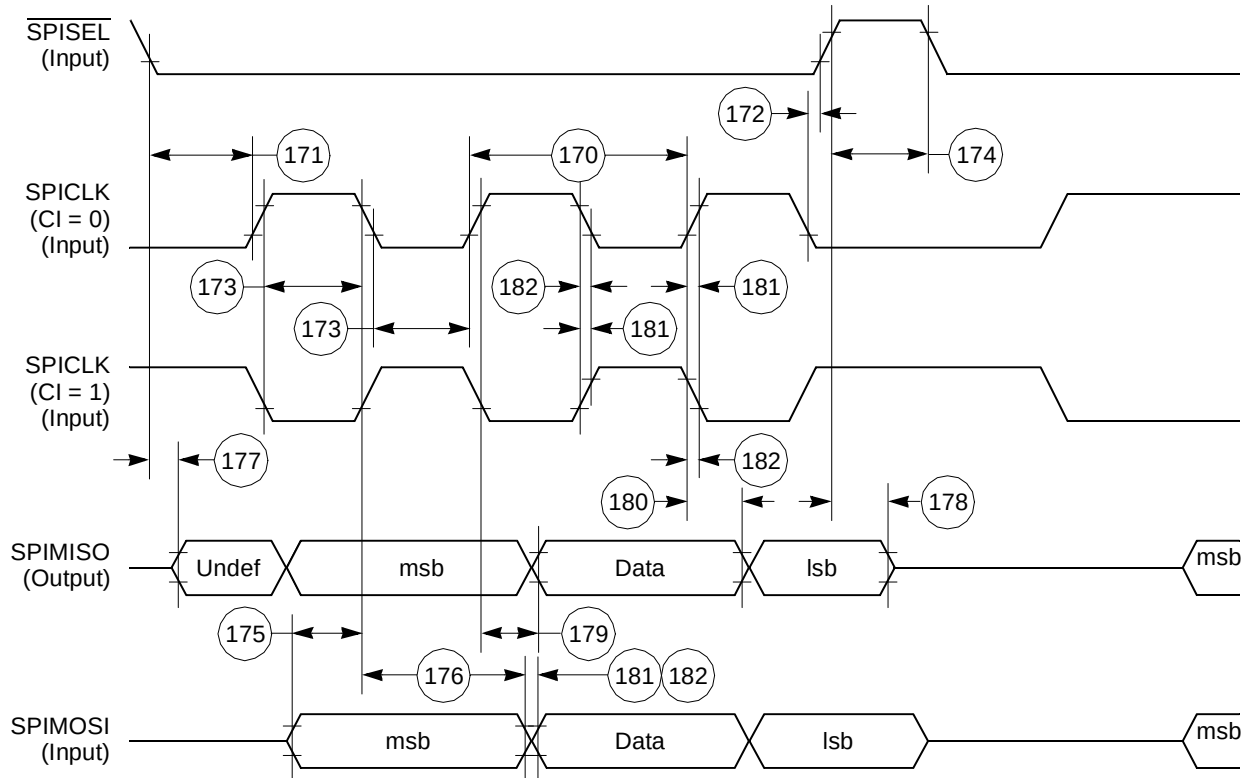


Figure 58. SPI Slave (CP = 1) Timing Diagram

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
FRZ $\overline{\text{IRQ6}}$	H4	Bidirectional (3.3 V only)
$\overline{\text{IRQ0}}$	P13	Input (3.3 V only)
$\overline{\text{IRQ1}}$	M11	Input (3.3 V only)
$\overline{\text{M_TX_CLK}}$ $\overline{\text{IRQ7}}$	N12	Input (3.3 V only)
$\overline{\text{CS}}[0:5]$	B2, A2, D3, C3, E6, C4	Output
$\overline{\text{CS6}}$	D4	Output
$\overline{\text{CS7}}$	A3	Output
$\overline{\text{WE0}}$ BS_B0 $\overline{\text{IORD}}$	D6	Output
$\overline{\text{WE1}}$ BS_B1 $\overline{\text{IOWR}}$	C6	Output
$\overline{\text{WE2}}$ BS_B2 $\overline{\text{PCOE}}$	A5	Output
$\overline{\text{WE3}}$ BS_B3 $\overline{\text{PCWE}}$	B5	Output
$\overline{\text{BS_A}}[0:3]$	A6, D7, C7, B7	Output
$\overline{\text{GPL_A0}}$ $\overline{\text{GPL_B0}}$	C5	Output
$\overline{\text{OE}}$ $\overline{\text{GPL_A1}}$ $\overline{\text{GPL_B1}}$	D5	Output
$\overline{\text{GPL_A}}[2:3]$ $\overline{\text{GPL_B}}[2:3]$ $\overline{\text{CS}}[2-3]$	A4, B4	Output
UPWAITA $\overline{\text{GPL_A4}}$	C2	Bidirectional (3.3 V only)
$\overline{\text{GPL_A5}}$	E4	Output
$\overline{\text{PORESET}}$	P1	Input (3.3 V only)
$\overline{\text{RSTCONF}}$	K4	Input (3.3 V only)
$\overline{\text{HRESET}}$	J4	Open-drain
$\overline{\text{SRESET}}$	M3	Open-drain
XTAL	N1	Analog Output

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PA3, CLK5, BRGO3, TIN3	K16	Bidirectional (5-V tolerant)
PA2, CLK6, $\overline{\text{TOUT3}}$	K14	Bidirectional (5-V tolerant)
PA1, CLK7, BRGO4, TIN4	L15	Bidirectional (5-V tolerant)
PA0, CLK8, $\overline{\text{TOUT4}}$	M16	Bidirectional (5-V tolerant)
PB31, $\overline{\text{SPISEL}}$	E13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	F13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	D15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	G13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	H16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	L16	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	C16	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	E14	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	E15	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	J14	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	K15	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	J13	Bidirectional (5-V tolerant)

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PC4, $\overline{\text{CD4}}$	L14	Bidirectional (5-V tolerant)
PD15, MII_RXD3	M14	Bidirectional (5-V tolerant)
PD14, MII_RXD2	N16	Bidirectional (5-V tolerant)
PD13, MII_RXD1	K13	Bidirectional (5-V tolerant)
PD12, MII_MDC	N15	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	P16	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	R15	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	N14	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	M13	Bidirectional (5-V tolerant)
PD7, $\overline{\text{RTS3}}$, MII_RX_ER	T15	Bidirectional (5-V tolerant)
PD6, $\overline{\text{RTS4}}$, MII_RX_DV	N13	Bidirectional (5-V tolerant)
PD5, MII_TXD3	R14	Bidirectional (5-V tolerant)
PD4, MII_TXD2	P14	Bidirectional (5-V tolerant)
PD3, MII_TXD1	M12	Bidirectional (5-V tolerant)
TMS	F15	Input (5-V tolerant)
TDI, DSDI	G14	Input (5-V tolerant)
TCK, DSCK	H13	Input (5-V tolerant)
$\overline{\text{TRST}}$	F16	Input (5-V tolerant)
TDO, DSDO	F14	Output (5-V tolerant)
MIICRS	B6	Input

Table 30. Pin Assignments—JEDEC Standard (continued)

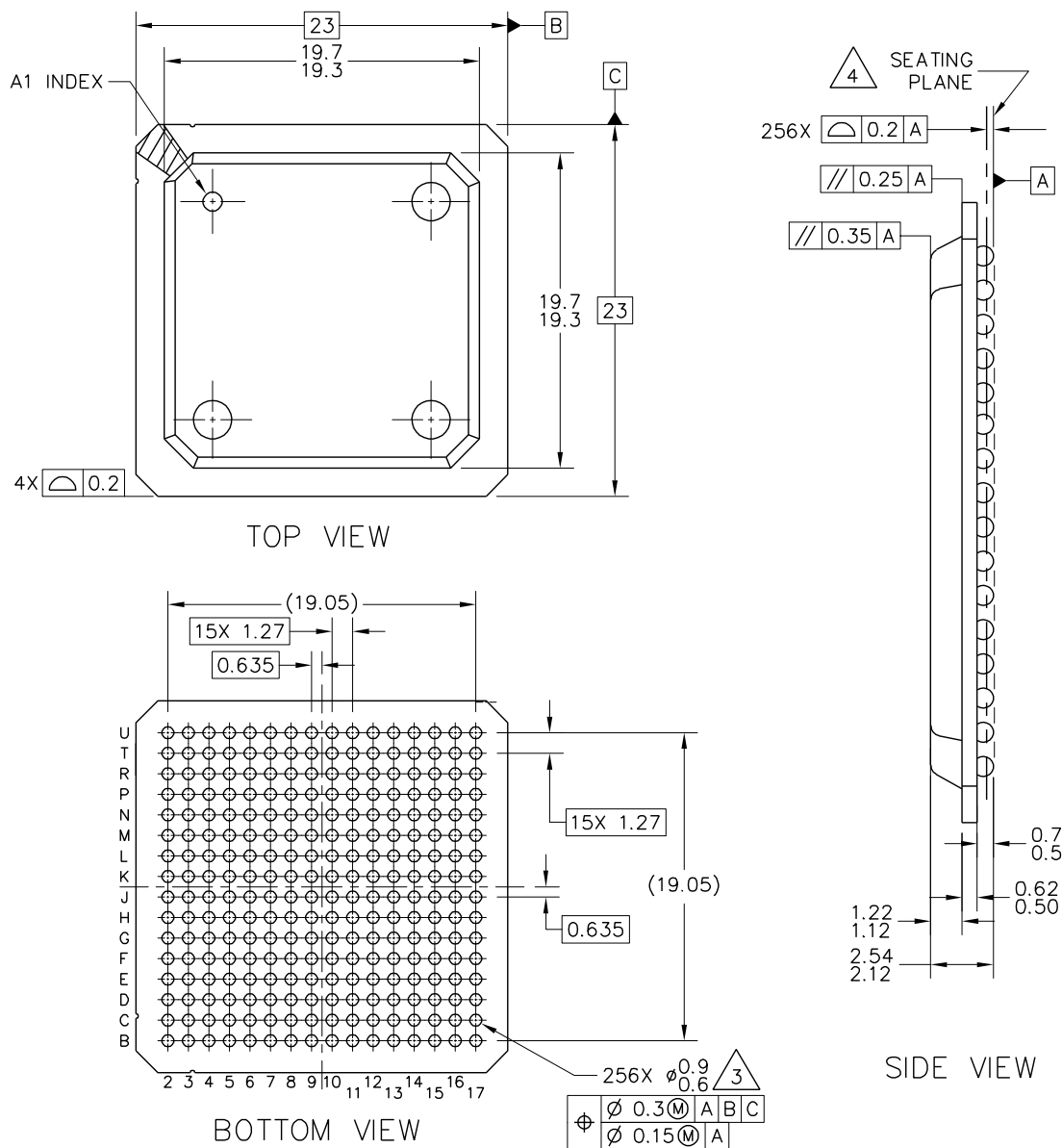
Name	Pin Number	Type
MII_MDIO	G16	Bidirectional (5-V tolerant)
MII_TXEN	T14	Output (5-V tolerant)
MII_COL	F2	Input
V _{SSSYN}	N4	PLL analog GND
V _{SSSYN1}	P3	PLL analog GND
V _{DDSYN}	P2	PLL analog V _{DD}
GND	G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11	Power
V _{DDL}	A7, C1, D16, G15, L4, M2, R1, M15, T8	Power
V _{DDH}	F5, F6, F7, F8, F9, F10, F11, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L8, L9, L10, L11, L12	Power
N/C	A1, A16, B16, C15, D14, E12, L13, M4, P15, R16, T1, T16	No connect

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PB31, $\overline{\text{SPISEL}}$	F14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	G14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	E16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO , BRGO4	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	J15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	J17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	M17	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	D17	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	F15	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	F16	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	K15	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	L16	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	K14	Bidirectional (5-V tolerant)
PC4, $\overline{\text{CD4}}$	M15	Bidirectional (5-V tolerant)
PD15, MII_RXD3	N15	Bidirectional (5-V tolerant)
PD14, MII_RXD2	P17	Bidirectional (5-V tolerant)
PD13, MII_RXD1	L14	Bidirectional (5-V tolerant)

16.2 Mechanical Dimensions of the PBGA Package

For more information on the printed-circuit board layout of the PBGA package, including thermal via design and suggested pad layout, refer to Plastic Ball Grid Array Application Note (order number: AN1231) that is available from your local Freescale sales office. Figure 65 shows the mechanical dimensions of the PBGA package.



Notes:

1. All dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M—1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.

Note: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC852TVRXXX.

Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC852TZXXXX.

Figure 65. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

17 Document Revision History

Table 32 lists significant changes between revisions of this document.

Table 32. Document Revision History

Revision	Date	Changes
4		- Updated template. - On page 1, updated first paragraph and added a second paragraph. - After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 2) and renumbered the rest of the figures. - In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. - In Figure 4, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. - In Table 17, changed num 46 description to read, "TA assertion to rising edge ..." - In Figure 42, changed TA to reflect the rising edge of the clock.
3.1	1/18/2005	Document template update.
3.0	11/2004	- Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values - Added a footnote to Spec 41 specifying that EDM = 1 - Broke the Section 16.1, "Pin Assignments," into 2 smaller sections for the JEDEC and non-JEDEC pinouts.
2.0	12/2003	Put 852T on the 1st page in place of 8245. Figure 62 on page 59 had overbars added on signals CR (pin G2) and WAIT_A (pin P4).
1.8	7/2003	Changed the pinout to be JEDEC Compliant, changed timing parameters B28a through B28d, and B29d to show that TRLX can be 0 or 1.
1.7	5/2003	Changed the SPI Master Timing Specs. 162 and 164
1.6	4/2003	Changed the package drawing in Figure 15-63
1.5	4/2003	Changed 5 Port C pins with interrupt capability to 7 Port C pins. Added the Note: solder sphere composition for MPC852TVR and MPC852TCVR devices is 95.5%Sn 45%Ag 0.5%Cu to Figure 15-63
1.4	2/2003	Changed Table 15-30 Pin Assignments for the PLL Pins V _{SSSYN1} , V _{SSSYN} , V _{DDSYN}
1.3	1/2003	Added subscripts to timing diagrams for B1-B35, to specify memory controller settings for the specific edges.
1.2	1/2003	In Table 15-30, specified EXTCLK as 3.3 V.
1.1	12/2002	Added fast Ethernet controller to the features
1	11/2002	Added values for 80 and 100 MHz
0	10/2002	Initial release

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