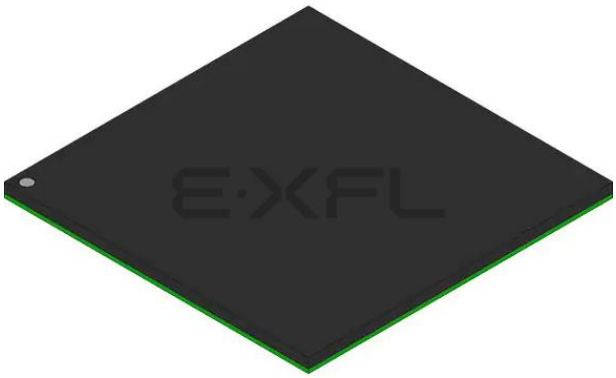

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Product Status	Active
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Graphics Acceleration	-
Display & Interface Controllers	-
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SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc852tczt50a

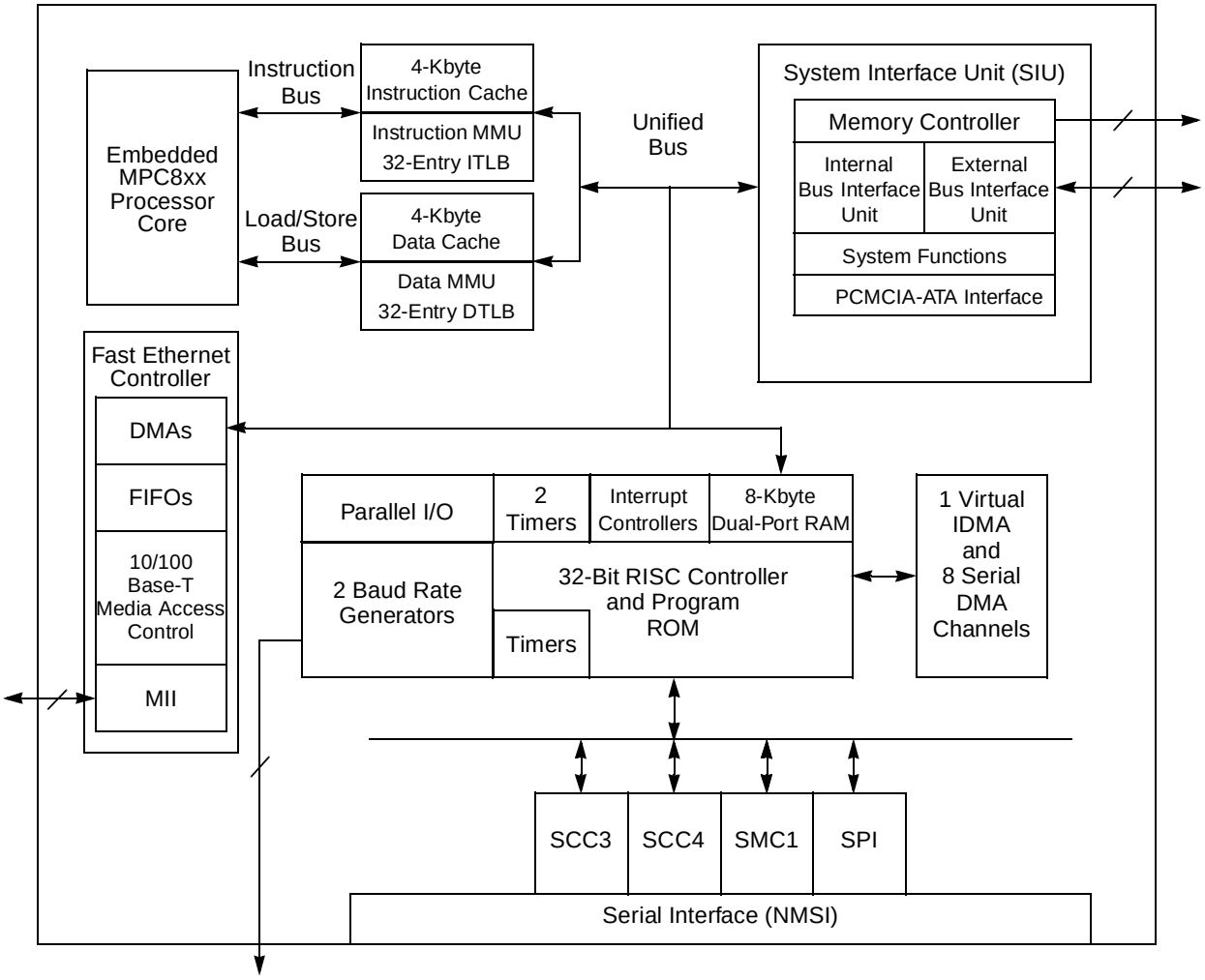

Figure 1. MPC852T Block Diagram

9 Power Supply and Power Sequencing

This section provides design considerations for the MPC852T power supply. The MPC852T has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}) that operates at a lower voltage than the I/O voltage V_{DDH}. The I/O section of the MPC852T is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15] PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO are 5-V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins can not exceed 5.5 V, and the remaining input pins cannot exceed 3.465 V. This restriction applies to power-on reset or power down and normal operation.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power-on reset or power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 3 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power-on reset, and the 1N5820 diodes regulate the maximum potential difference on power-down.

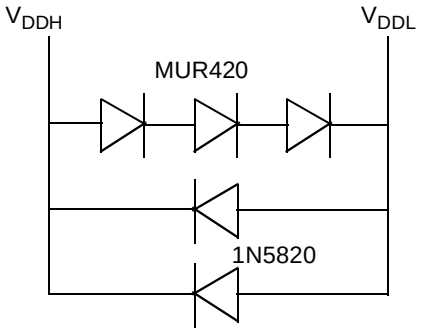

Figure 3. Example Voltage Sequencing Circuit

10 Mandatory Reset Configurations

The MPC852T requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion, the HRCW[DBGC] value that is needed to be set to binary X1 in the hardware reset configuration word (HRCW) and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset.

If hardware reset configuration word (HRCW) is disabled, by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - As Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B37	UPWAIT valid to CLKOUT falling edge[10] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[10] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[11] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the maximum allowed jitter on EXTAL can be up to 2%.

2 For part speeds above 50MHz, use 9.80ns for B11a.

3 The timing required for $\overline{BR}$ input is relevant when the MPC852T is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC852T is selected to work with external bus arbiter.

4 For part speeds above 50MHz, use 2ns for B17.

5 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

6 For part speeds above 50MHz, use 2ns for B19.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 This formula applies to bus operation up to 50 MHz.

9 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

10 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 19.

11 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 22.

Figure 6 provides the timing for the synchronous output signals.

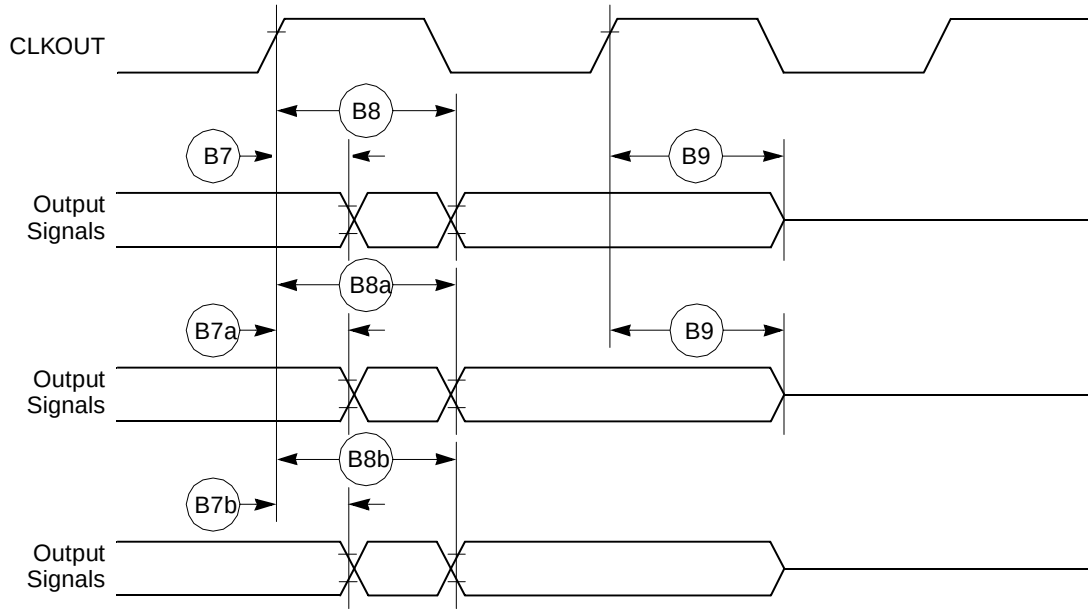

Figure 6. Synchronous Output Signals Timing

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

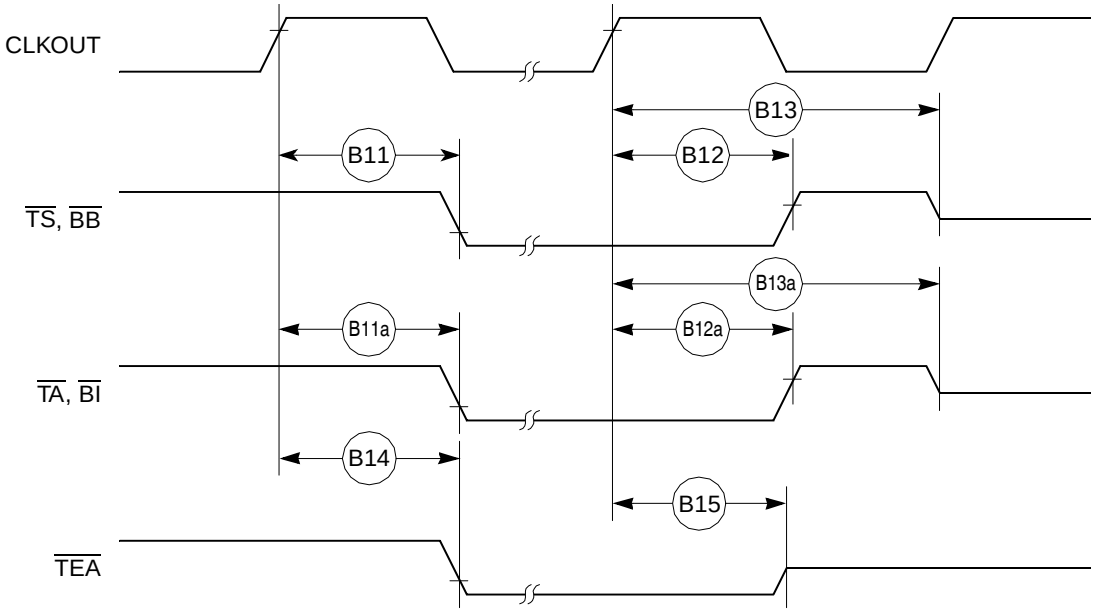

Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

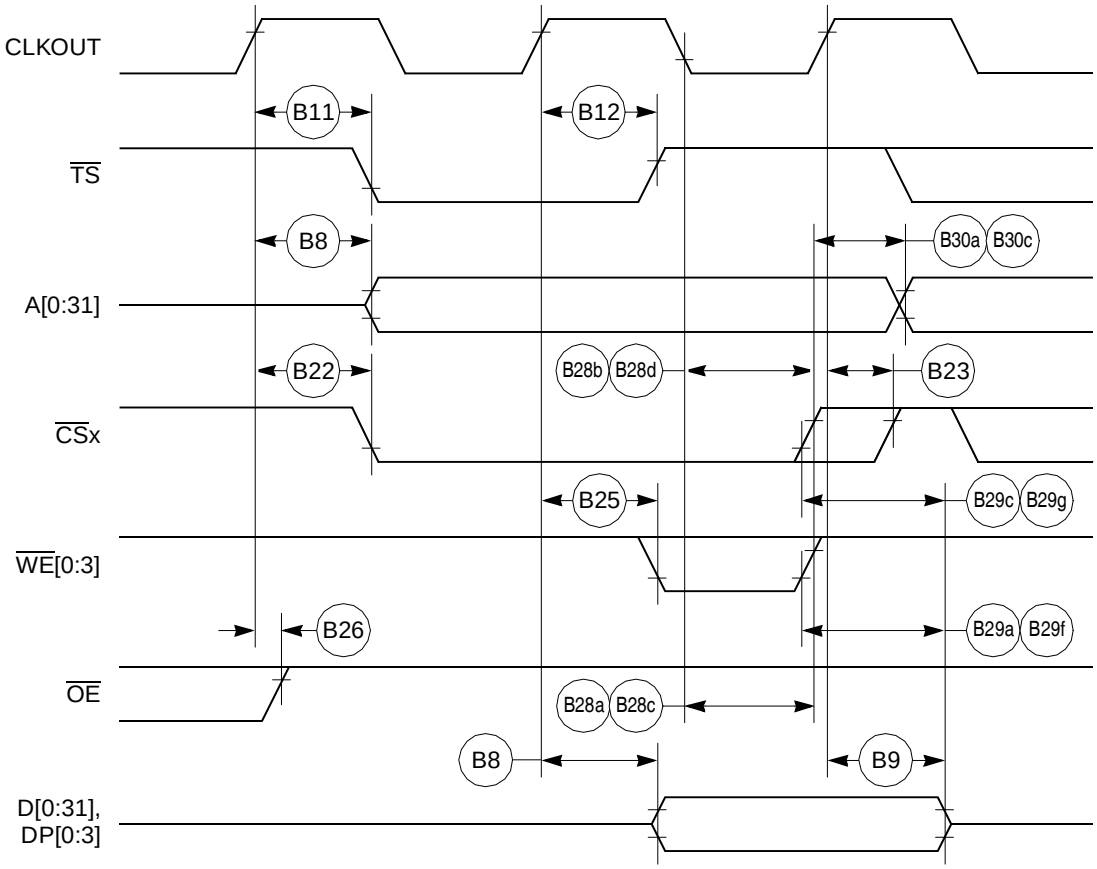

Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Table 10 provides interrupt timing for the MPC852T.

Table 10. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (set up time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

1 The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and need not be asserted or negated with reference to the CLKOUT. The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and have no direct relation with the total system interrupt latency that the MPC852T is able to support.

Figure 24 provides the interrupt detection timing for the external level-sensitive lines.

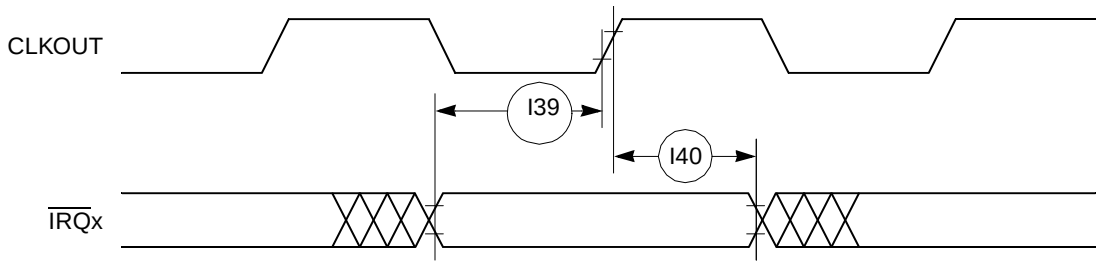

Figure 24. Interrupt Detection Timing for External Level Sensitive Lines

Figure 25 provides the interrupt detection timing for the external edge-sensitive lines.

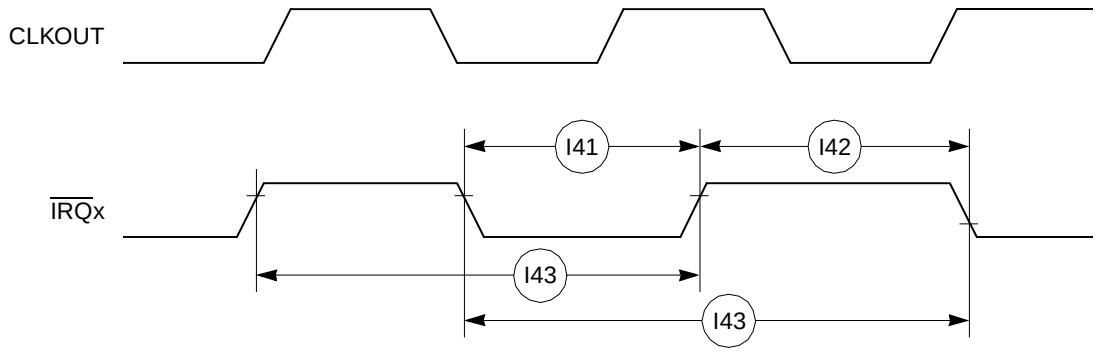

Figure 25. Interrupt Detection Timing for External Edge Sensitive Lines

Table 12 shows the PCMCIA port timing for the MPC852T.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J95	CLKOUT to OPx Valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
J96	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	18.00	—	14.40	—	ns
J97	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
J98	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 29 provides the PCMCIA output port timing for the MPC852T.

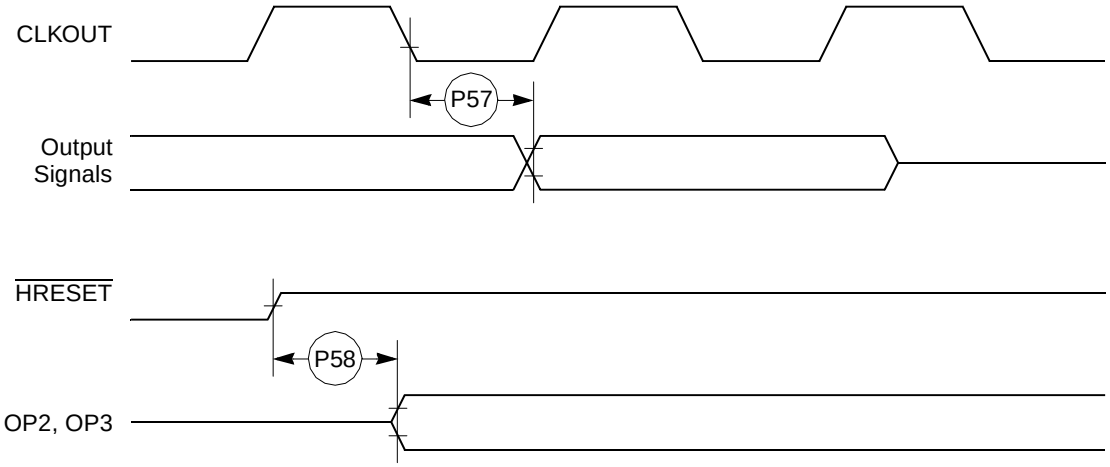

Figure 29. PCMCIA Output Port Timing

Figure 30 provides the PCMCIA output port timing for the MPC852T.

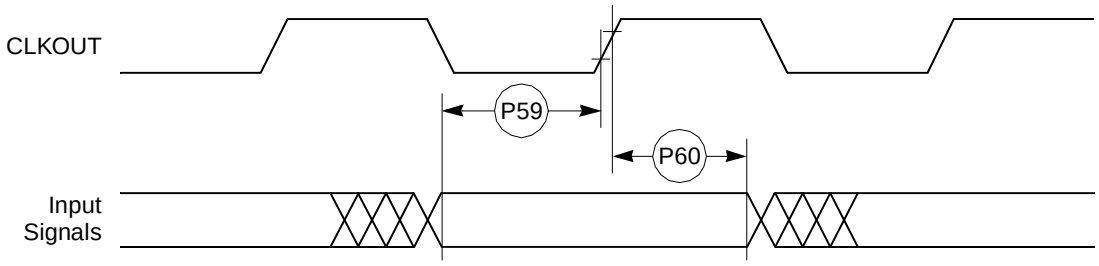

Figure 30. PCMCIA Input Port Timing

Figure 35 provides the reset timing for the debug port configuration.

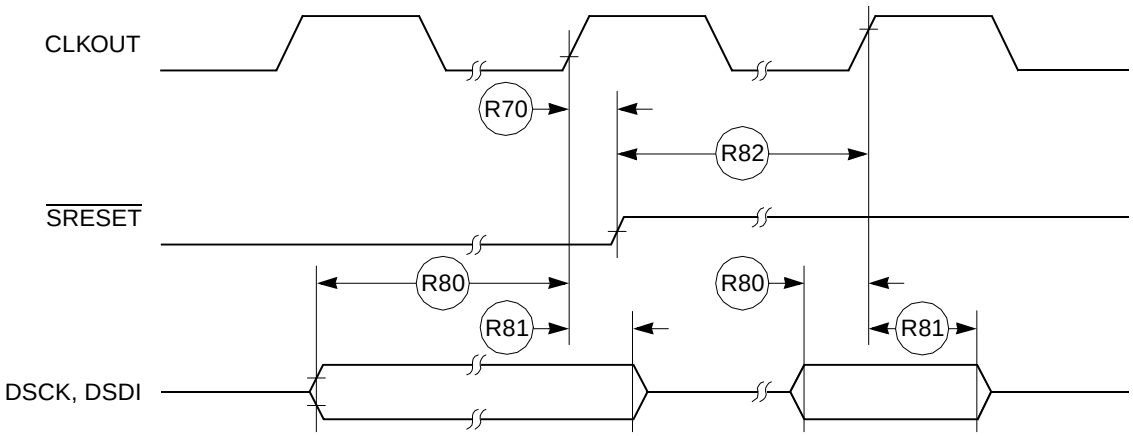

Figure 35. Reset Timing—Debug Port Configuration

13 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC852T shown in Figure 36 through Figure 39.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

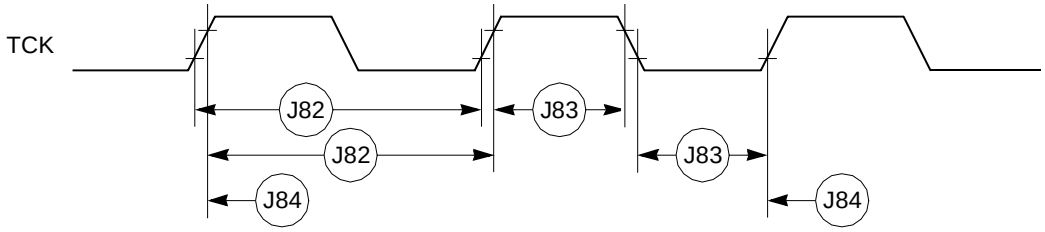

Figure 36. JTAG Test Clock Input Timing

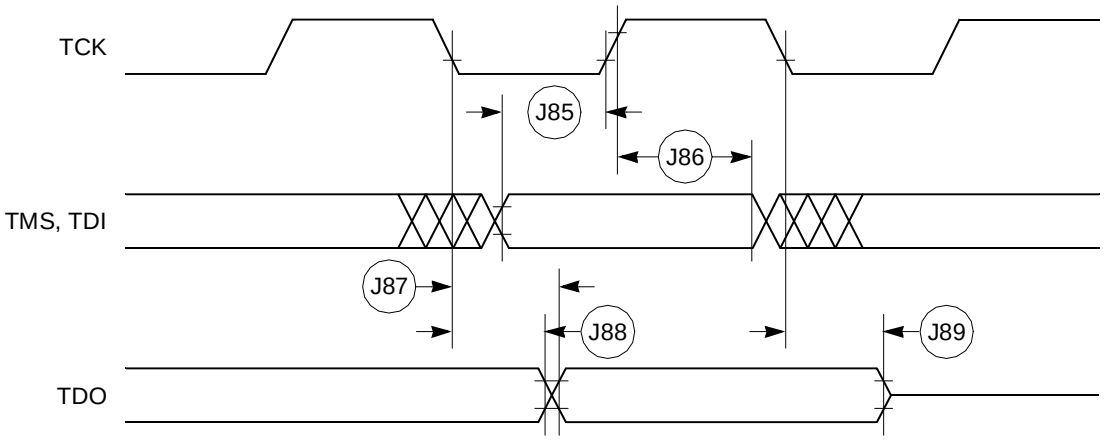

Figure 37. JTAG Test Access Port Timing Diagram

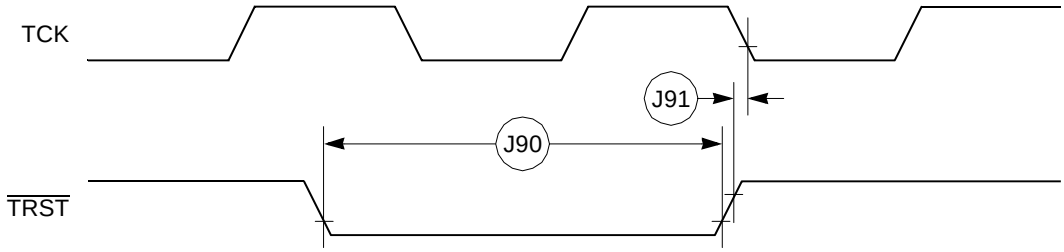

Figure 38. JTAG $\overline{\text{TRST}}$ Timing Diagram

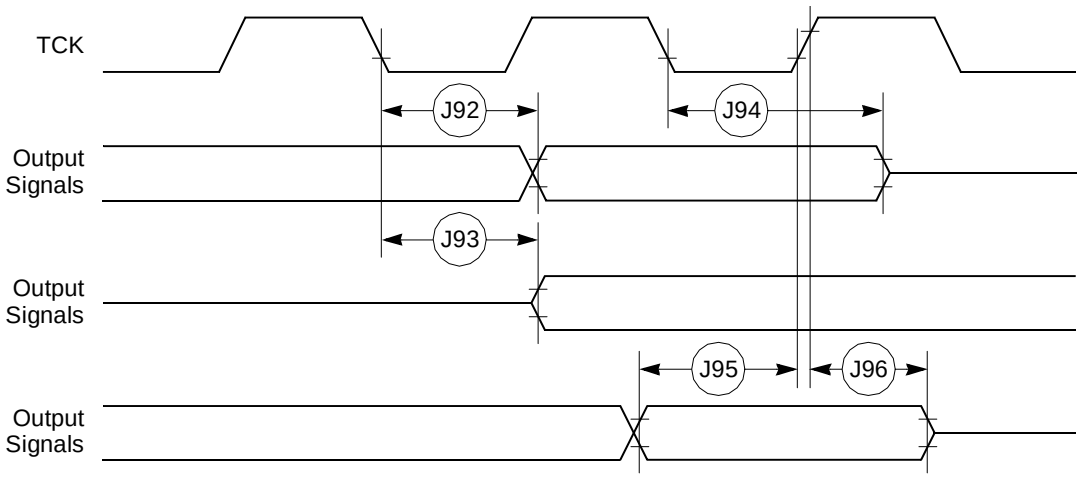

Figure 39. Boundary Scan (JTAG) Timing Diagram

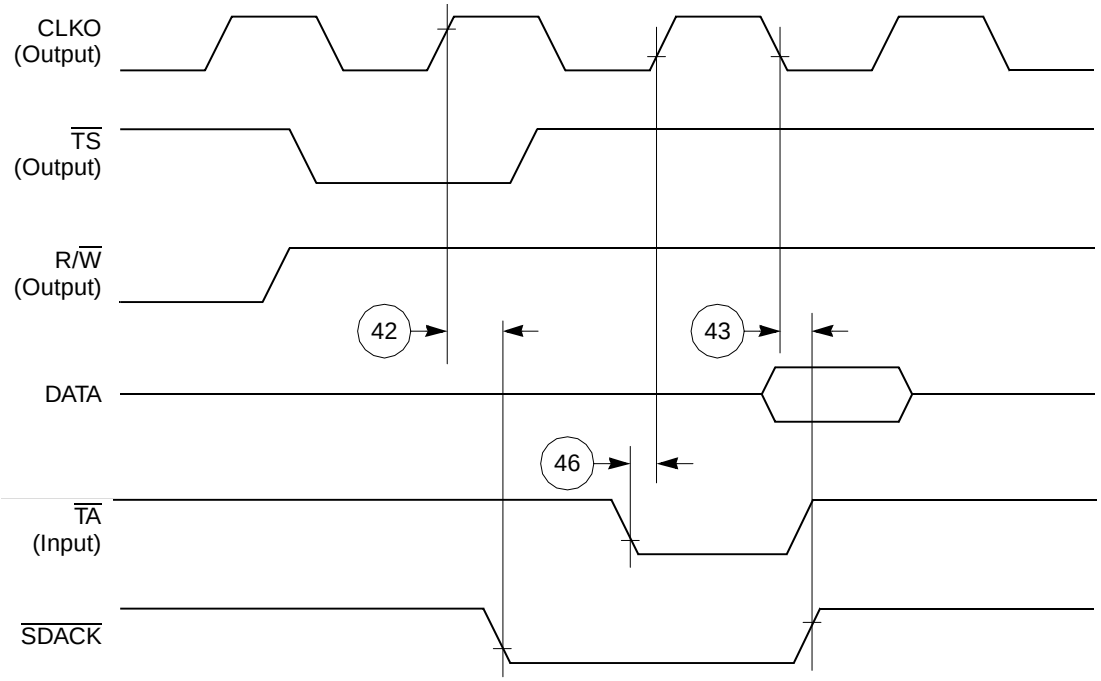

Figure 42. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

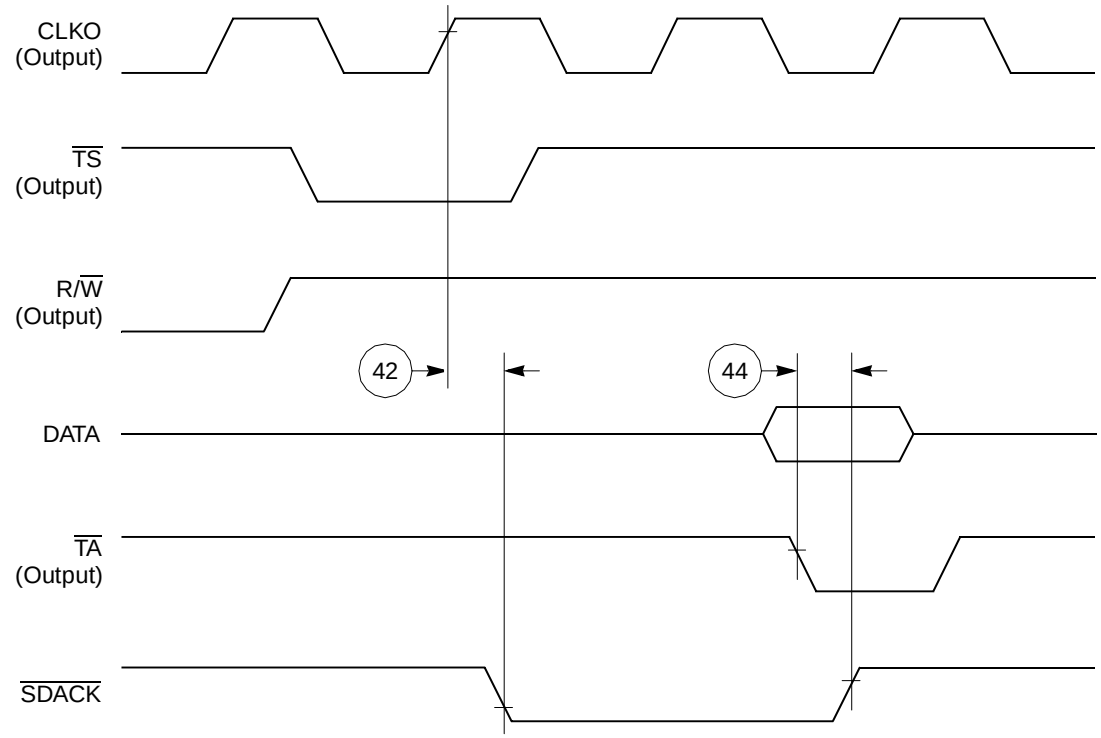

Figure 43. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

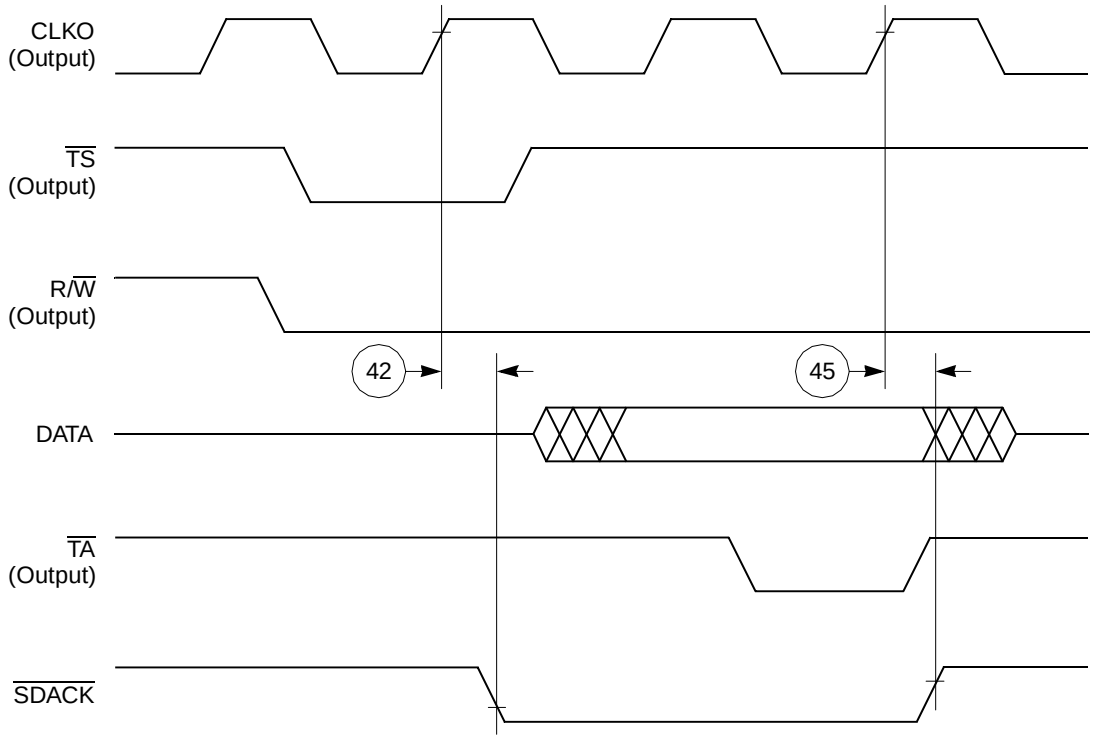

Figure 44. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

14.3 Baud Rate Generator AC Electrical Specifications

Table 18 provides the baud rate generator timings as shown in Figure 45.

Table 18. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

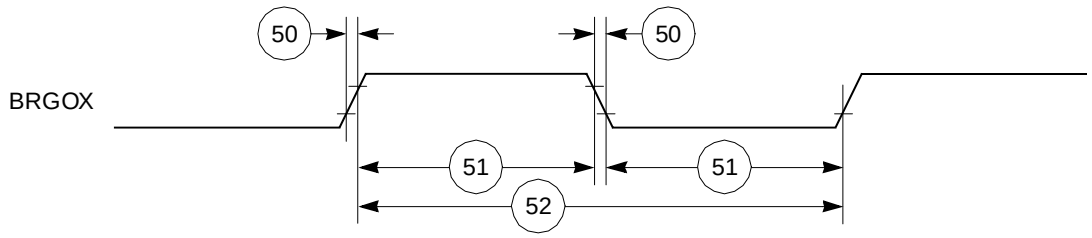

Figure 45. Baud Rate Generator Timing Diagram

14.4 Timer AC Electrical Specifications

Table 19 provides the general-purpose timer timings as shown in Figure 46.

Table 19. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

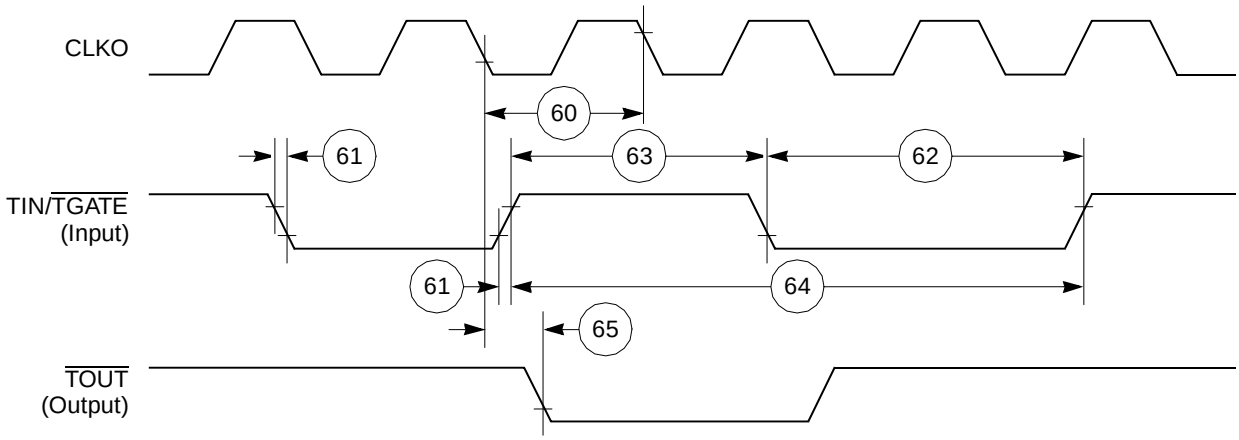

Figure 46. CPM General-Purpose Timers Timing Diagram

14.5 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high[1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK + 5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 28 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 28. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 62 shows the MII serial management channel timing diagram.

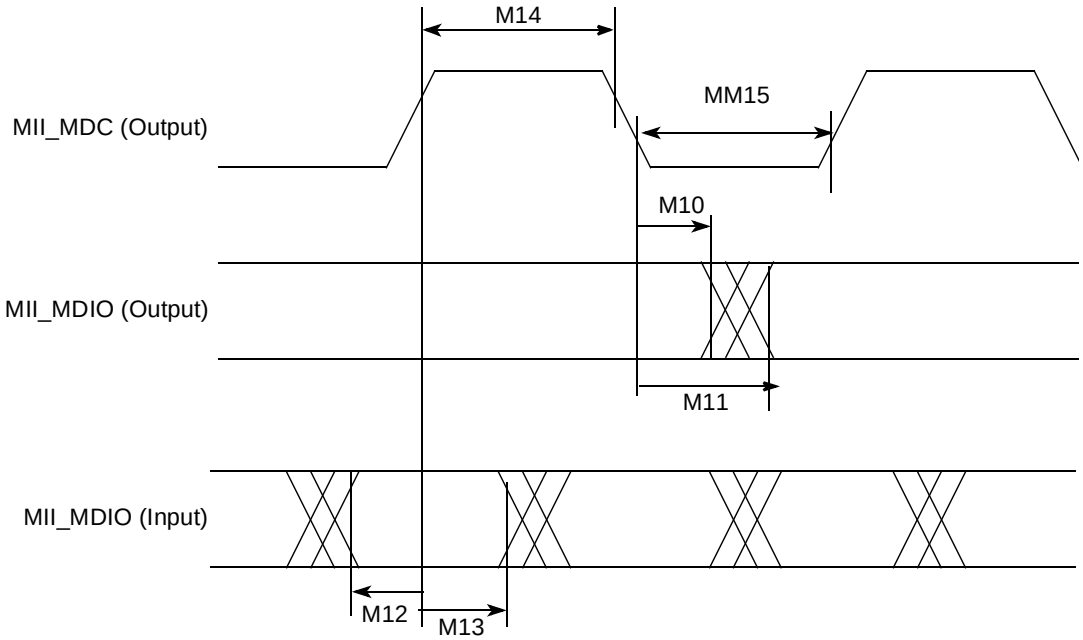

Figure 62. MII Serial Management Channel Timing Diagram

16.1.1 JEDEC Compliant Pinout

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC™ Family Reference Manual*.

NOTE: This is the top view of the device.

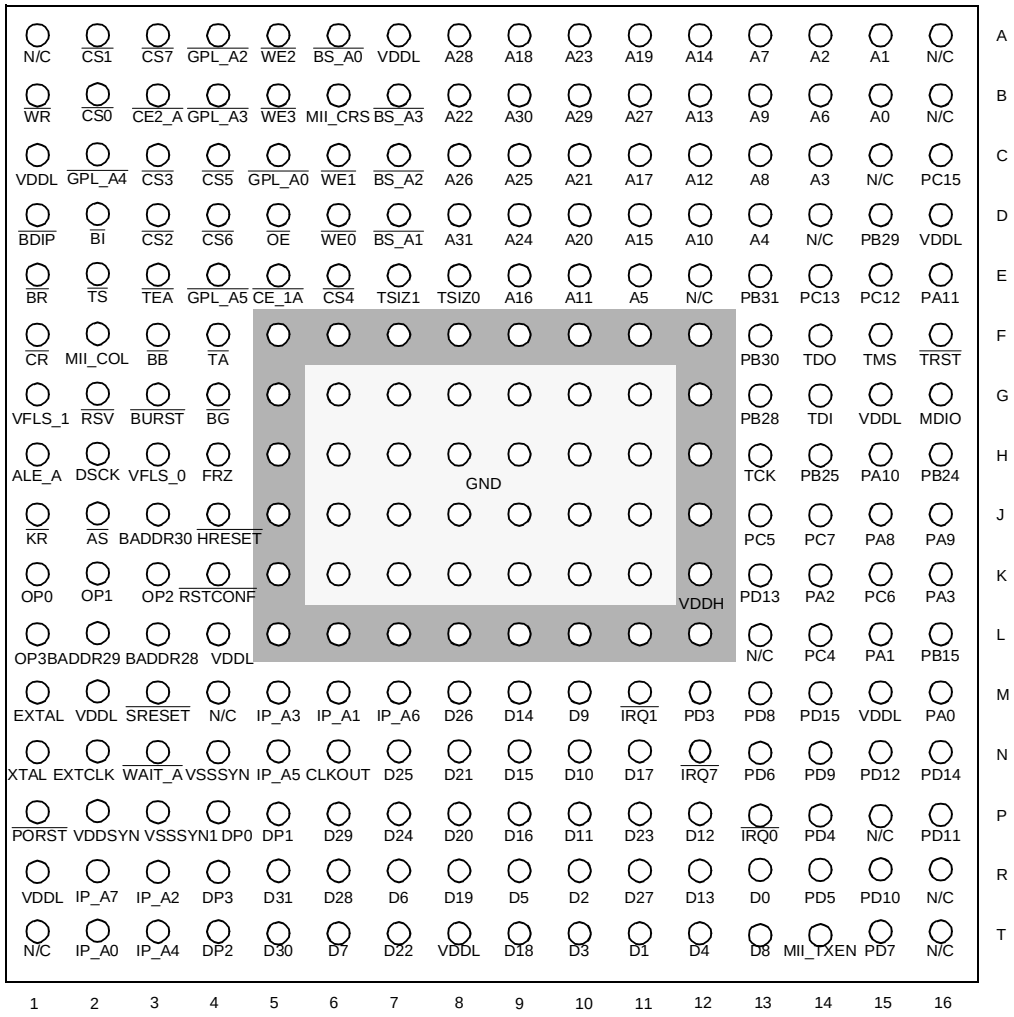

Figure 63. Pinout of PBGA Package—JEDEC Standard

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
FRZ IRQ6	H4	Bidirectional (3.3 V only)
IRQ0	P13	Input (3.3 V only)
IRQ1	M11	Input (3.3 V only)
M_TX_CLK IRQ7	N12	Input (3.3 V only)
CS[0:5]	B2, A2, D3, C3, E6, C4	Output
CS6	D4	Output
CS7	A3	Output
WE0 BS_B0 IORD	D6	Output
WE1 BS_B1 IOWR	C6	Output
WE2 BS_B2 PCOE	A5	Output
WE3 BS_B3 PCWE	B5	Output
BS_A[0:3]	A6, D7, C7, B7	Output
GPL_A0 GPL_B0	C5	Output
OE GPL_A1 GPL_B1	D5	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	A4, B4	Output
UPWAITA GPL_A4	C2	Bidirectional (3.3 V only)
GPL_A5	E4	Output
PORESET	P1	Input (3.3 V only)
RSTCONF	K4	Input (3.3 V only)
HRESET	J4	Open-drain
SRESET	M3	Open-drain
XTAL	N1	Analog Output

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
EXTAL	M1	Analog Input (1.8 V only)
CLKOUT	N6	Output
EXTCLK	N2	Input (1.8 V only)
ALE_A	H1	Output
$\overline{\text{CE1\_A}}$	E5	Output
$\overline{\text{CE2\_A}}$	B3	Output
$\overline{\text{WAIT\_A}}$	N3	Input (3.3 V only)
IP_A0	T2	Input (3.3 V only)
IP_A1	M6	Input (3.3 V only)
IP_A2, $\overline{\text{IOIS16\_A}}$	R3	Input (3.3 V only)
IP_A3	M5	Input (3.3 V only)
IP_A4	T3	Input (3.3 V only)
IP_A5	N5	Input (3.3 V only)
IP_A6	M7	Input (3.3 V only)
IP_A7	R2	Input (3.3 V only)
DSCK	H2	Bidirectional Three-state (3.3 V only)
IWP[0:1], VFLS[0:1]	H3, G1	Bidirectional (3.3 V only)
OP0	K1	Bidirectional (3.3 V only)
OP1	K2	Output
OP2, MODCK1, $\overline{\text{STS}}$	K3	Bidirectional (3.3 V only)
OP3, MODCK2, DSDO	L1	Bidirectional (3.3 V only)
BADDR[28:29]	L3, L2	Output
BADDR30, $\overline{\text{REG}}$	J3	Output
$\overline{\text{AS}}$	J2	Input (3.3 V only)
PA11, RXD3	E16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA10, TXD3	H15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA9, RXD4	J16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA8, TXD4	J15	Bidirectional (Optional: Open-drain) (5-V tolerant)

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PA3, CLK5, BRGO3, TIN3	K16	Bidirectional (5-V tolerant)
PA2, CLK6, $\overline{\text{TOUT3}}$	K14	Bidirectional (5-V tolerant)
PA1, CLK7, BRGO4, TIN4	L15	Bidirectional (5-V tolerant)
PA0, CLK8, $\overline{\text{TOUT4}}$	M16	Bidirectional (5-V tolerant)
PB31, $\overline{\text{SPISEL}}$	E13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	F13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	D15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	G13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	H16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	L16	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	C16	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	E14	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	E15	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	J14	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	K15	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	J13	Bidirectional (5-V tolerant)

16.1.2 The non-JEDEC Pinout

Figure 64 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *PowerQUICC™ Family Reference Manual*.

NOTE: This figure shows the top view of the device.

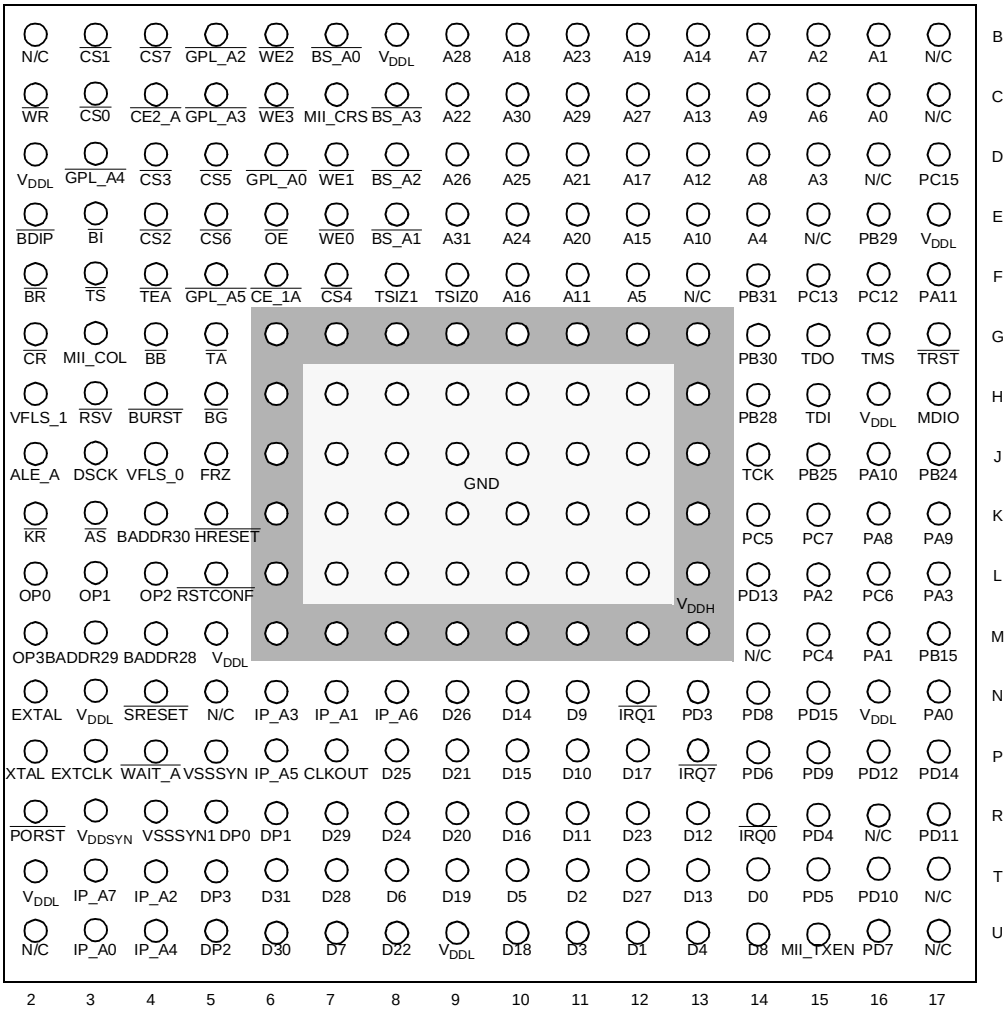

Figure 64. Pinout of PBGA Package—Non-JEDEC

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