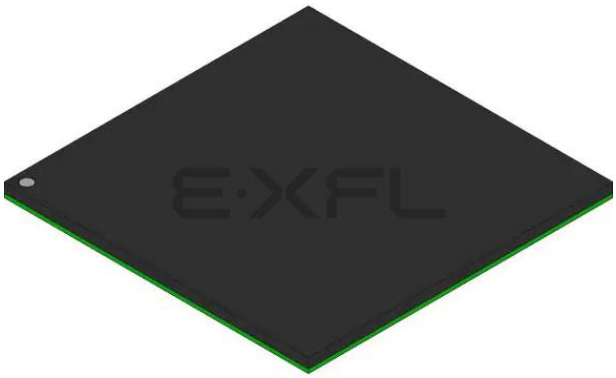

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc852tczt66a

1 Overview

The MPC852T is a 0.18-micron derivative of the MPC860 PowerQUICC™ family, and can operate up to 100 MHz on the MPC8xx core with a 66-MHz external bus. The MPC852T has a 1.8-V core and a 3.3-V I/O operation with 5-V TTL compatibility. The MPC852T integrated communications controller is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in Ethernet control applications, including CPE equipment, Ethernet routers and hubs, VoIP clients, and WiFi access points.

The MPC852T is a PowerPC architecture-based derivative of the MPC860 Quad Integrated Communications Controller (PowerQUICC). The CPU on the MPC852T is a MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches. The MPC852T is the subset of this family of devices.

2 Features

The MPC852T is comprised of three modules that each use a 32-bit internal bus: an MPC8xx core, system integration unit (SIU), and communication processor module (CPM).

The following list summarizes the key MPC852T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - 50/66 MHz core frequencies support both 1:1 and 2:1 modes
  - 80/100 MHz core frequencies support 2:1 mode only
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - 4-Kbyte instruction caches is two-way, set-associative with 128 sets
    - 4-Kbyte data cachesis two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis
  - MMUs with 32-entry TLB, fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces, and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank

- Two baud rate generators
  - Independent (can be connected toany SCC3/4 or SMC1)
  - Allows changes during operation
  - Autobaud support option
- Two SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3® standard optional on SCC3 and SCC4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Universal asynchronous receiver transmitter (UART)
  - Totally transparent (bit streams)
  - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- One SMC (serial management channel)
  - UART
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one independent PCMCIA socket; 8-memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3-V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V tolerant pins.

Figure 1 shows the MPC852T block diagram.

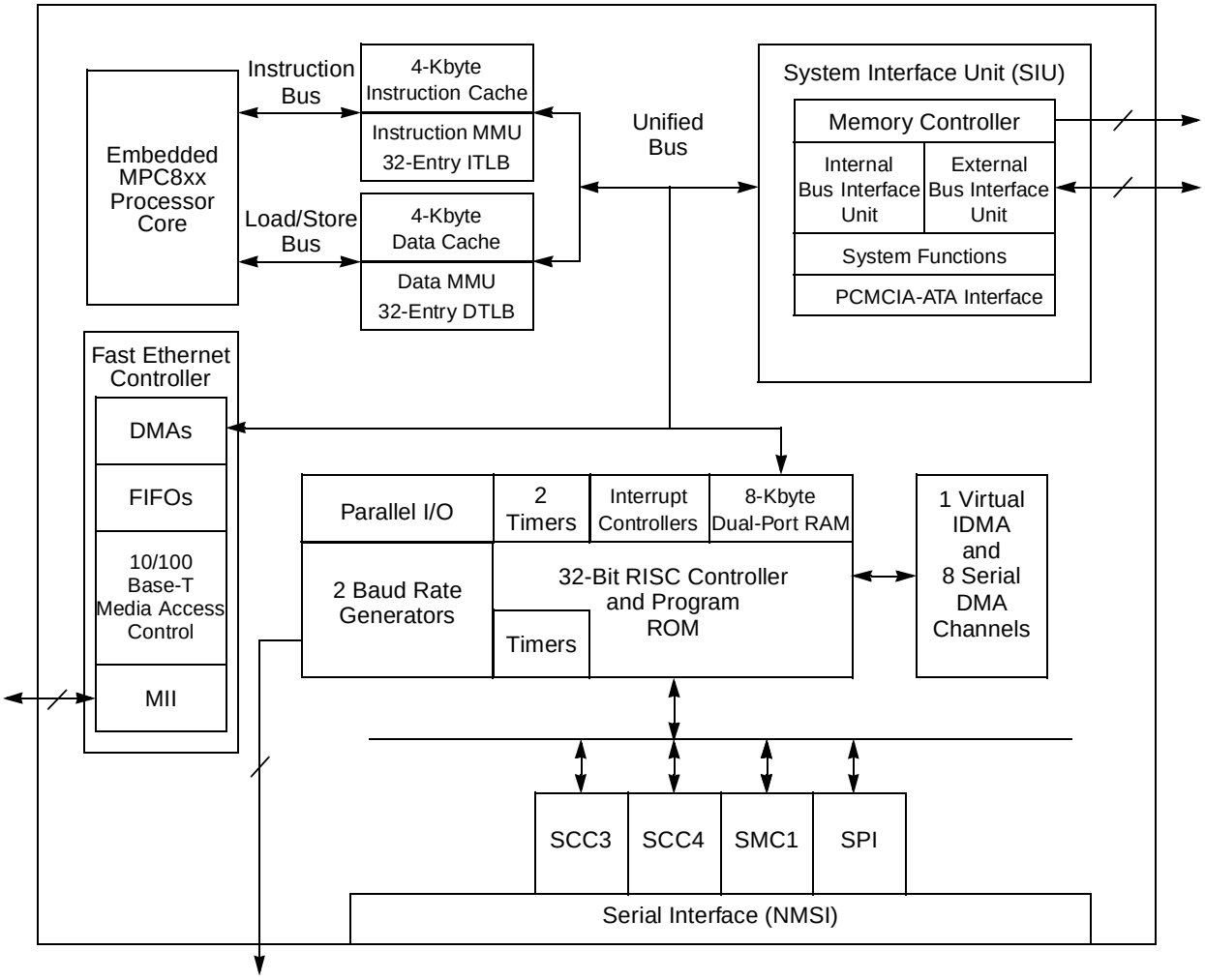


Figure 1. MPC852T Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC852T. Table 1 provides the maximum ratings and operating temperatures.

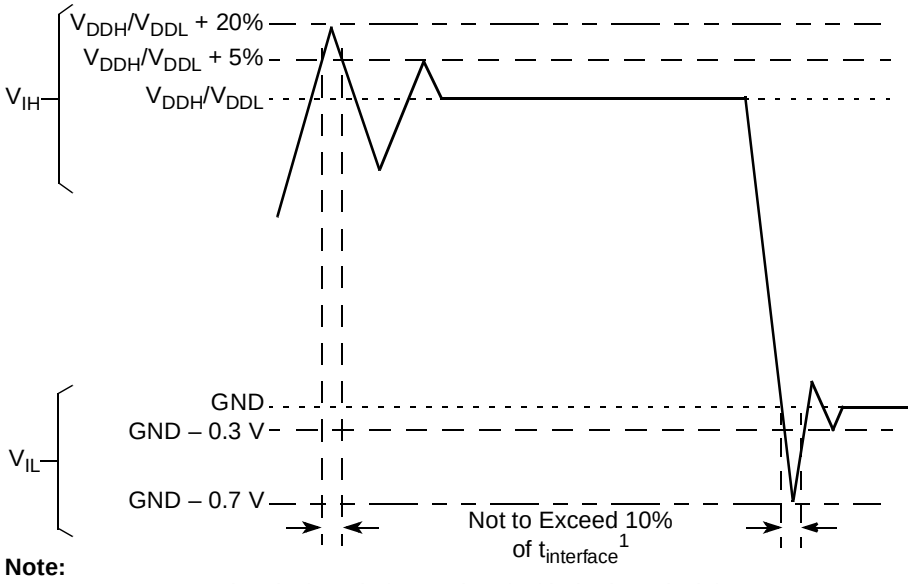
Table 1. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDL} (core voltage)	– 0.3 to 3.4	V
	V_{DDH} (I/O voltage)	– 0.3 to 4	V
	V_{DDSYN}	– 0.3 to 3.4	V
	Difference between V_{DDL} to V_{DDSYN}	100	mV
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	– 55 to +150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power-up and normal operation (that is, if the MPC852T is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 2 shows the undershoot and overshoot voltages at the interface of the MPC852T.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

where:

T_A = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. Thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature (ºC)

P_D = power dissipation in package

9 Power Supply and Power Sequencing

This section provides design considerations for the MPC852T power supply. The MPC852T has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}) that operates at a lower voltage than the I/O voltage V_{DDH}. The I/O section of the MPC852T is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15] PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO are 5-V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins can not exceed 5.5 V, and the remaining input pins cannot exceed 3.465 V. This restriction applies to power-on reset or power down and normal operation.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power-on reset or power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 3 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power-on reset, and the 1N5820 diodes regulate the maximum potential difference on power-down.

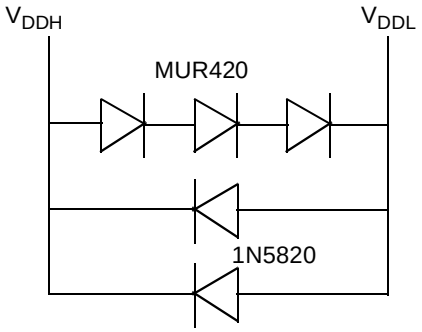


Figure 3. Example Voltage Sequencing Circuit

10 Mandatory Reset Configurations

The MPC852T requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion, the HRCW[DBGC] value that is needed to be set to binary X1 in the hardware reset configuration word (HRCW) and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset.

If hardware reset configuration word (HRCW) is disabled, by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset.

12 Bus Signal Timing

The maximum bus speed that the MPC852T supports is 66 MHz. Table 7 shows the frequency ranges for standard part frequencies.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core	40	50	40	66.67
Bus	40	50	40	66.67

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core	40	50	40	66.67	40	80	40	100
Bus 2:1	20	25	20	33.33	20	40	20	50

Table 9 provides the bus operation timing for the MPC852T at 33, 40, 50, and 66 MHz.

The timing for the MPC852T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT) See Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK[1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns

Figure 8 provides the timing for the synchronous input signals.

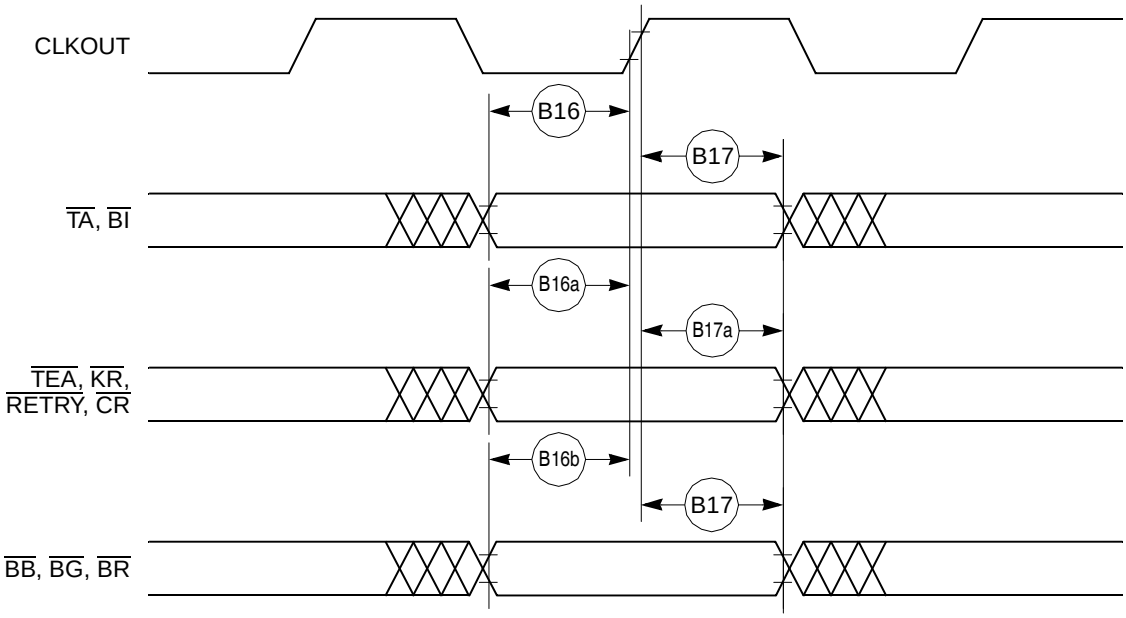


Figure 8. Synchronous Input Signals Timing

Figure 9 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

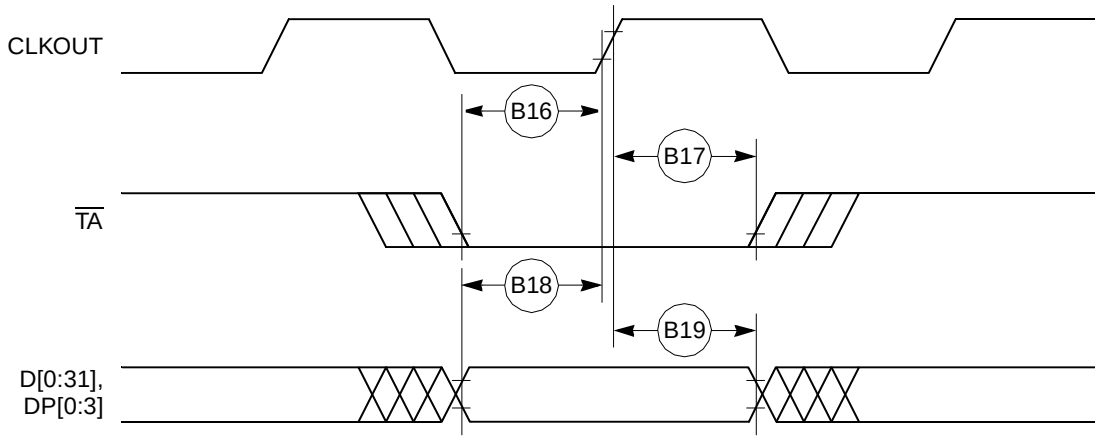


Figure 9. Input Data Timing in Normal Case

Figure 10 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

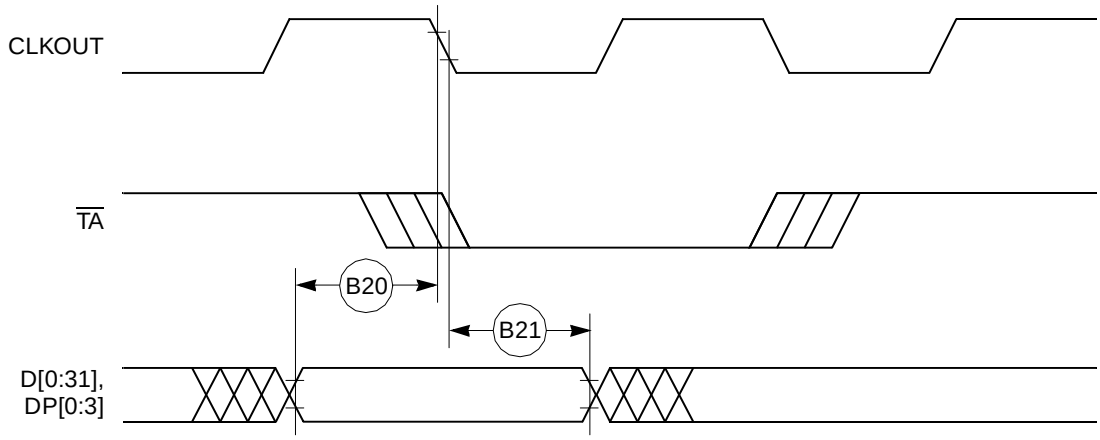


Figure 10. Input Data Timing When Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 11 through Figure 14 provide the timing for the external bus read that various GPCM factors control.

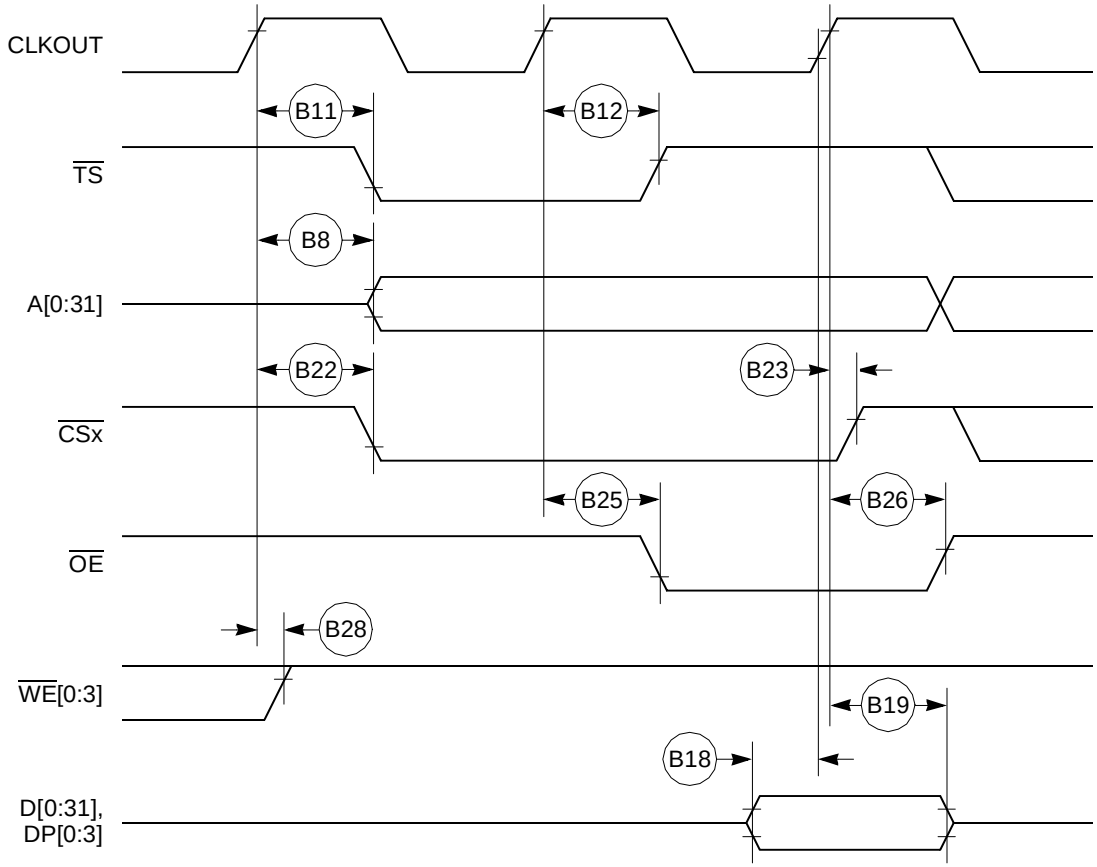


Figure 11. External Bus Read Timing (GPCM Controlled—ACS = 00)

Figure 18 provides the timing for the external bus that the UPM controls.

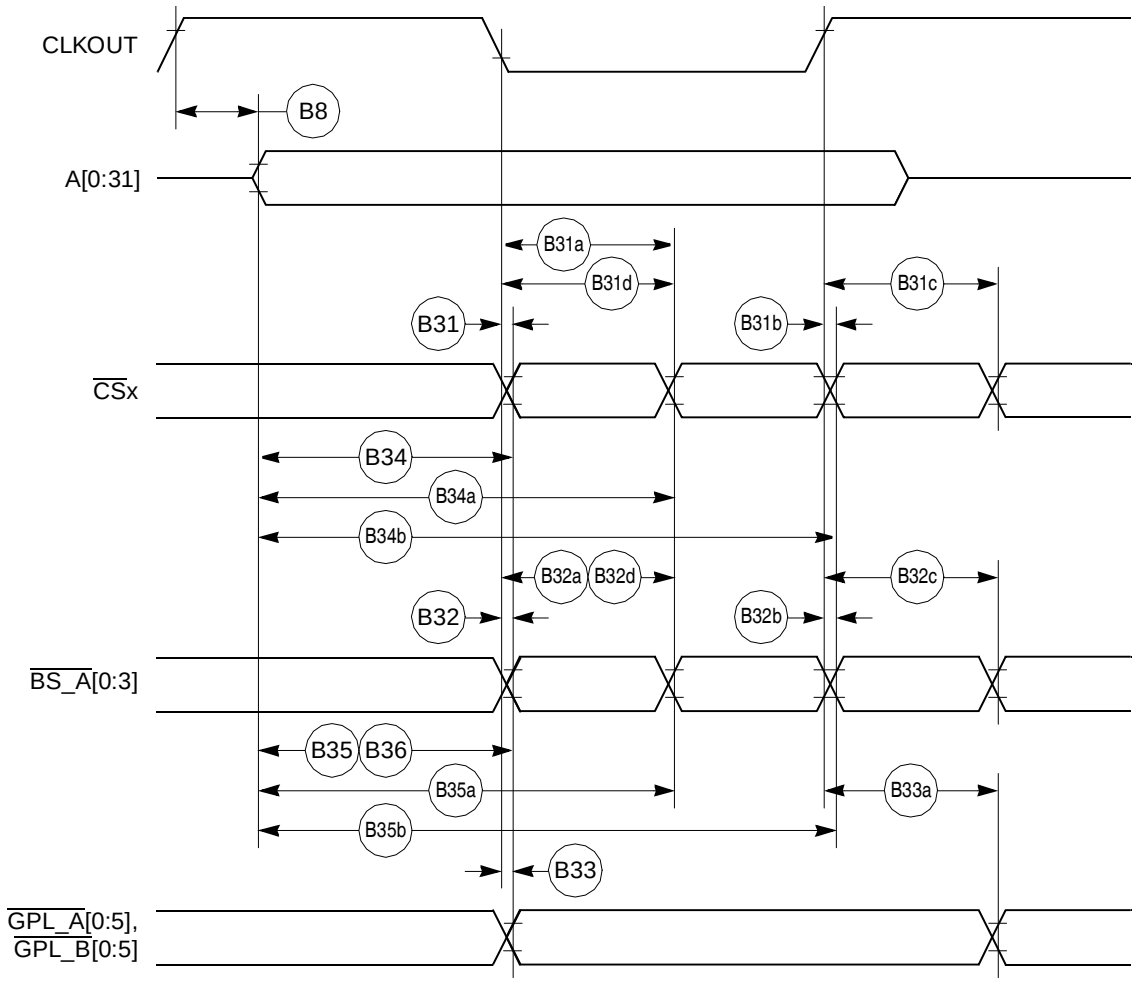


Figure 18. External Bus Timing (UPM Controlled Signals)

Figure 19 provides the timing for the asynchronous asserted UPWAIT signal that the UPM controls.

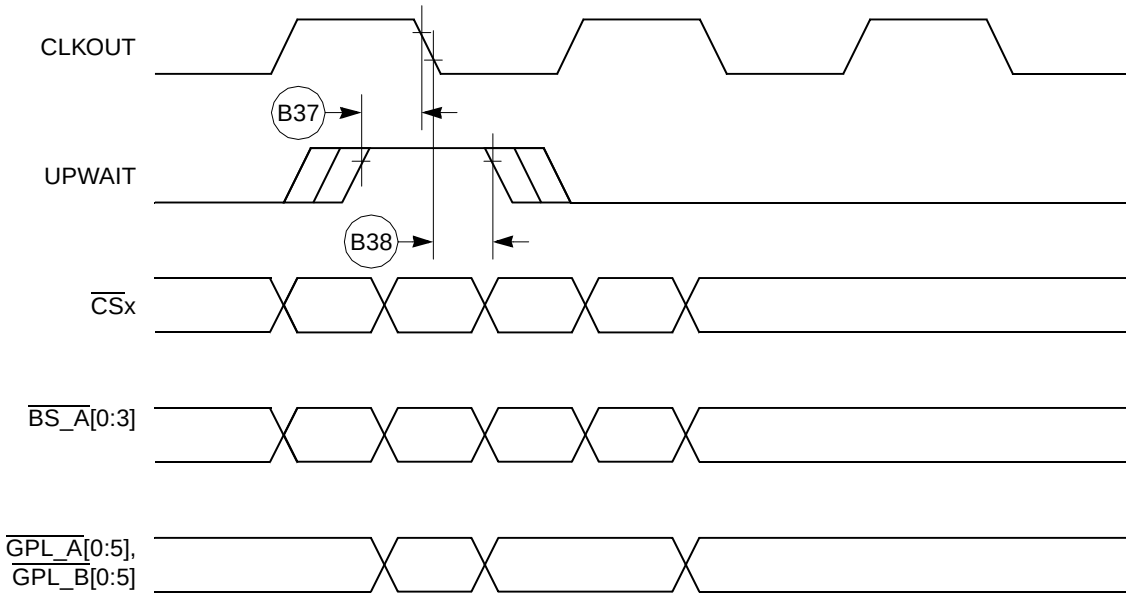


Figure 19. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 20 provides the timing for the asynchronous negated UPWAIT signal that the UPM controls.

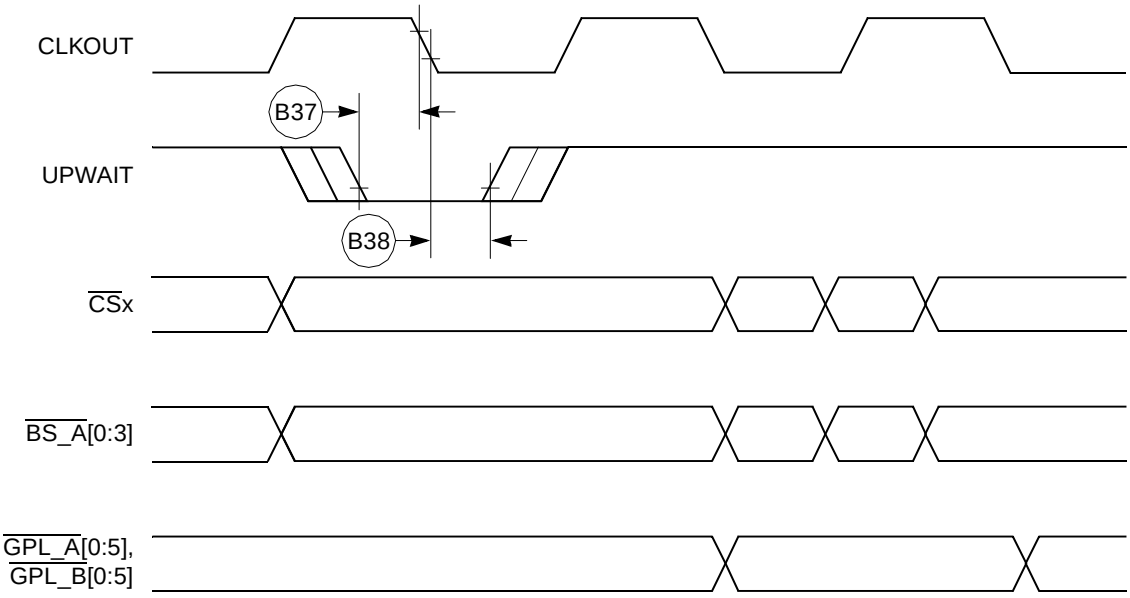


Figure 20. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Table 10 provides interrupt timing for the MPC852T.

Table 10. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (set up time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

1 The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and need not be asserted or negated with reference to the CLKOUT. The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and have no direct relation with the total system interrupt latency that the MPC852T is able to support.

Figure 24 provides the interrupt detection timing for the external level-sensitive lines.

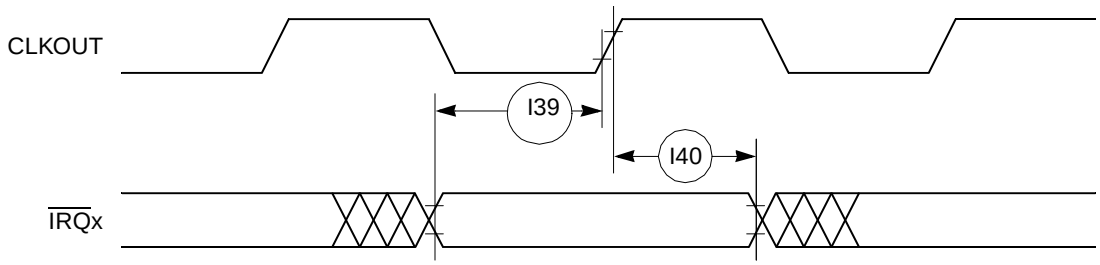


Figure 24. Interrupt Detection Timing for External Level Sensitive Lines

Figure 25 provides the interrupt detection timing for the external edge-sensitive lines.

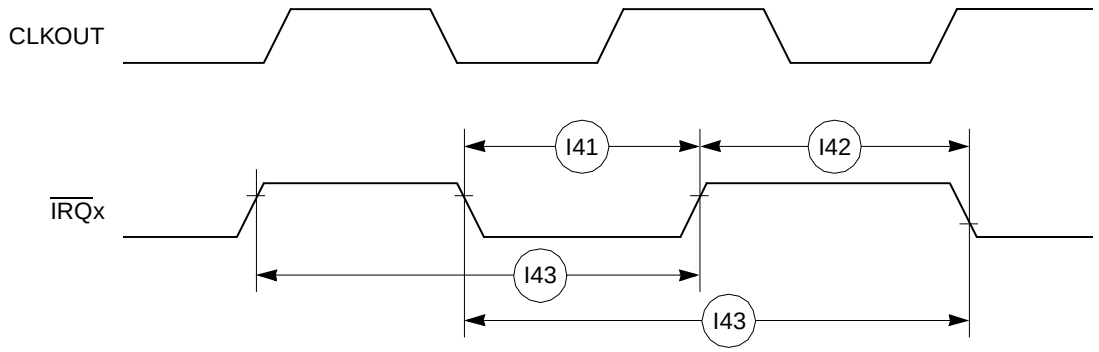


Figure 25. Interrupt Detection Timing for External Edge Sensitive Lines

Figure 26 provides the PCMCIA access cycle timing for the external bus read.

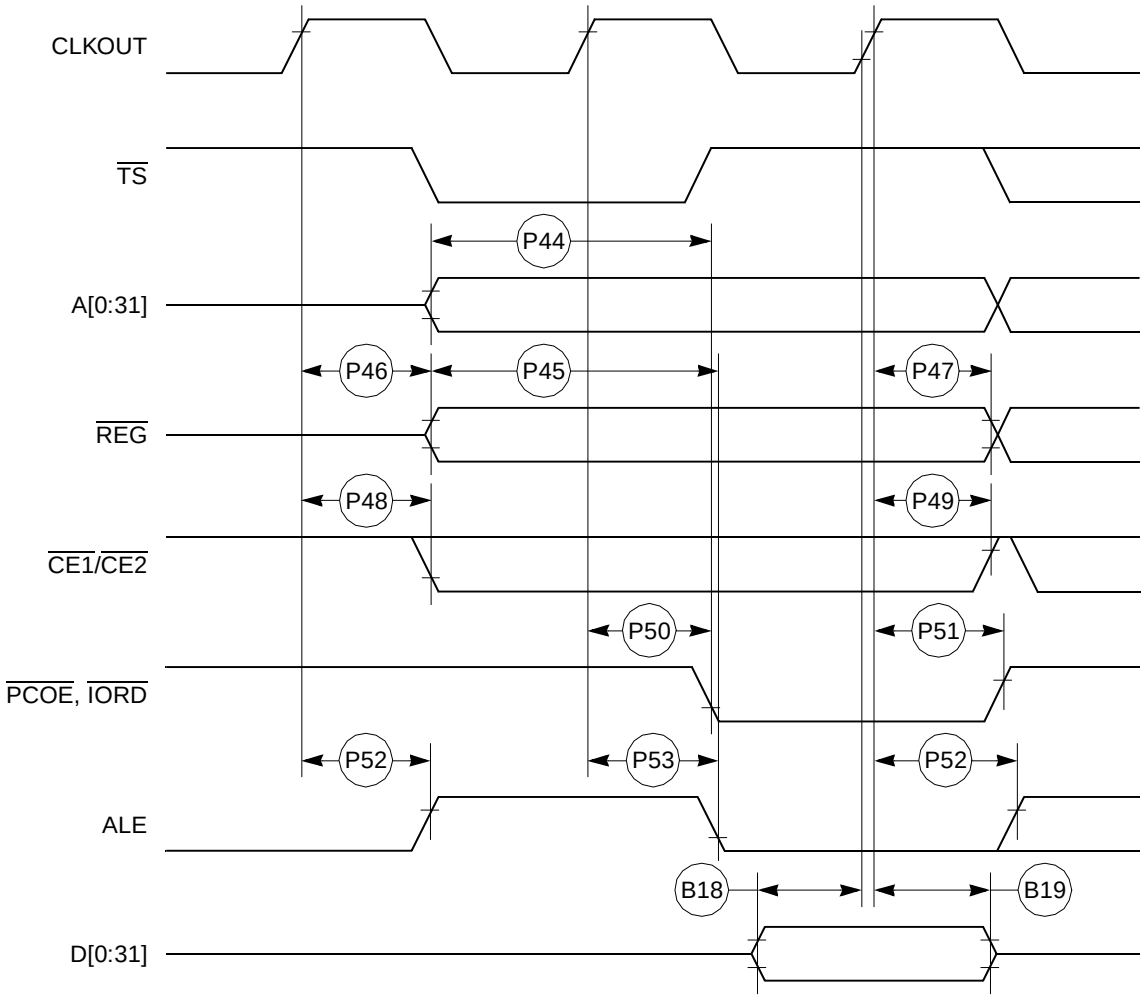


Figure 26. PCMCIA Access Cycles Timing External Bus Read

Figure 27 provides the PCMCIA access cycle timing for the external bus write.

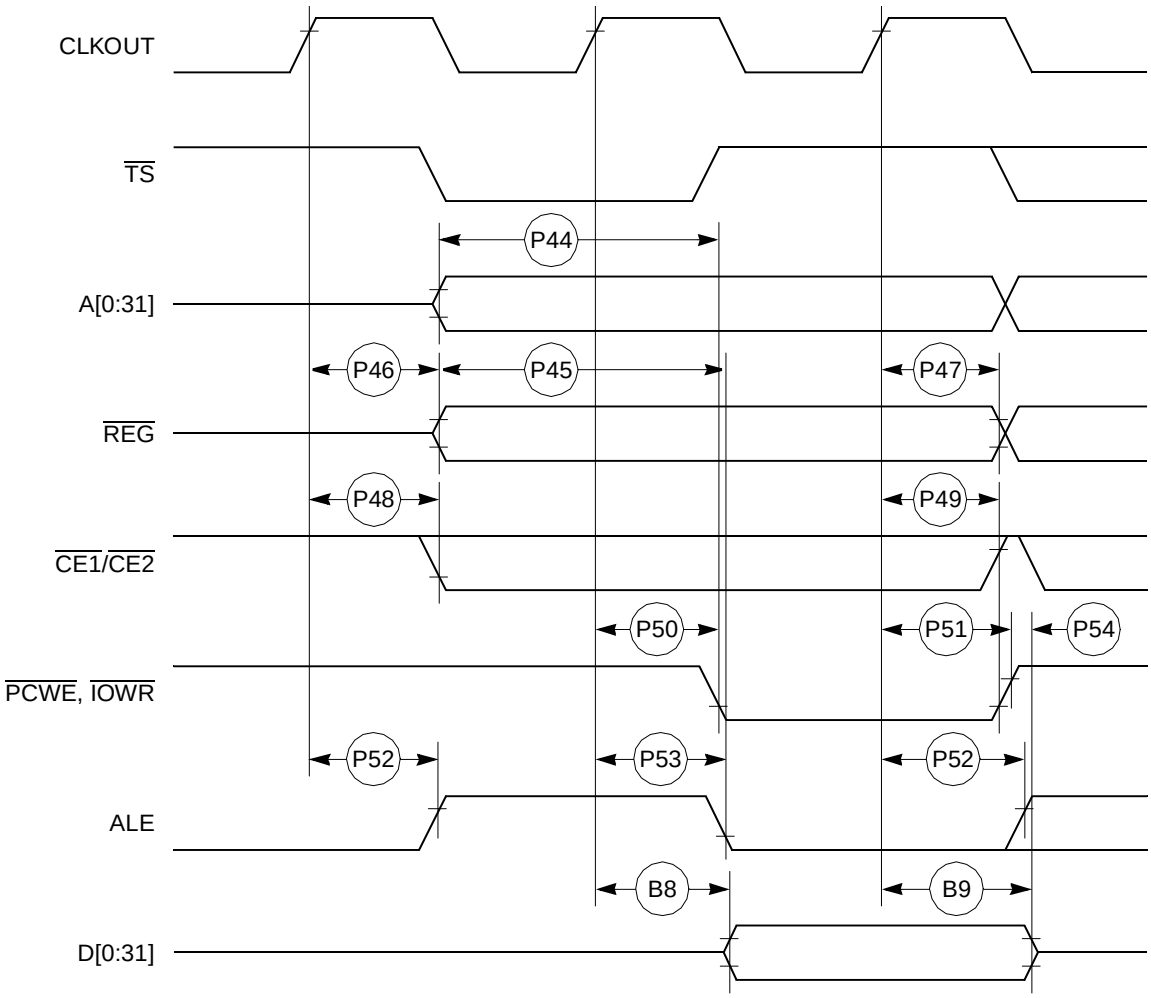


Figure 27. PCMCIA Access Cycles Timing External Bus Write

Figure 28 provides the PCMCIA WAIT signals detection timing.

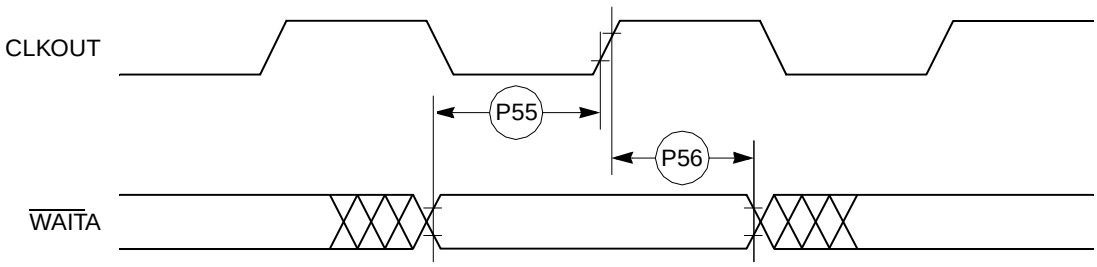


Figure 28. PCMCIA WAIT Signals Detection Timing

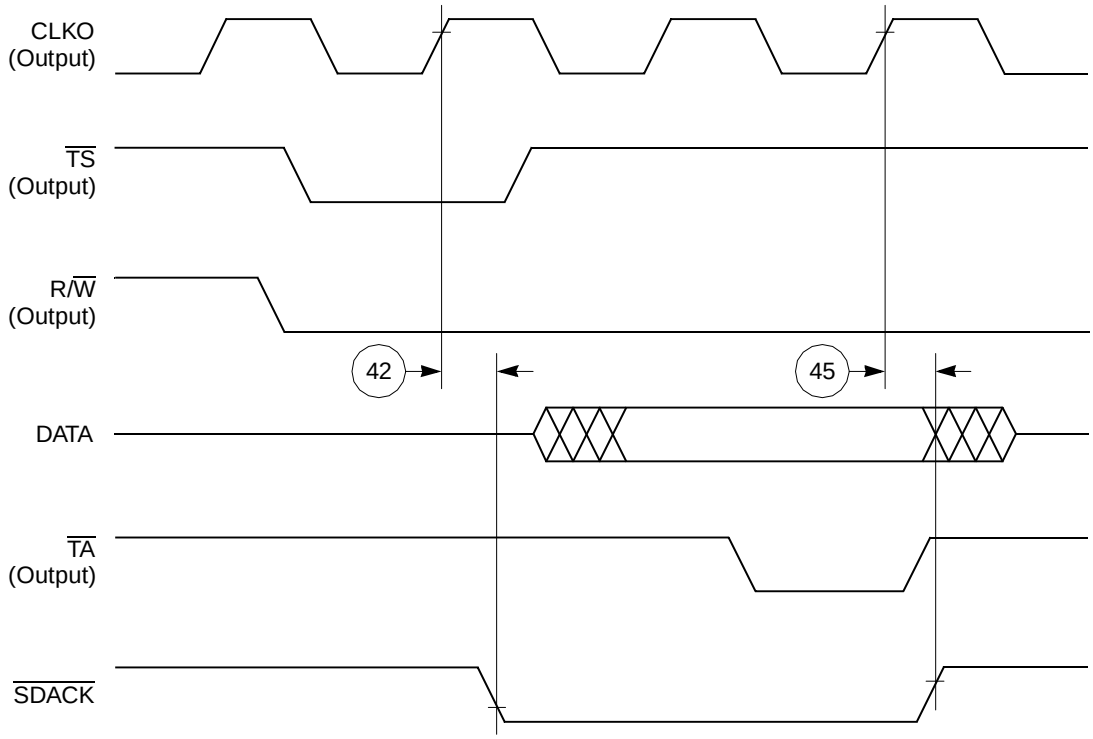


Figure 44. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

14.3 Baud Rate Generator AC Electrical Specifications

Table 18 provides the baud rate generator timings as shown in Figure 45.

Table 18. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

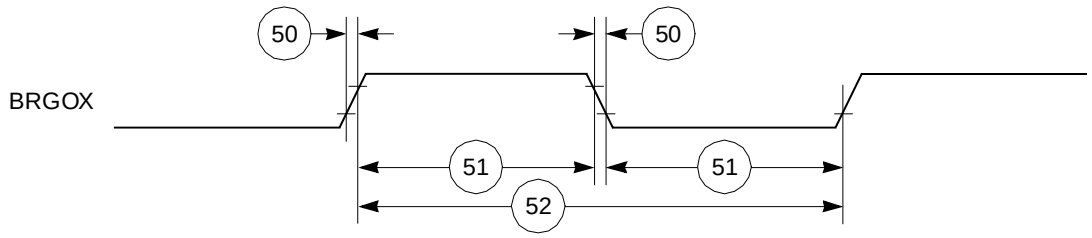


Figure 45. Baud Rate Generator Timing Diagram

Figure 47 through Figure 49 show the NMSI timings.

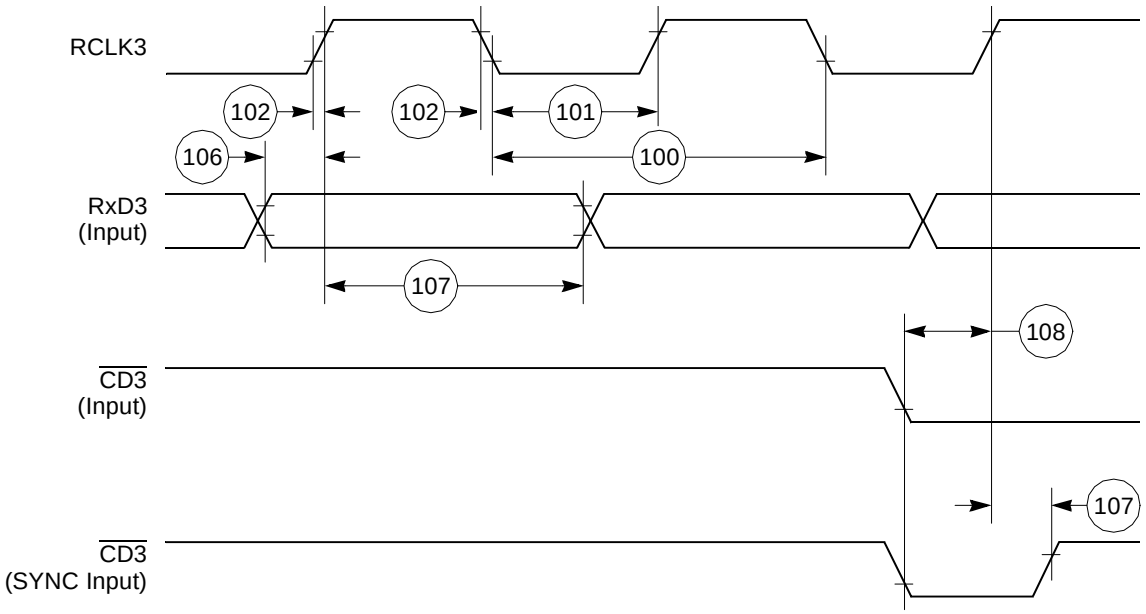


Figure 47. SCC NMSI Receive Timing Diagram

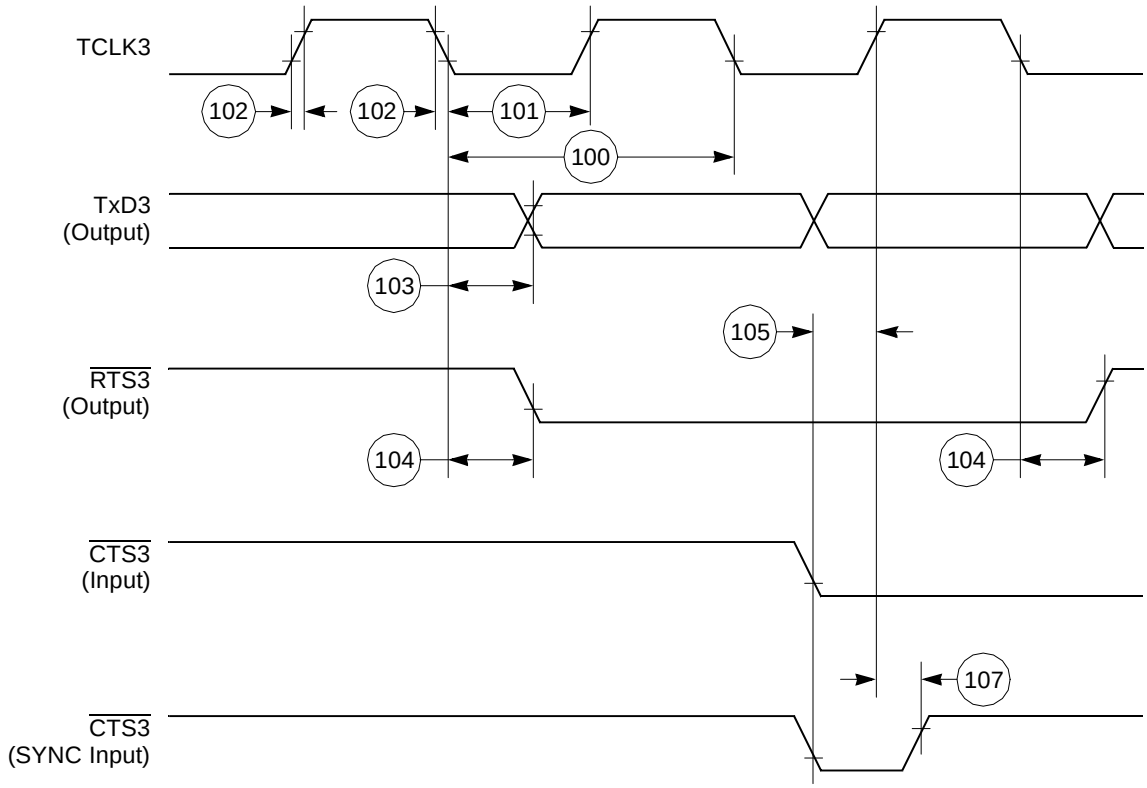


Figure 48. SCC NMSI Transmit Timing Diagram

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK3 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK3 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

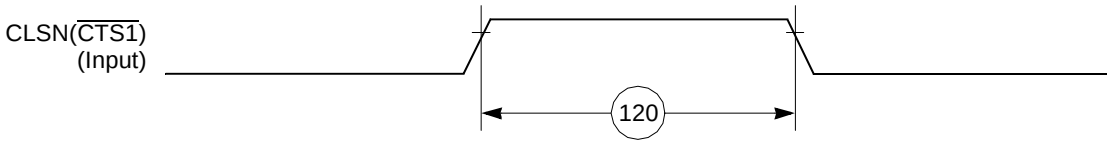


Figure 50. Ethernet Collision Timing Diagram

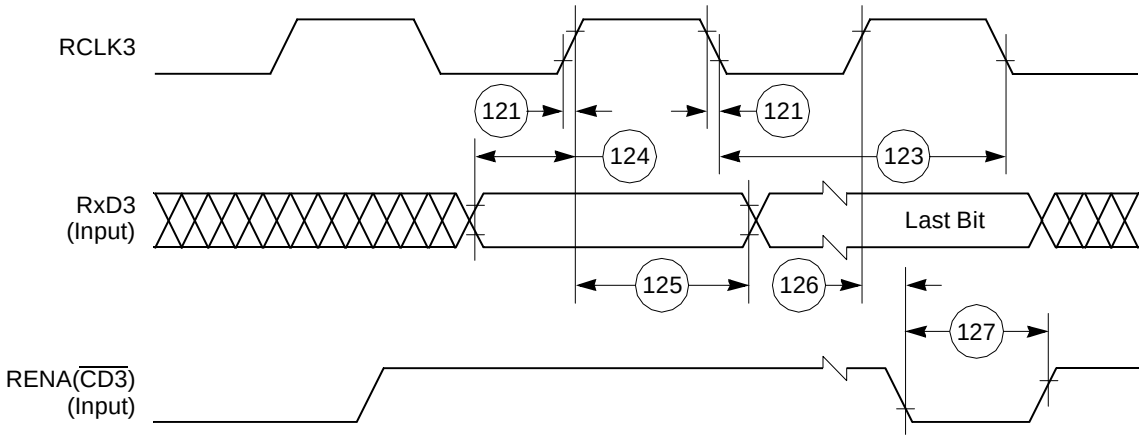


Figure 51. Ethernet Receive Timing Diagram

16.1.2 The non-JEDEC Pinout

Figure 64 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *PowerQUICC™ Family Reference Manual*.

NOTE: This figure shows the top view of the device.

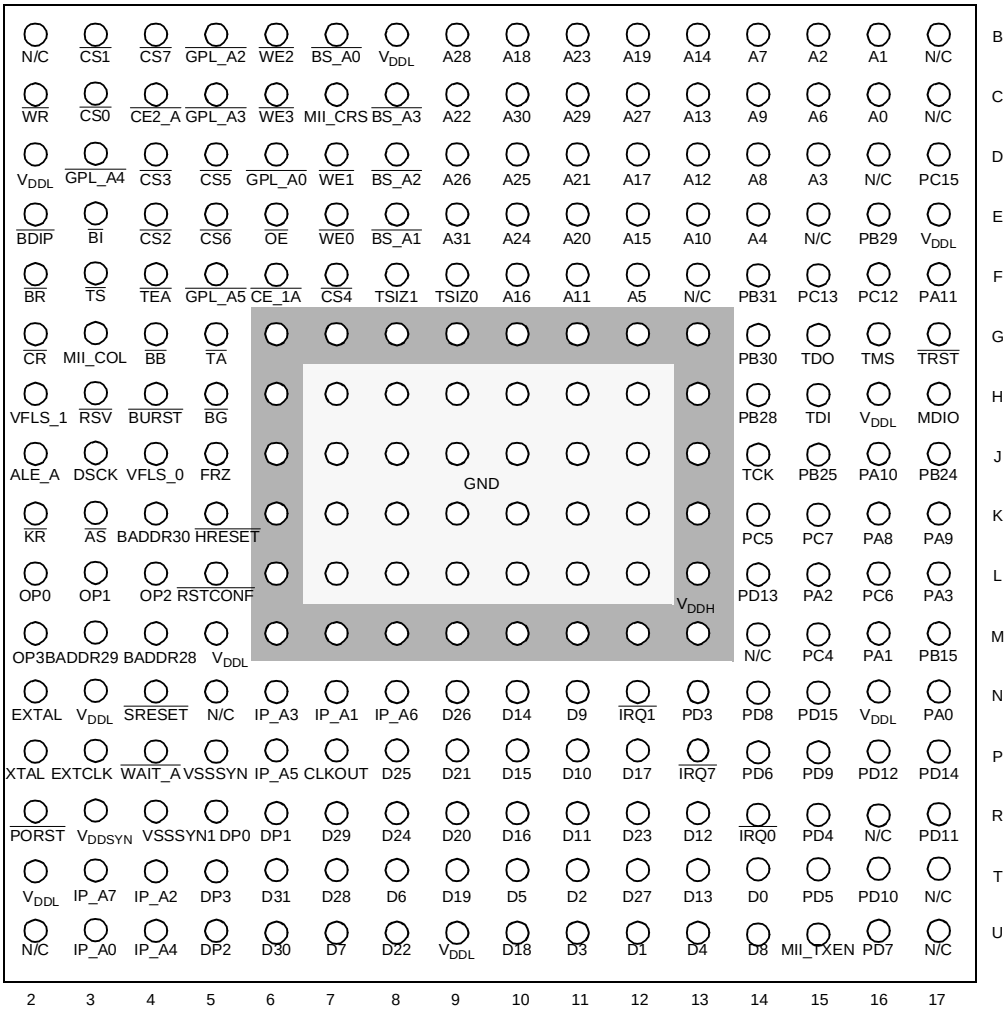


Figure 64. Pinout of PBGA Package—Non-JEDEC

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
$\overline{BB}$	G4	Bidirectional Active Pull-up (3.3 V only)
FRZ, $\overline{IRQ6}$	J5	Bidirectional (3.3 V only)
$\overline{IRQ0}$	R14	Input (3.3 V only)
$\overline{IRQ1}$	N12	Input (3.3 V only)
$\overline{IRQ7}$, M_TX_CLK	P13	Input (3.3 V only)
$\overline{CS}$[0:5]	C3, B3, E4, D4, F7, D5	Output
$\overline{CS6}$	E5	Output
$\overline{CS7}$	B4	Output
$\overline{WE0}$, BS_B0, $\overline{IORD}$	E7	Output
$\overline{WE1}$, BS_B1, $\overline{IOWR}$	D7	Output
$\overline{WE2}$, BS_B2, $\overline{PCOE}$	B6	Output
$\overline{WE3}$, BS_B3, $\overline{PCWE}$	C6	Output
$\overline{BS\_A}$[0:3]	B7, E8, D8, C8	Output
$\overline{GPL\_A0}$, $\overline{GPL\_B0}$	D6	Output
$\overline{OE}$, $\overline{GPL\_A1}$, $\overline{GPL\_B1}$	E6	Output
$\overline{GPL\_A}$[2:3], $\overline{GPL\_B}$[2:3], $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA, $\overline{GPL\_A4}$	D3	Bidirectional (3.3 V only)
$\overline{GPL\_A5}$	F5	Output
$\overline{PORESET}$	R2	Input (3.3 V only)
$\overline{RSTCONF}$	L5	Input (3.3 V only)
$\overline{HRESET}$	K5	Open-drain
$\overline{SRESET}$	N4	Open-drain
XTAL	P2	Analog output
EXTAL	N2	Analog input (3.3 V only)
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{CE1\_A}$	F6	Output
$\overline{CE2\_A}$	C4	Output
$\overline{WAIT\_A}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
IP_A1	N7	Input (3.3 V only)
IP_A2, $\overline{\text{IOIS16\_A}}$	T4	Input (3.3 V only)
IP_A3	N6	Input (3.3 V only)
IP_A4	U4	Input (3.3 V only)
IP_A5	P6	Input (3.3 V only)
IP_A6	N8	Input (3.3 V only)
IP_A7	T3	Input (3.3 V only)
DSCK	J3	Bidirectional Three-state (3.3 V only)
IWP[0:1], VFLS[0:1]	J4, H2	Bidirectional (3.3 V only)
OP0	L2	Bidirectional (3.3 V only)
OP1	L3	Output
OP2, MODCK1, $\overline{\text{STS}}$	L4	Bidirectional (3.3 V only)
OP3, MODCK2, DSDO	M2	Bidirectional (3.3 V only)
BADDR[28:29]	M4, M3	Output
BADDR30, $\overline{\text{REG}}$	K4	Output
$\overline{\text{AS}}$	K3	Input (3.3 V only)
PA11, RXD3	F17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA10, TXD3	J16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA9, RXD4	K17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA8, TXD4	K16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA3, CLK5, BRGO3, TIN3	L17	Bidirectional (5-V tolerant)
PA2, CLK6, $\overline{\text{TOUT3}}$	L15	Bidirectional (5-V tolerant)
PA1, CLK7, BRGO4, TIN4	M16	Bidirectional (5-V tolerant)
PA0, CLK8, $\overline{\text{TOUT4}}$	N17	Bidirectional (5-V tolerant)