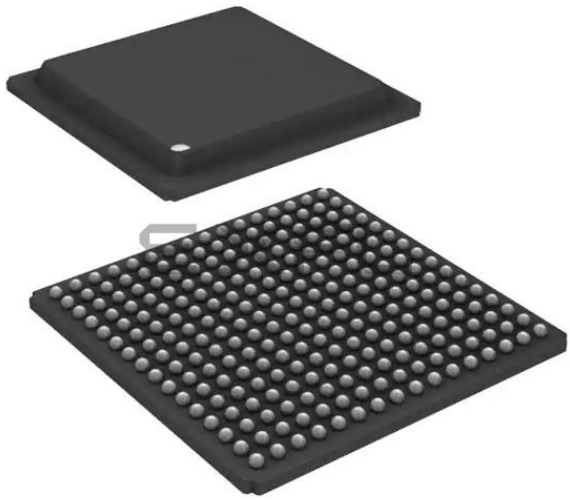


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc852tczt80a

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC852T. Table 1 provides the maximum ratings and operating temperatures.

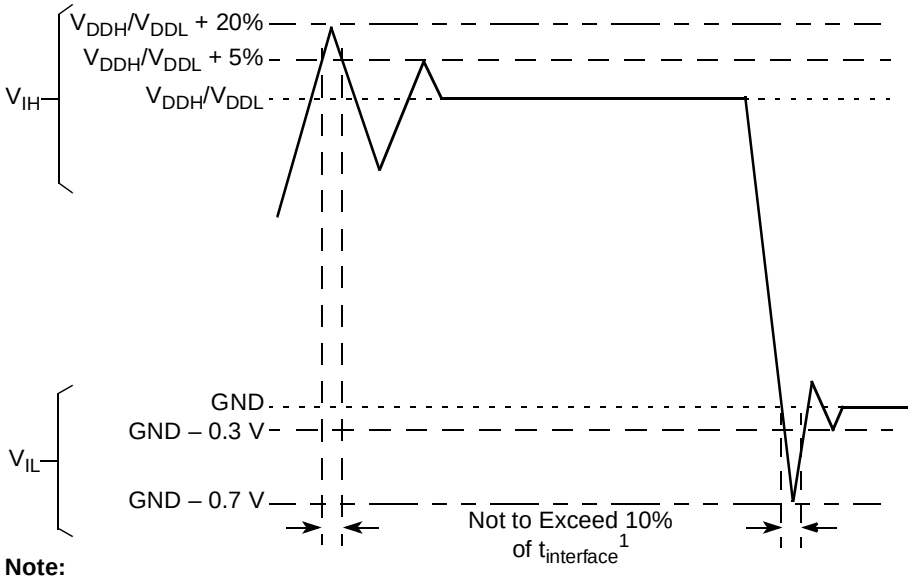
Table 1. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDL} (core voltage)	– 0.3 to 3.4	V
	V_{DDH} (I/O voltage)	– 0.3 to 4	V
	V_{DDSYN}	– 0.3 to 3.4	V
	Difference between V_{DDL} to V_{DDSYN}	100	mV
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	– 55 to +150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power-up and normal operation (that is, if the MPC852T is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 2 shows the undershoot and overshoot voltages at the interface of the MPC852T.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

Table 2. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature [1] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	– 40	°C
	$T_{j(max)}$	100	°C

1 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

This device contains circuitry protecting against damage that high-static voltage or electrical fields cause; however, Freescale recommends taking normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC852T.

Table 3. MPC852T Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient[1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$[2]	49	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	32	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$[3]	41	
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	29	
Junction-to-board[4]			$R_{\theta JB}$	24	
Junction-to-case[5]			$R_{\theta JC}$	13	
Junction-to-package top[6]	Natural convection		Ψ_{JT}	3	
	Airflow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal

3 Per JEDEC JESD51-6 with the board horizontal

4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR should be configured with the mandatory value in Table 6 in the boot code after the reset deasserts.

Table 6. Mandatory Reset Configuration of MPC852T

Register/Configuration	Field	Value (Binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	X1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	X1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[4–7] PAPAR[12–15]	0
PADIR (Port A data direction register)	PADIR[4–7] PADIR[12–15]	1
PBPAR (Port B pin assignment register)	PBPAR[14] PBPAR[16–23] PBPAR[26–27]	0
PBDIR (Port B data direction register)	PBDIR[14] PBDIR[16–23] PBDIR[26–27]	1
PCPAR (Port C pin assignment register)	PCPAR[8–11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8–11] PCDIR[14]	1

11 Layout Practices

Each V_{DD} pin on the MPC852T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC852T have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized to minimize undershoot and reflections that these fast output switching times cause. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances that the PC traces cause. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads, because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that are inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to the *MPC866 PowerQUICC™ Family Reference Manual*, Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})."

12 Bus Signal Timing

The maximum bus speed that the MPC852T supports is 66 MHz. Table 7 shows the frequency ranges for standard part frequencies.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core	40	50	40	66.67
Bus	40	50	40	66.67

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core	40	50	40	66.67	40	80	40	100
Bus 2:1	20	25	20	33.33	20	40	20	50

Table 9 provides the bus operation timing for the MPC852T at 33, 40, 50, and 66 MHz.

The timing for the MPC852T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT) See Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK[1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ Valid[3] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	9.80	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30[2])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0,1 CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30b	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B30c	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid- as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - As Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B37	UPWAIT valid to CLKOUT falling edge[10] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[10] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[11] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the maximum allowed jitter on EXTAL can be up to 2%.

2 For part speeds above 50MHz, use 9.80ns for B11a.

3 The timing required for $\overline{BR}$ input is relevant when the MPC852T is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC852T is selected to work with external bus arbiter.

4 For part speeds above 50MHz, use 2ns for B17.

5 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

6 For part speeds above 50MHz, use 2ns for B19.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 This formula applies to bus operation up to 50 MHz.

9 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

10 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 19.

11 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 22.

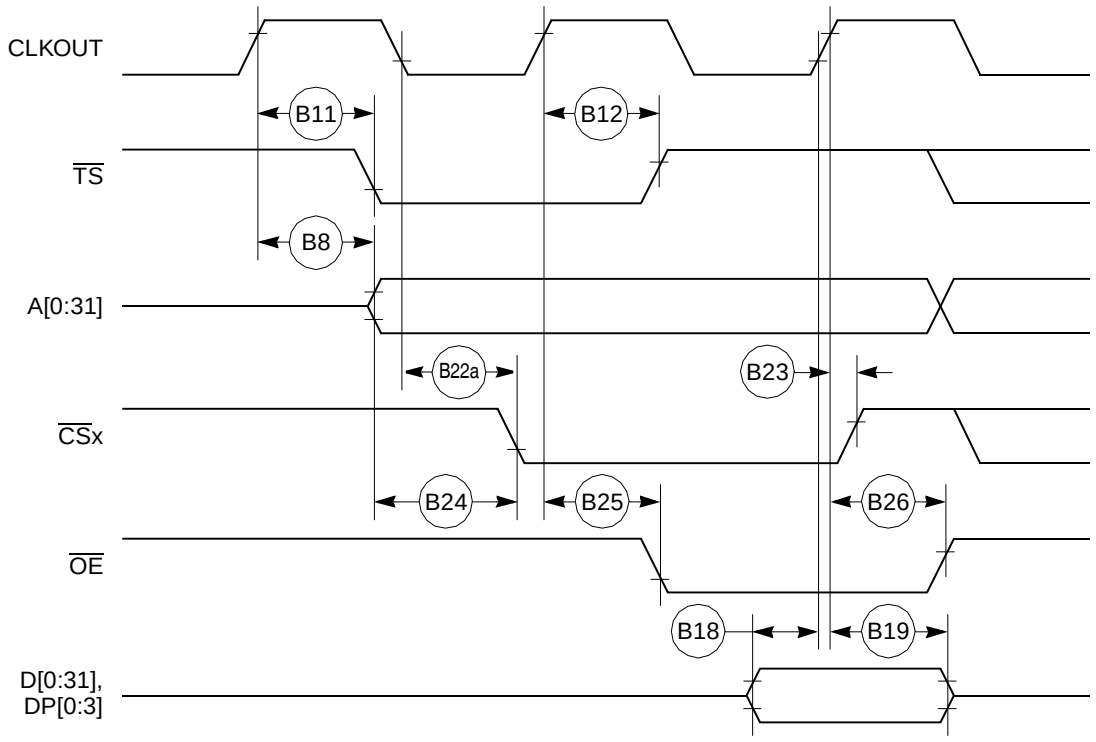


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

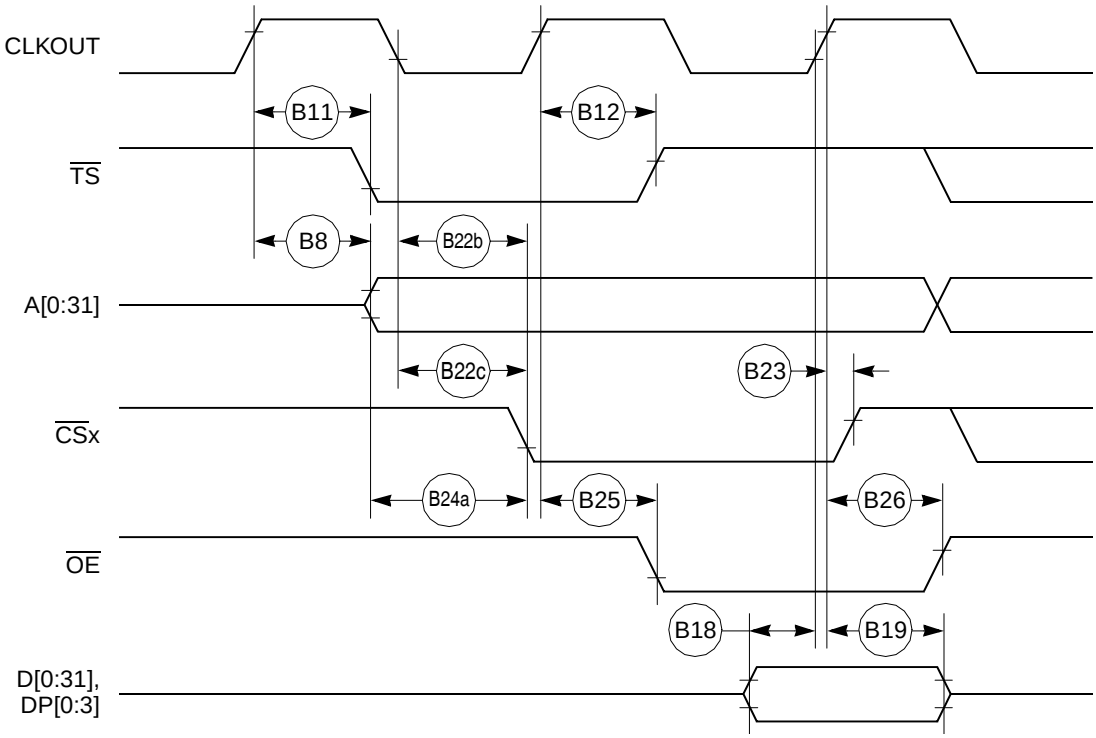


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

Figure 15 through Figure 17 provide the timing for the external bus write that various GPCM factors control.

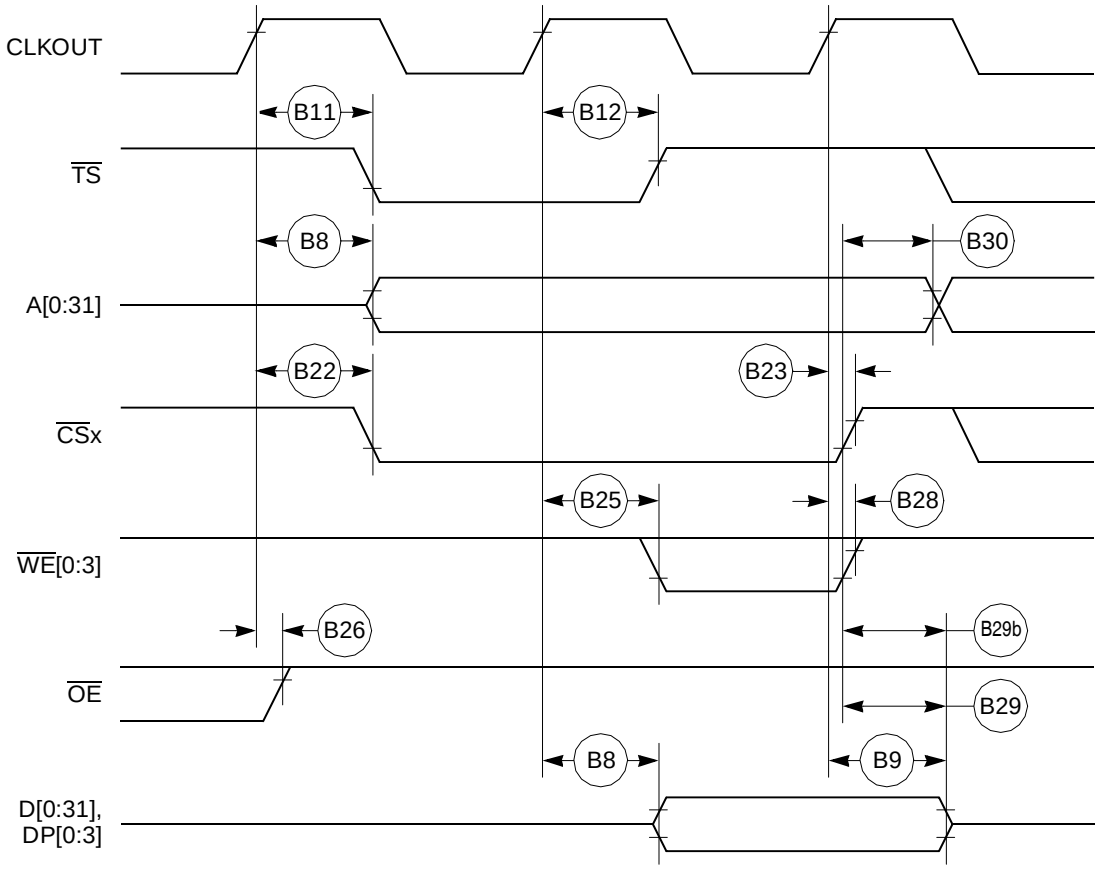


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

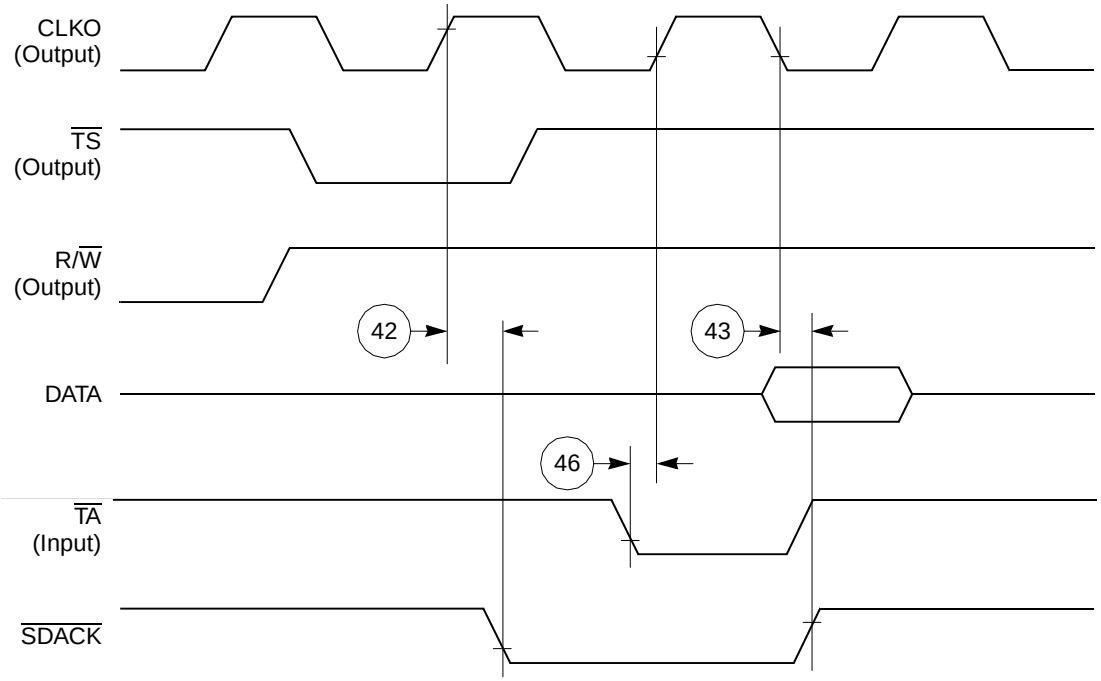


Figure 42. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

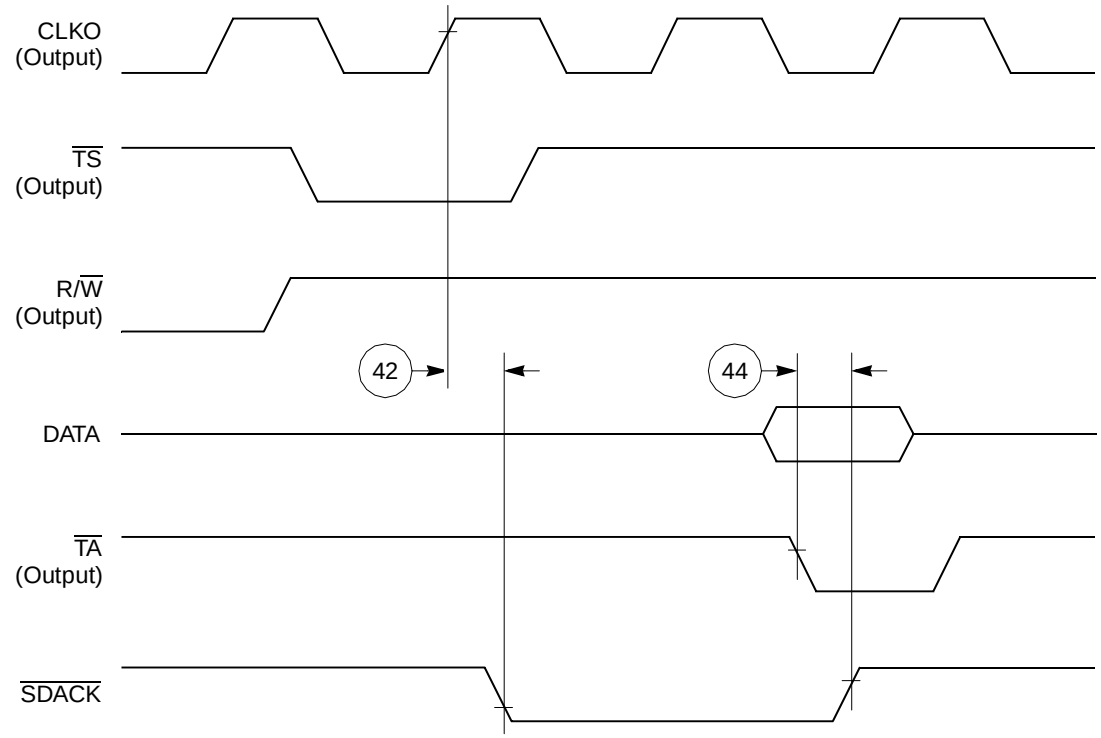


Figure 43. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

Table 20. NMSI External Clock Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
107	RXD3 hold time from RCLK3 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD3}}$ setup Time to RCLK3 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

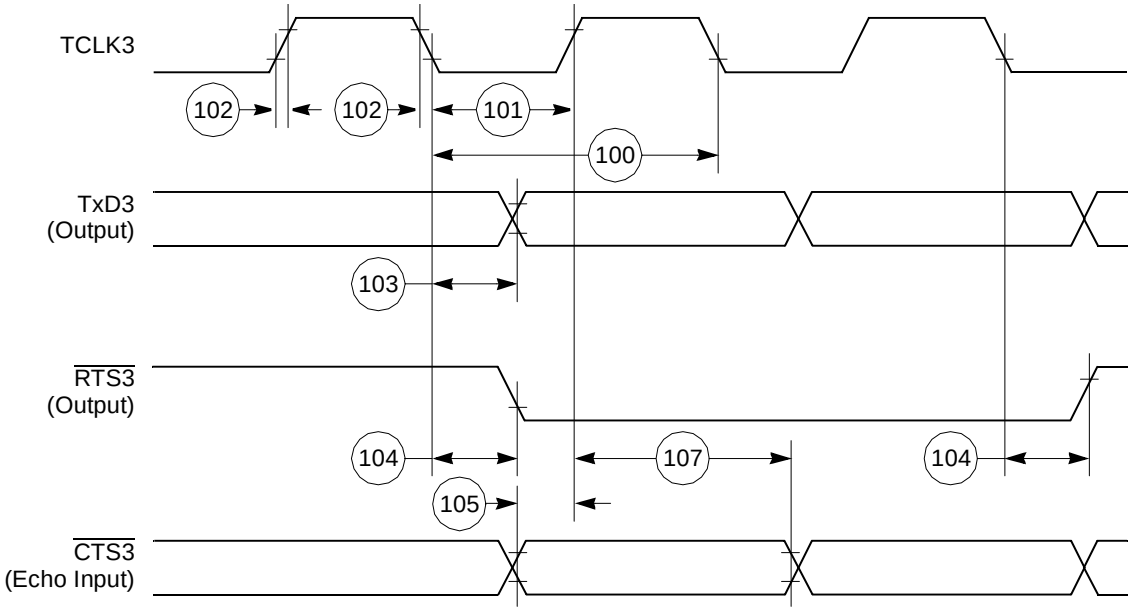


Figure 49. HDLC Bus Timing Diagram

14.6 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 50 through Figure 54.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	—	ns
123	RCLK3 clock period[1]	80	120	ns
124	RXD3 setup time	20	—	ns
125	RXD3 hold time	5	—	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	—	ns
130	TCLK3 clock period[1]	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	—	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns

14.7 SPI Master AC Electrical Specifications

Table 23 provides the SPI master timings as shown in Figure 55 and Figure 56.

Table 23. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

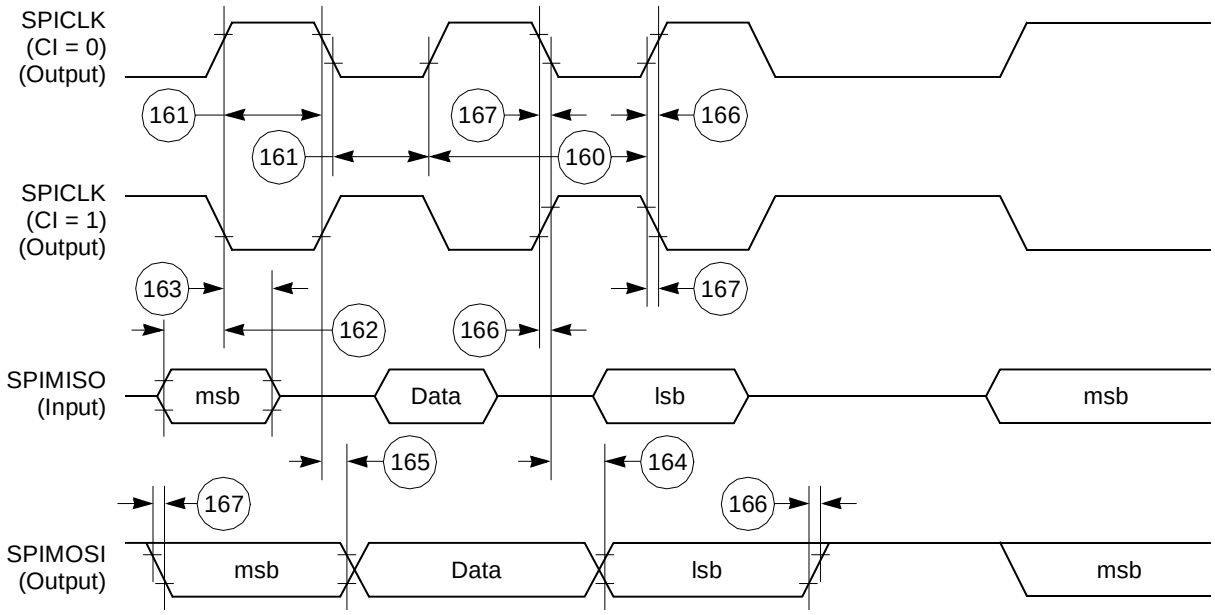


Figure 55. SPI Master (CP = 0) Timing Diagram

16 Mechanical Data and Ordering Information

Table 29 identifies the packages and operating frequencies orderable for the MPC852T.

Table 29. MPC852T Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (VR and ZT suffix)	0°C to 95°C	50	MPC852TVR50A MPC852TZT50A
		66	MPC852TVR66A MPC852TZT66A
		80	MPC852TVR80A MPC852TZT80A
		100	MPC852TVR100A MPC852TZT100A
Plastic ball grid array (CVR and CZTsuffix)	–40°C to 100°C	50	MPC852TCVR50A MPC852TCZT50A
		66	MPC852TCVR66A MPC852TCZT66A
		80	MPC852TCVR80A MPC852TCZT80A
		100	MPC852TCVR100A MPC852TCZT100A

16.1 Pin Assignments

The following sections give the pinout and pin listing for the JEDEC compliant and the non-JEDEC versions of the 16 × 16 PBGA package.

16.1.1 JEDEC Compliant Pinout

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC™ Family Reference Manual*.

NOTE: This is the top view of the device.

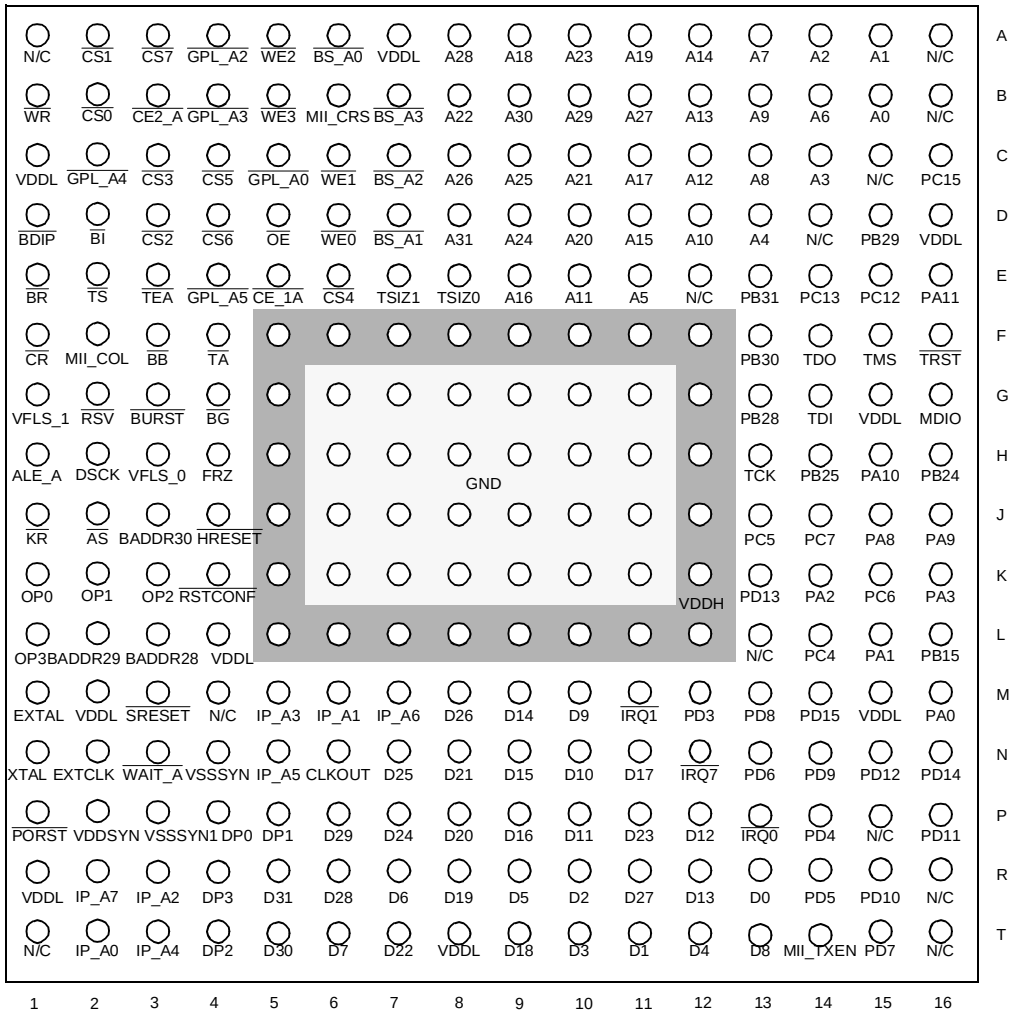


Figure 63. Pinout of PBGA Package—JEDEC Standard

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
EXTAL	M1	Analog Input (1.8 V only)
CLKOUT	N6	Output
EXTCLK	N2	Input (1.8 V only)
ALE_A	H1	Output
$\overline{\text{CE1\_A}}$	E5	Output
$\overline{\text{CE2\_A}}$	B3	Output
$\overline{\text{WAIT\_A}}$	N3	Input (3.3 V only)
IP_A0	T2	Input (3.3 V only)
IP_A1	M6	Input (3.3 V only)
IP_A2, $\overline{\text{IOIS16\_A}}$	R3	Input (3.3 V only)
IP_A3	M5	Input (3.3 V only)
IP_A4	T3	Input (3.3 V only)
IP_A5	N5	Input (3.3 V only)
IP_A6	M7	Input (3.3 V only)
IP_A7	R2	Input (3.3 V only)
DSCK	H2	Bidirectional Three-state (3.3 V only)
IWP[0:1], VFLS[0:1]	H3, G1	Bidirectional (3.3 V only)
OP0	K1	Bidirectional (3.3 V only)
OP1	K2	Output
OP2, MODCK1, $\overline{\text{STS}}$	K3	Bidirectional (3.3 V only)
OP3, MODCK2, DSDO	L1	Bidirectional (3.3 V only)
BADDR[28:29]	L3, L2	Output
BADDR30, $\overline{\text{REG}}$	J3	Output
$\overline{\text{AS}}$	J2	Input (3.3 V only)
PA11, RXD3	E16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA10, TXD3	H15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA9, RXD4	J16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA8, TXD4	J15	Bidirectional (Optional: Open-drain) (5-V tolerant)

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PC4, $\overline{\text{CD4}}$	L14	Bidirectional (5-V tolerant)
PD15, MII_RXD3	M14	Bidirectional (5-V tolerant)
PD14, MII_RXD2	N16	Bidirectional (5-V tolerant)
PD13, MII_RXD1	K13	Bidirectional (5-V tolerant)
PD12, MII_MDC	N15	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	P16	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	R15	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	N14	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	M13	Bidirectional (5-V tolerant)
PD7, $\overline{\text{RTS3}}$, MII_RX_ER	T15	Bidirectional (5-V tolerant)
PD6, $\overline{\text{RTS4}}$, MII_RX_DV	N13	Bidirectional (5-V tolerant)
PD5, MII_TXD3	R14	Bidirectional (5-V tolerant)
PD4, MII_TXD2	P14	Bidirectional (5-V tolerant)
PD3, MII_TXD1	M12	Bidirectional (5-V tolerant)
TMS	F15	Input (5-V tolerant)
TDI, DSDI	G14	Input (5-V tolerant)
TCK, DSCK	H13	Input (5-V tolerant)
$\overline{\text{TRST}}$	F16	Input (5-V tolerant)
TDO, DSDO	F14	Output (5-V tolerant)
MII_CRS	B6	Input

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PB31, $\overline{\text{SPISEL}}$	F14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	G14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	E16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	J15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	J17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	M17	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	D17	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	F15	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	F16	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	K15	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	L16	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	K14	Bidirectional (5-V tolerant)
PC4, $\overline{\text{CD4}}$	M15	Bidirectional (5-V tolerant)
PD15, MII_RXD3	N15	Bidirectional (5-V tolerant)
PD14, MII_RXD2	P17	Bidirectional (5-V tolerant)
PD13, MII_RXD1	L14	Bidirectional (5-V tolerant)