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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

E·XF

2000	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc852tvr100a

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



1 Overview

The MPC852T is a 0.18-micron derivative of the MPC860 PowerQUICC[™] family, and can operate up to 100 MHz on the MPC8xx core with a 66-MHz external bus. The MPC852T has a 1.8-V core and a 3.3-V I/O operation with 5-V TTL compatibility. The MPC852T integrated communications controller is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in Ethernet control applications, including CPE equipment, Ethernet routers and hubs, VoIP clients, and WiFi access points.

The MPC852T is a PowerPC architecture-based derivative of the MPC860 Quad Integrated Communications Controller (PowerQUICC). The CPU on the MPC852T is a MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches. The MPC852T is the subset of this family of devices.

2 Features

The MPC852T is comprised of three modules that each use a 32-bit internal bus: an MPC8xx core, system integration unit (SIU), and communication processor module (CPM).

The following list summarizes the key MPC852T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
 - 50/66 MHz core frequencies support both 1:1 and 2:1 modes
 - 80/100 MHz core frequencies support 2:1 mode only
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch, without conditional execution.
 - 4-Kbyte data cache and 4-Kbyte instruction cache
 - 4-Kbyte instruction caches is two-way, set-associative with 128 sets
 - 4-Kbyte data cachesis two-way, set-associative with 128 sets
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis
 - MMUs with 32-entry TLB, fully associative instruction, and data TLBs
 - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces, and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or \overline{RAS} to support a DRAM bank



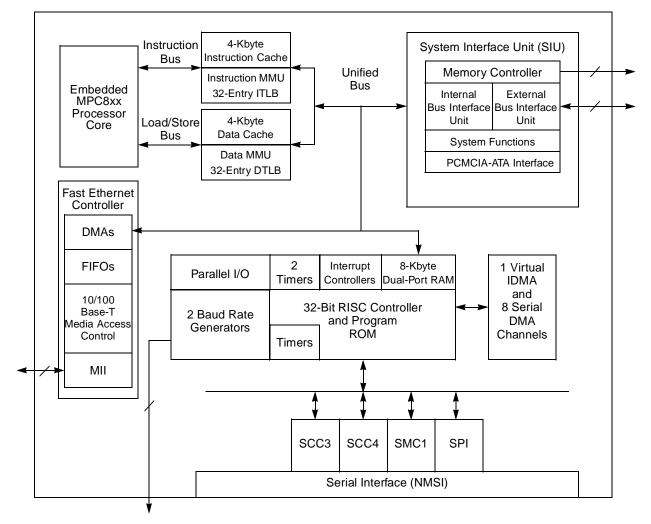


Figure 1. MPC852T Block Diagram



NP

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR should be configured with the mandatory value in Table 6 in the boot code after the reset deasserts.

Register/Configuration	Field	Value (Binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	X1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	X1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[4-7] PAPAR[12-15]	0
PADIR (Port A data direction register)	PADIR[4–7] PADIR[12–15]	1
PBPAR (Port B pin assignment register)	PBPAR[14] PBPAR[16–23] PBPAR[26–27]	0
PBDIR (Port B data direction register)	PBDIR[14] PBDIR[16–23] PBDIR[26–27]	1
PCPAR (Port C pin assignment register)	PCPAR[8–11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8–11] PCDIR[14]	1

Table 6. Mandatory	v Reset	Configuration	of MPC852T
	y neset	ooninguration	01 101 00321

11 Layout Practices

Each V_{DD} pin on the MPC852T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC852T have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized to minimize undershoot and reflections that these fast output switching times cause. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances that the PC traces cause. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads, because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that are inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to the *MPC866 PowerQUICC*TM *Family Reference Manual*, Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN} , V_{SSSYN} , V_{SSSYN1})."



Num	Characteristic	33	MHz	40 1	MHz	50 MHz		66 MHz		Unit
Num		Min	Max	Min	Max	Min	Max	Min	Max	Omit
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	_	6.00		6.00	—	6.00	—	ns
B16a	TEA, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	_	4.50	_	4.50	_	4.50	_	ns
B16b	$\overline{BB}, \overline{BG}, \overline{BR}, \text{ valid to CLKOUT (setup time)}$ ³ (4MIN = 0.00 × B1 +.000)	4.00	_	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (hold time) (MIN = $0.00 \times B1 + 1.00^4$)	1.00	_	1.00	_	1.00	_	2.00	_	ns
B17a	CLKOUT to \overline{KR} , \overline{RETRY} , \overline{CR} valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	_	2.00		2.00	—	2.00	_	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) ⁵ (MIN = $0.00 \times B1 + 6.00$)	6.00	_	6.00		6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) ⁵ (MIN = $0.00 \times B1 + 1.00^{6}$)	1.00	_	1.00	_	1.00	—	2.00	_	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) ⁷ (MIN = $0.00 \times B1 + 4.00$)	4.00	_	4.00	_	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) ⁷ (MIN = $0.00 \times B1 + 2.00$)	2.00	_	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00)	—	8.00	_	8.00	_	8.00	_	8.00	ns
B22b	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 0 (MIN = $0.25 \times B1 - 2.00$)	5.60		4.30		3.00		1.80	_	ns

Table 9. Bus Operation Timings (continued)



Nivues	Characteristic	33 I	ИНz	40 M	ИНz	50 MHz		66 MHz		l lm it
Num	Characteristic	Min	Мах	Min	Мах	Min	Max	Min	Max	Unit
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 and CSNT = 0 (MIN = 0.25 × B1 - 2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns
B29c	$\label{eq:constraint} \hline \hline \hline CS \ negated to \ D(0:31), \ DP(0:3) \ High-Z \\ GPCM \ write \ access, \ TRLX = 0, \ CSNT = 1, \\ ACS = 10, \ or \ ACS = 11 \ EBDF = 0 \\ (MIN = 0.50 \times B1 - 2.00) \\ \hline \hline$	13.20	_	10.50	_	8.00	_	5.60	_	ns
B29d	$ \frac{\overline{WE}(0:3)/BS_B[0:3] \text{ negated to } D(0:31), \\ DP(0:3) \text{ High-Z GPCM write access, TRLX} \\ = 1, CSNT = 1, EBDF = 0 \\ (MIN = 1.50 \times B1 - 2.00) $	43.50	_	35.50	_	28.00	_	20.70	_	ns
B29e	\overline{CS} negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 × B1 - 2.00)	43.50	_	35.50	_	28.00	_	20.70	_	ns
B29f	$\label{eq:weighted} \hline \hline WE(0:3/BS_B[0:3]) \ \text{negated to } D(0:31), \\ DP(0:3) \ \text{High Z GPCM write access}, \\ TRLX = 0, \ CSNT = 1, \ EBDF = 1 \\ (MIN = 0.375 \times B1 - 6.30)^8 \\ \hline \hline \hline \\ \hline \\ $	5.00	_	3.00	_	1.10	_	0.00	_	ns
B29g	$\frac{\overline{\text{CS}} \text{ negated to D}(0:31), \text{ DP}(0:3) \text{ High-Z}}{\text{GPCM write access, TRLX = 0, CSNT = 1}}$ $\text{ACS = 10 \text{ or ACS = 11, EBDF = 1}}$ $(\text{MIN = 0.375 \times \text{B1} - 6.30)^8}$	5.00	_	3.00	_	1.10	—	0.00	_	ns
B29h	$\label{eq:weighted} \hline \hline WE(0:3)/BS_B[0:3] \mbox{ negated to } D(0:31), \\ DP(0:3) \mbox{ High Z GPCM write access,} \\ TRLX = 1, \mbox{ CSNT = 1, EBDF = 1} \\ (MIN = 0.375 \times B1 - 3.30) \\ \hline \hline \hline \end{tabular}$	38.40	_	31.10	_	24.20	_	17.50	_	ns
B29i	$\label{eq:cs} \hline \hline CS \ \text{negated to } D(0:31), \ DP(0:3) \ \text{High-Z} \\ GPCM \ \text{write access, } TRLX = 1, \ CSNT = 1, \\ ACS = 10 \ \text{or } ACS = 11, \ EBDF = 1 \\ (MIN = 0.375 \times B1 - 3.30) \\ \hline \hline \end{tabular}$	38.40	_	31.10	_	24.20	_	17.50	_	ns
B30	\overline{CS} , \overline{WE} (0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) Invalid GPCM write access ⁹ (MIN = 0.25 × B1 – 2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns
B30a	$eq:weighted_$	13.20		10.50		8.00		5.60		ns

Table 9. Bus Operation Timings (continued)



Figure 4 is the control timing diagram.

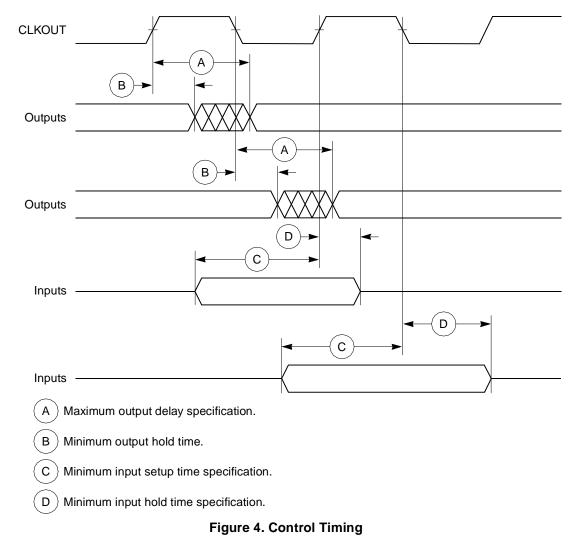


Figure 5 provides the timing for the external clock.

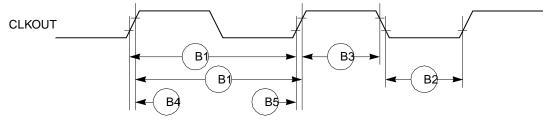


Figure 5. External Clock Timing



Figure 8 provides the timing for the synchronous input signals.

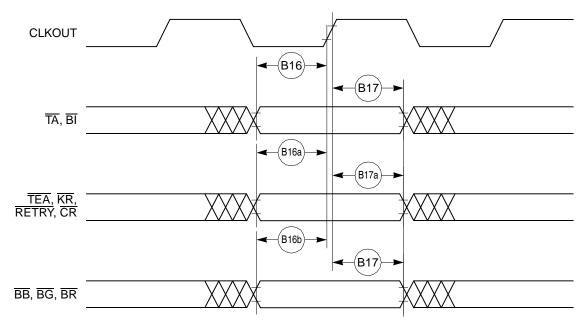


Figure 8. Synchronous Input Signals Timing

Figure 9 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

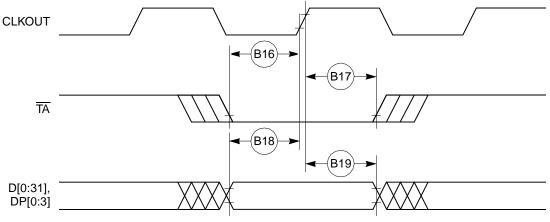


Figure 9. Input Data Timing in Normal Case



Figure 10 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

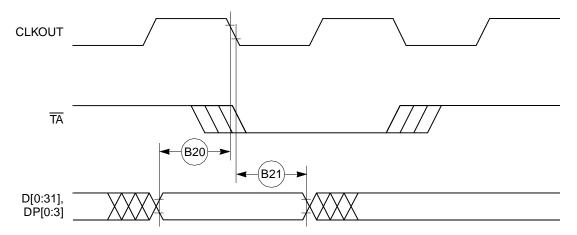


Figure 10. Input Data Timing When Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 11 through Figure 14 provide the timing for the external bus read that various GPCM factors control.

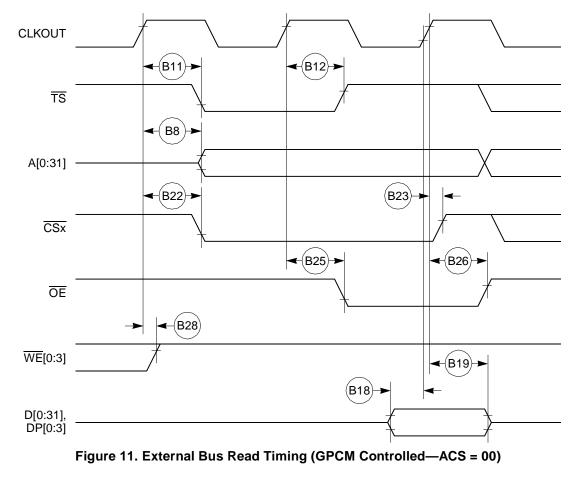




Figure 19 provides the timing for the asynchronous asserted UPWAIT signal that the UPM controls.

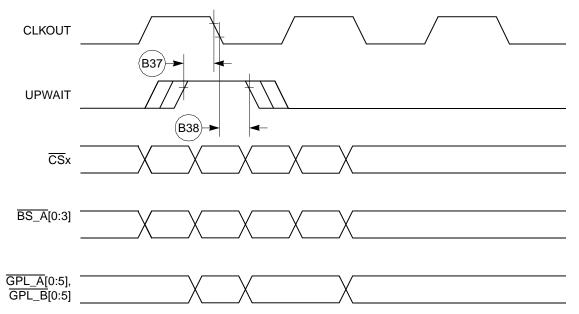


Figure 19. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 20 provides the timing for the asynchronous negated UPWAIT signal that the UPM controls.

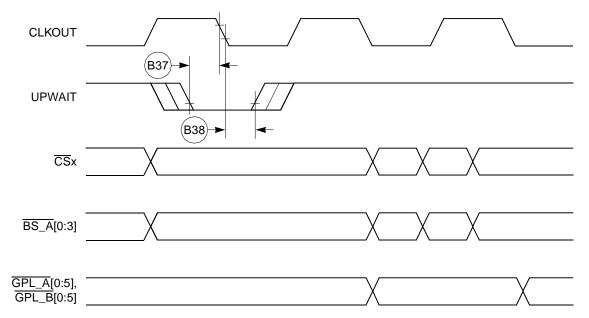


Figure 20. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing



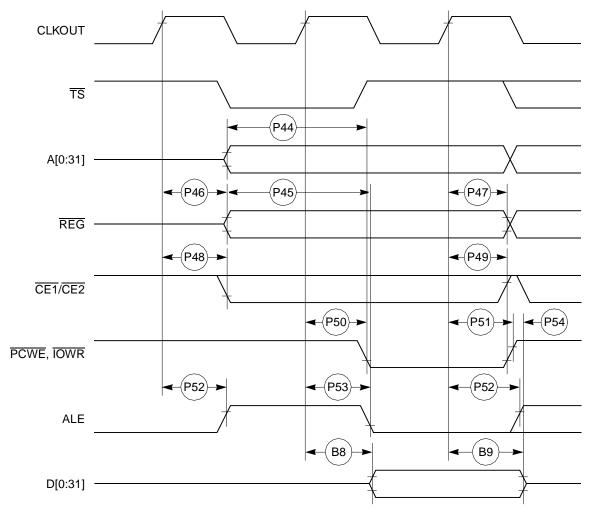


Figure 27 provides the PCMCIA access cycle timing for the external bus write.

Figure 27. PCMCIA Access Cycles Timing External Bus Write

Figure 28 provides the PCMCIA \overline{WAIT} signals detection timing.

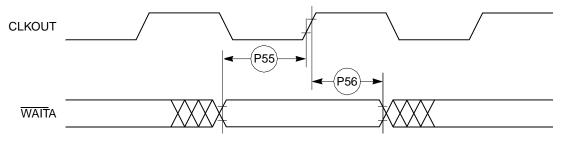


Figure 28. PCMCIA WAIT Signals Detection Timing



IEEE 1149.1 Electrical Specifications

Figure 35 provides the reset timing for the debug port configuration.

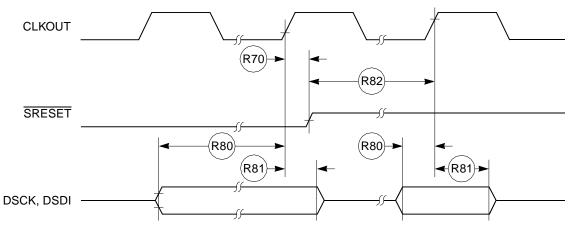


Figure 35. Reset Timing—Debug Port Configuration

13 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC852T shown in Figure 36 through Figure 39.

Num	Characteristic	All Freq	uencies	Unit
Num	Min		Мах	Unit
J82	TCK cycle time	100.00		ns
J83	TCK clock pulse width measured at 1.5 V	40.00	_	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	_	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	_	20.00	ns
J90	TRST assert time	100.00	—	ns
J91	TRST setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

Table	15.	JTAG	Timing
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CPM Electrical Characteristics

14 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC852T.

14.1 Port C Interrupt AC Electrical Specifications

Table 16 provides the timings for port C interrupts.

Table 16. Port C Interrupt Timing

Num	Characteristic	33.34	Unit	
Num		Min	Мах	Onit
35	Port C interrupt pulse width low (edge-triggered mode)	55	_	ns
36	Port C interrupt minimum time between active edges	55	_	ns

Figure 40 shows the port C interrupt detection timing.

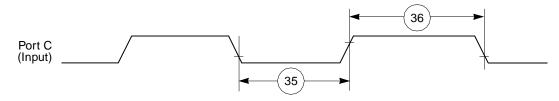


Figure 40. Port C Interrupt Detection Timing



CPM Electrical Characteristics

SPI Master AC Electrical Specifications 14.7

Table 23 provides the SPI master timings as shown in Figure 55 and Figure 56.

Table 23. SPI Master Timing

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Unit
160	MASTER cycle time	4	1024	t _{cyc}
161	MASTER clock (SCK) high or low time	2	512	t _{cyc}
162	MASTER data setup time (inputs)	15	_	ns
163	Master data hold time (inputs)	0	_	ns
164	Master data valid (after SCK edge)	_	10	ns
165	Master data hold time (outputs)	0	_	ns
166	Rise time output	—	15	ns
167	Fall time output	_	15	ns

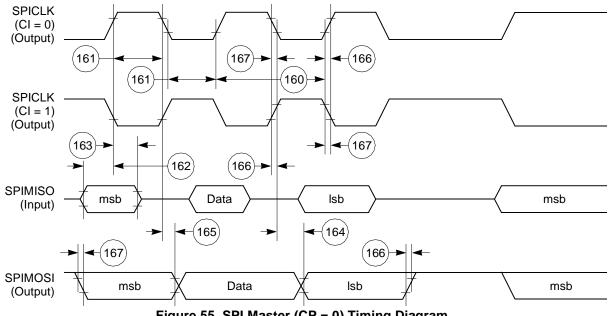


Figure 55. SPI Master (CP = 0) Timing Diagram



15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

15.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency –1%.

Table 25 provides information on the MII receive signal timing.

Num	Characteristic	Min	Мах	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Table 25. MII Receive Signal Timing

Figure 59 shows MII receive signal timing.

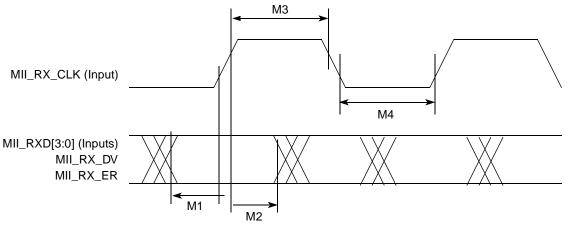


Figure 59. MII Receive Signal Timing Diagram

15.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency -1%.



FEC Electrical Characteristics

Table 26 provides information about the MII transmit signal timing,.

Num	Characteristic	Min	Мах	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	—
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Table 26. MII Transmit Signal Timing

Figure 60 shows the MII transmit signal timing diagram.

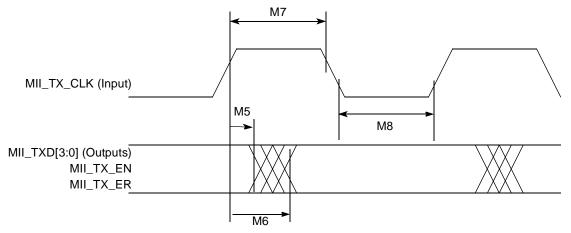


Figure 60. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 27 provides information about the MII async inputs signal timing.

Table 27. MII Async Inputs Signal Timing

Num	Characteristic	Min	Мах	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5		MII_TX_CLK period

Figure 61 shows the MII asynchronous inputs signal timing diagram.

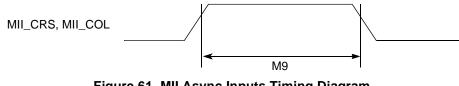


Figure 61. MII Async Inputs Timing Diagram



16.1.1 JEDEC Compliant Pinout

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC*TM *Family Reference Manual*.

 $\bigcup_{\mathsf{CS7}} \ \bigcup_{\mathsf{GPL}_\mathsf{A2}} \ \bigcup_{\mathsf{WE2}} \ \bigcup_{\mathsf{BS}_\mathsf{A0}} \ \bigcup_{\mathsf{VDDL}}$ O A19 O A18 O A23 O A14 O A7 O A1 O N/C O_{CS1} O A28 O A2 А O N/C $\underset{A0}{O}$ O A30 O A29 O A27 O A13 0 A9 O N/C $\frac{O}{CS0}$ OCE2_A OD WE3 MILCRS OD A3 O A22 O A6 В O A8 O A21 $O_{\overline{CS3}}$ O CS5 O A26 Ο Ο Ο Ο Ο Ο С A25 A17 A12 A3 N/C PC15 O PB29 O A20 O A4 $\frac{O}{CS6}$ O A31 OBI $\frac{O}{CS2}$ $\bigcup_{WE0} \bigcup_{BS_A1}$ Ο Ο Ο Ο Ο OE D A24 A15 A10 N/C VDDL O TSIZ0 O PC12 \bigcup_{TS} O GPL_A5 O CE_1A O TSIZ1 O A16 O A11 O A5 O PB31 O PA11 \bigcup_{BR} O_{TFA} O_{CS4} O N/C O PC13 Е O CR MIL_COL O TMS \bigcup_{BB} O_{TA} Ο Ο Ο Ο Ο Ο Ο Ο \bigcirc O TDO Ο F PB30 TRST VFLS_1 RSV OBURST O VDDL O O MDIO Ο Ο Ο Ο Ο Ο Ο Ο Ο G PB28 ALE_A DSCK VFLS_0 O FR7 Ο Ο Ο Ο О O PB25 O PA10 Ο Ο Ο Ο O PB24 н GND O BADDR30 O HRESET Ο Ο Ο Ο Ο Ο Ο Ο Ο Ο $O_{\overline{KR}}$ Ο Ο J PC7 PC5 PA8 PA9 O OP1 Ο OP2 RSTCONF Ο Ο Ο Ο Ο Ο Ο Ο O PD13 O PA2 O PC6 О κ OP0 VDDH O PC4 O PA1 O PB15 \bigcirc Ο Ο С Ο Ο Ο Ο Ο Ο Ο Ο O N/C L **OP3BADDR29 BADDR28** VDDL O D26 O D14 O D9 O IRQ1 O PD3 O PD8 O PD15 Ο Μ PÃ0 O D10 KTAL EXTCLK WAIT_A VSSSYN IP_A5 CLKOUT O D25 O D21 O D15 O D17 O IRQ7 O PD6 O PD9 O PD12 O PD14 Ν Ο Ο O D29 O D24 O D20 O D16 O D11 O D23 O D12 O PD4 O N/C O PD11 Р Ο Ο Ο Ο Ο Ο Ο Ο Ο Ο Ο Ο \bigcirc О \bigcirc С R IP_A2 VDDL IP_A7 D19 D13 D0 PD5 PD10 DP3 D31 D28 D6 D5 D2 D27 N/C O IP_A0 O IP_A4 O DP2 O_{D30} Ω O_{D22} O_{D18} \sum_{3} P $O_{N/C}$ B MILTXEN PD7 т UNC N/C \bigcup_{D4} 3 4 5 6 7 8 11 12 13 1 2 9 10 14 15 16 Figure 63. Pinout of PBGA Package—JEDEC Standard

NOTE: This is the top view of the device.



Name	Pin Number	Туре
MII_MDIO	G16	Bidirectional (5-V tolerant)
MII_TXEN	T14	Output (5-V tolerant)
MII_COL	F2	Input
V _{SSSYN}	N4	PLL analog GND
V _{SSSYN1}	P3	PLL analog GND
V _{DDSYN}	P2	PLL analog V _{DD}
GND	G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11	Power
V _{DDL}	A7, C1, D16, G15, L4, M2, R1, M15, T8	Power
V _{DDH}	F5, F6, F7, F8, F9, F10, F11, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L8, L9, L10, L11, L12	Power
N/C	A1, A16, B16, C15, D14, E12, L13, M4, P15, R16, T1, T16	No connect

Table 30. Pin Assignments—JEDEC Standard (continued)



Name	Pin Number	Туре
PD12, MII_MDC	P16	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	R17	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	T16	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	P15	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	N14	Bidirectional (5-V tolerant)
PD7, RTS3, MII_RX_ER	U16	Bidirectional (5-V tolerant)
PD6, RTS4, MII_RX_DV	P14	Bidirectional (5-V tolerant)
PD5, MII_TXD3	T15	Bidirectional (5-V tolerant)
PD4, MII_TXD2	R15	Bidirectional (5-V tolerant)
PD3, MII_TXD1	N13	Bidirectional (5-V tolerant)
TMS	G16	Input (5-V tolerant)
TDI, DSDI	H15	Input (5-V tolerant)
TCK, DSCK	J14	Input (5-V tolerant)
TRST	G17	Input (5-V tolerant)
TDO, DSDO	G15	Output (5-V tolerant)
MII_CRS	C7	Input
MII_MDIO	H17	Bidirectional (5-V tolerant)
MII_TX_EN	U15	Output (5-V tolerant)
MII_COL	G3	Input
V _{SSSYN}	P5	PLL analog GND

Table 31. Pin Assignments—Non-JEDEC (continued)



Mechanical Data and Ordering Information

Name	Pin Number	Туре
V _{SSSYN1}	R4	PLL analog GND
V _{DDSYN}	R3	PLL analog V _{DD}
GND	H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, L12	Power
V _{DDL}	B8, D2, E17, H16, M5, N3, T2, N16, U9	Power
V _{DDH}	G6, G7, G8, G9, G10, G11, G12, G13, H6, H13, J6, J13, K6, K13, L6, L13, M6, M7, M8, M9, M10, M11, M12, M13	Power
N/C	B2, B17, C17, D16, E15, F13, M14, N5, R16, T17, U2, U17	No connect

Table 31. Pin Assignments—Non-JEDEC (continued)

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