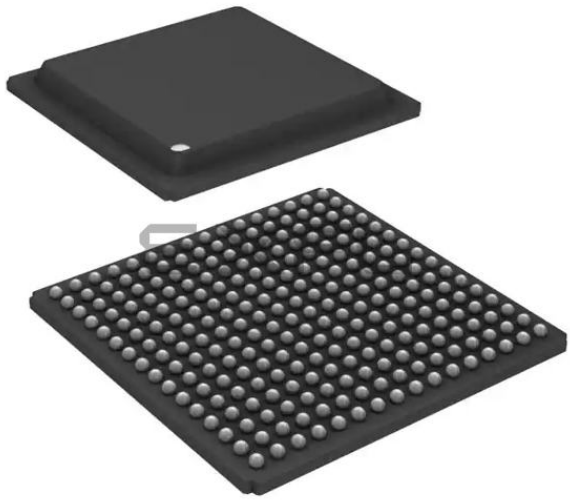

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc852tvr66a

1 Overview

The MPC852T is a 0.18-micron derivative of the MPC860 PowerQUICC™ family, and can operate up to 100 MHz on the MPC8xx core with a 66-MHz external bus. The MPC852T has a 1.8-V core and a 3.3-V I/O operation with 5-V TTL compatibility. The MPC852T integrated communications controller is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in Ethernet control applications, including CPE equipment, Ethernet routers and hubs, VoIP clients, and WiFi access points.

The MPC852T is a PowerPC architecture-based derivative of the MPC860 Quad Integrated Communications Controller (PowerQUICC). The CPU on the MPC852T is a MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches. The MPC852T is the subset of this family of devices.

2 Features

The MPC852T is comprised of three modules that each use a 32-bit internal bus: an MPC8xx core, system integration unit (SIU), and communication processor module (CPM).

The following list summarizes the key MPC852T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - 50/66 MHz core frequencies support both 1:1 and 2:1 modes
  - 80/100 MHz core frequencies support 2:1 mode only
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - 4-Kbyte instruction caches is two-way, set-associative with 128 sets
    - 4-Kbyte data cachesis two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis
  - MMUs with 32-entry TLB, fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces, and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) [3] (4MIN = 0.00 × B1 +.000)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = 0.00 × B1 + 1.00[4])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time)[5] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time)[5] (MIN = 0.00 × B1 + 1.00[6])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time)[7] (MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time)[7] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0,1 CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Figure 8 provides the timing for the synchronous input signals.

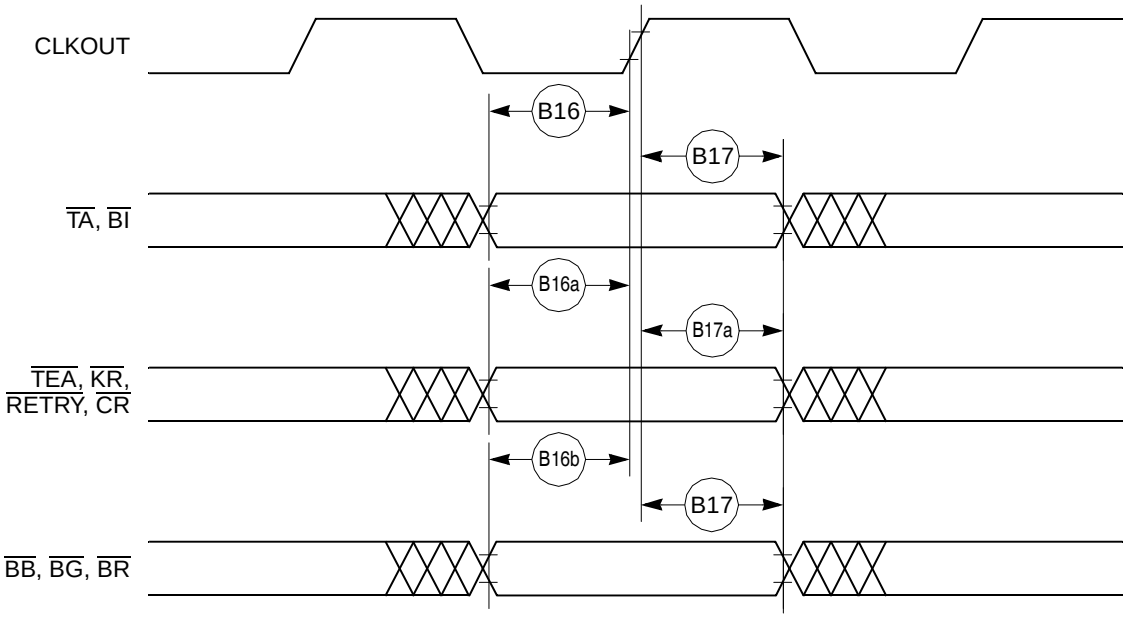

Figure 8. Synchronous Input Signals Timing

Figure 9 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

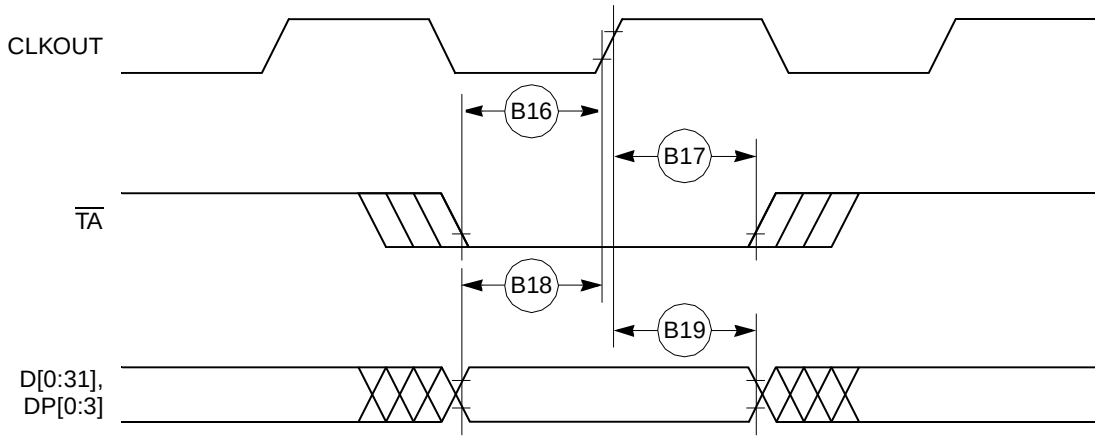

Figure 9. Input Data Timing in Normal Case

Figure 10 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

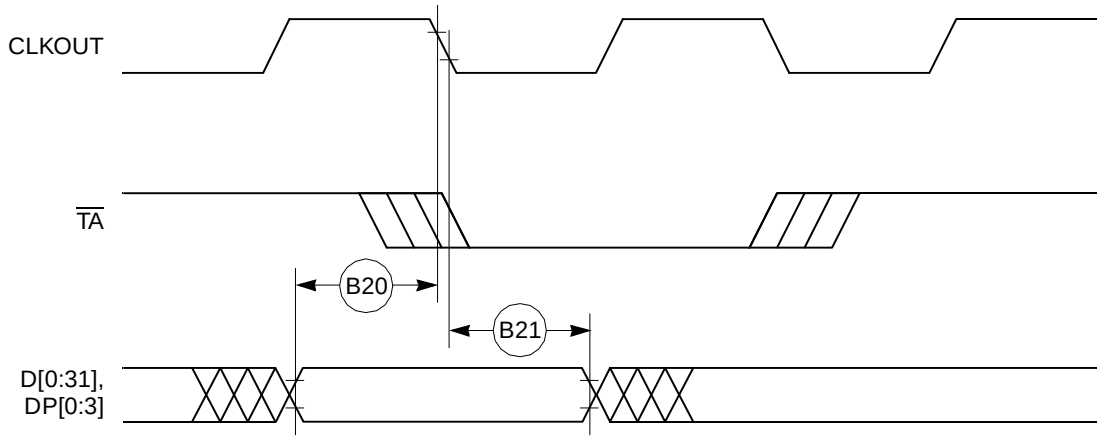

Figure 10. Input Data Timing When Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 11 through Figure 14 provide the timing for the external bus read that various GPCM factors control.

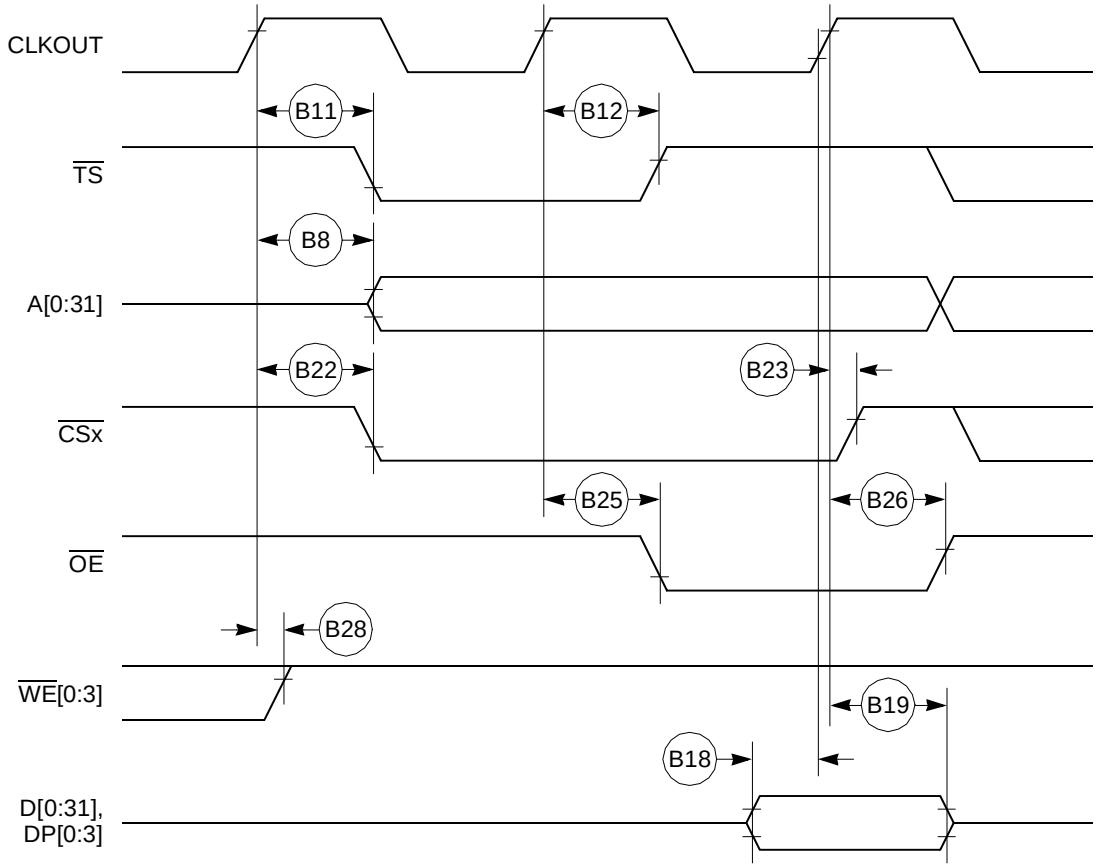

Figure 11. External Bus Read Timing (GPCM Controlled—ACS = 00)

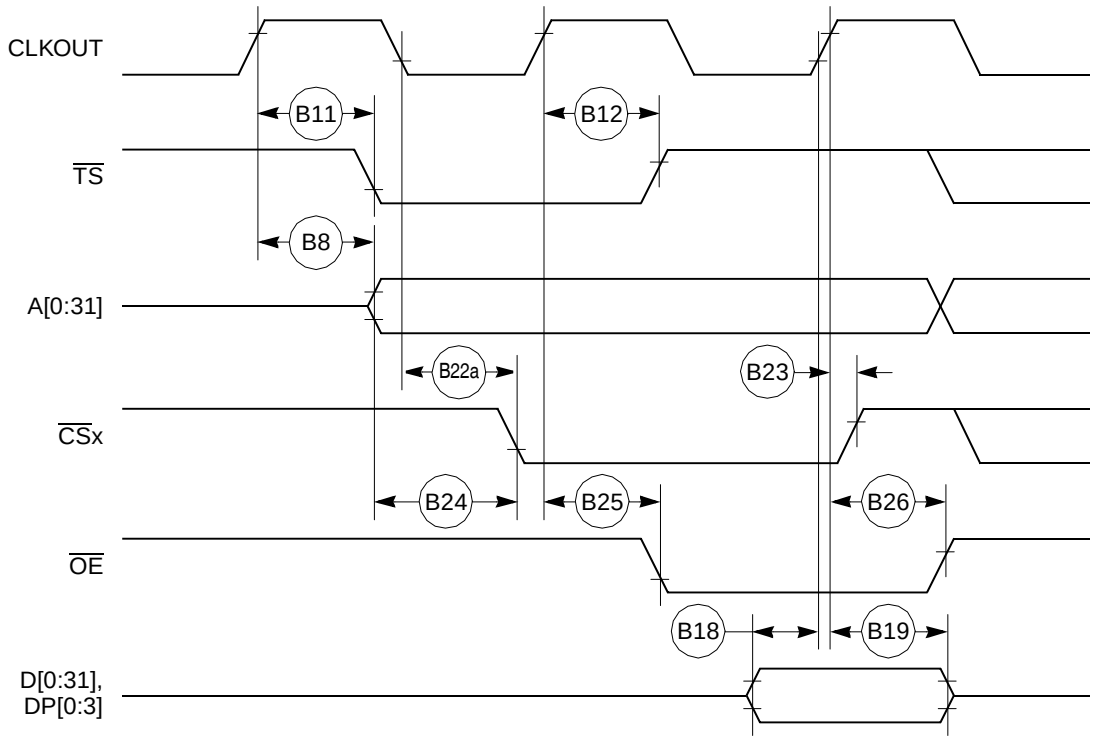

Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

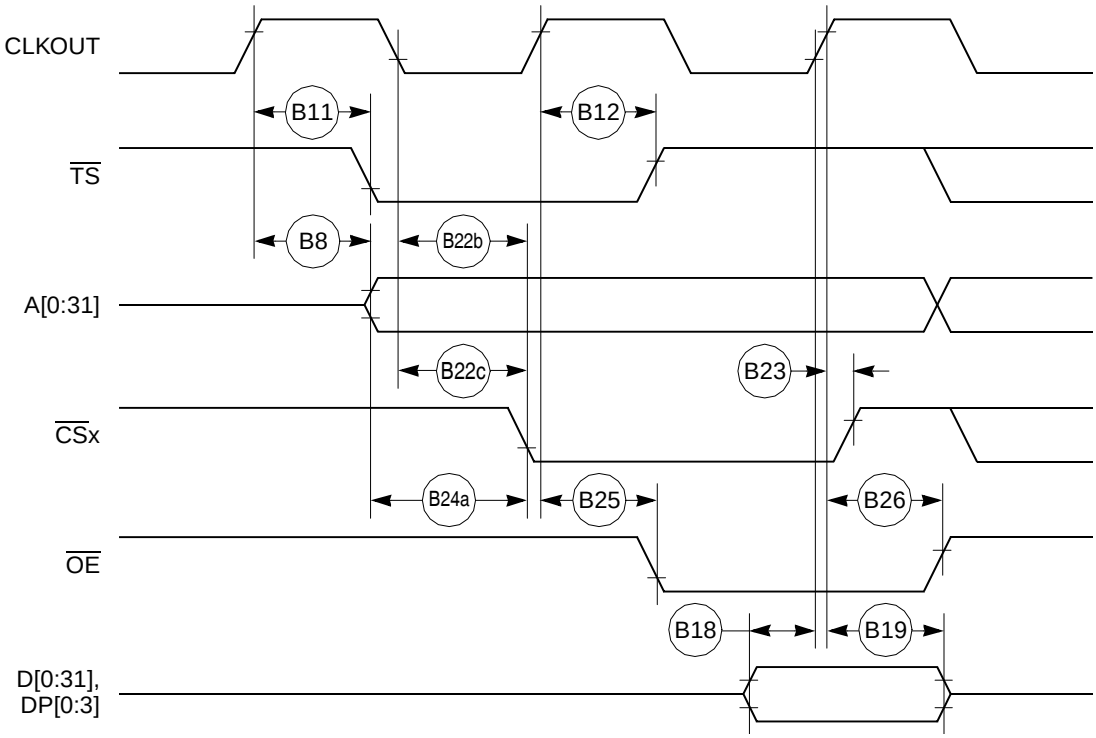

Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

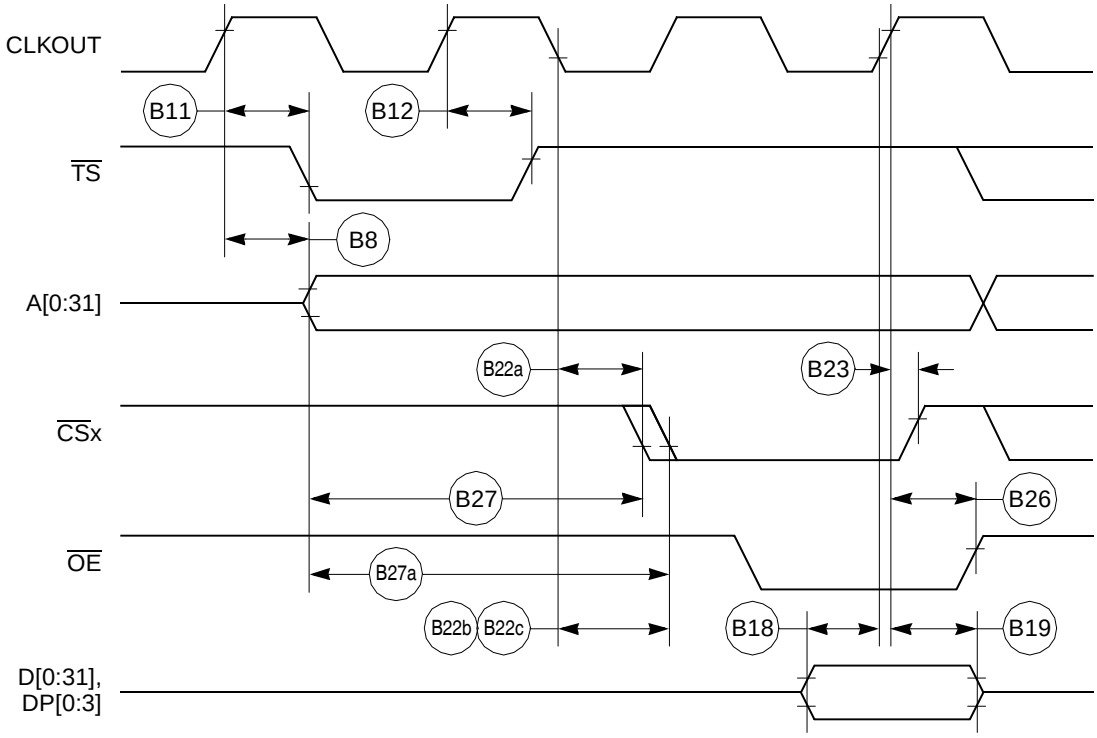

Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Figure 18 provides the timing for the external bus that the UPM controls.

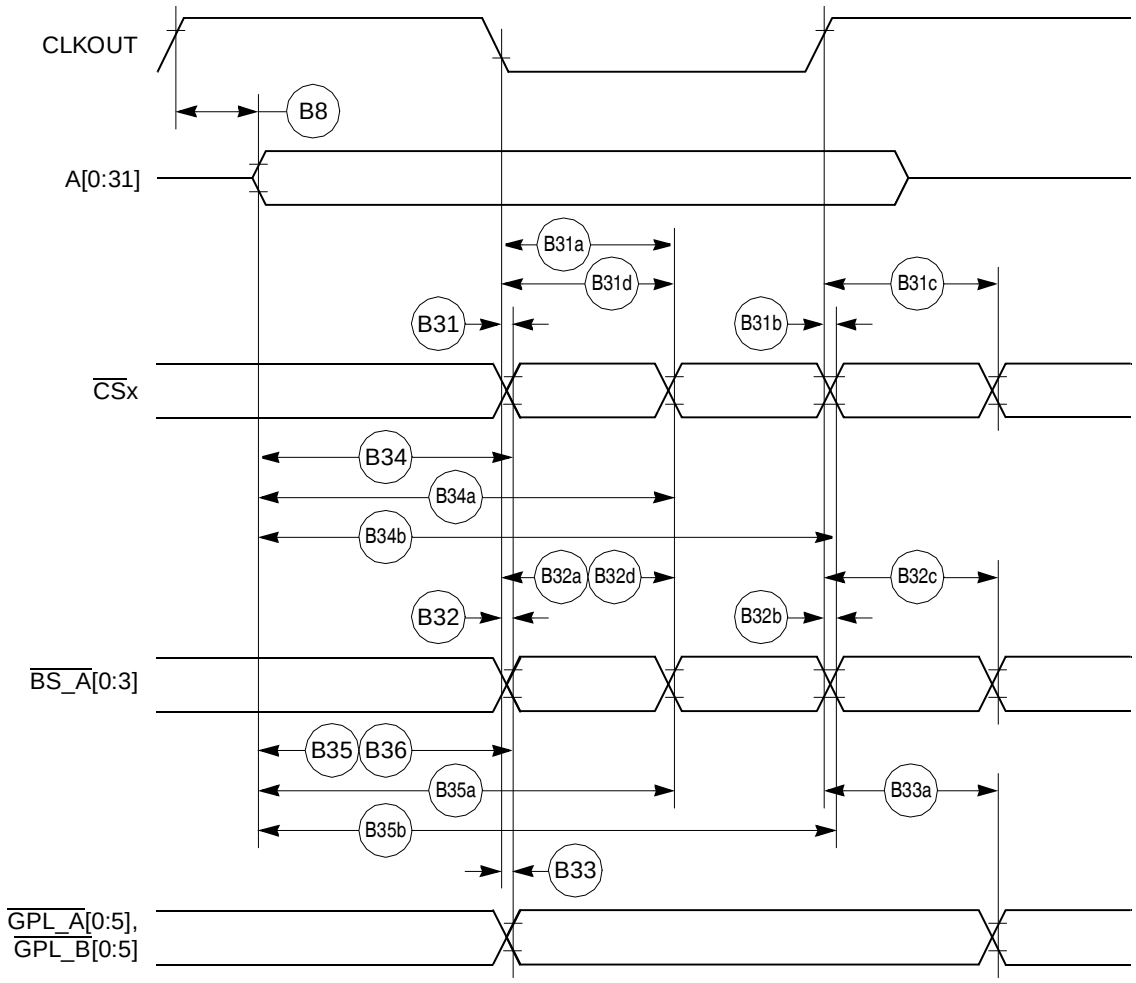

Figure 18. External Bus Timing (UPM Controlled Signals)

Figure 26 provides the PCMCIA access cycle timing for the external bus read.

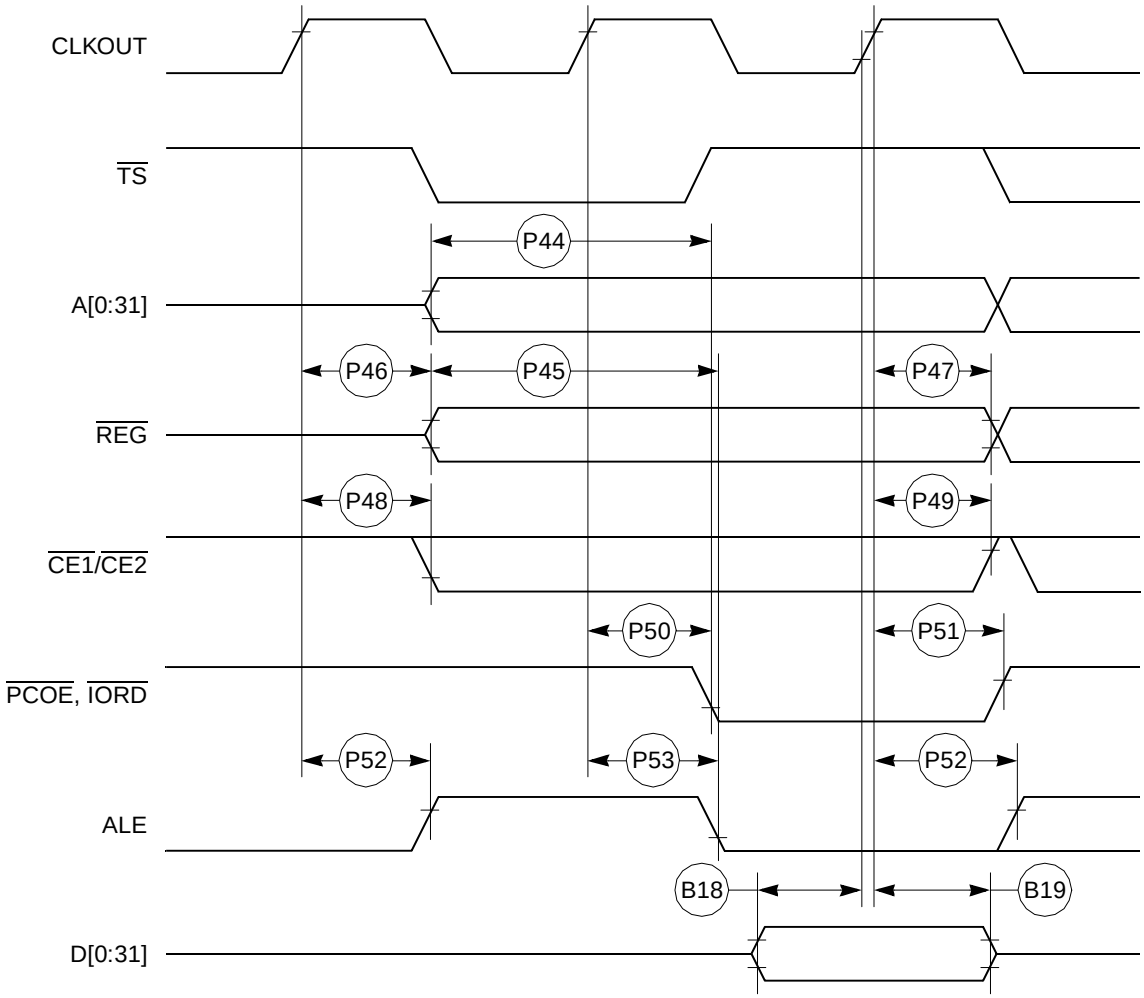

Figure 26. PCMCIA Access Cycles Timing External Bus Read

Table 12 shows the PCMCIA port timing for the MPC852T.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J95	CLKOUT to OPx Valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
J96	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	18.00	—	14.40	—	ns
J97	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
J98	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 29 provides the PCMCIA output port timing for the MPC852T.

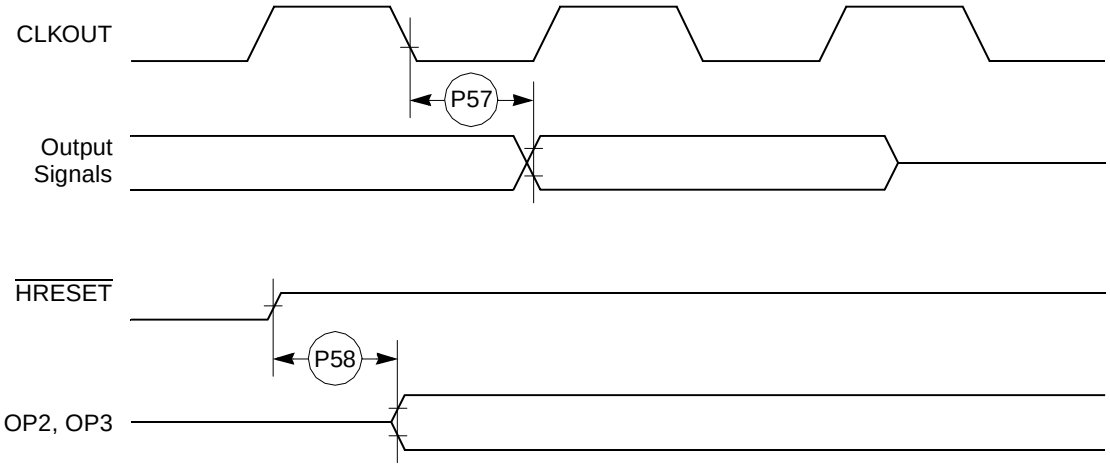

Figure 29. PCMCIA Output Port Timing

Figure 30 provides the PCMCIA output port timing for the MPC852T.

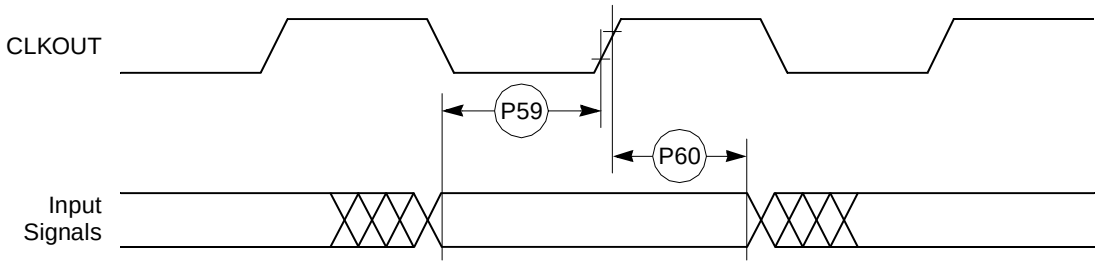

Figure 30. PCMCIA Input Port Timing

Table 14 shows the reset timing for the MPC852T.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J82	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J83	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J84	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
J85	—	—	—	—	—	—	—	—	—	—
J86	Configuration data to HRESET rising edge set up time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
J87	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
J88	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J89	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J90	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J91	$\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J92	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J93	DSDI, DSCK set up (MIN = 3.00 × B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
J94	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J95	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

Figure 33 shows the reset timing for the data bus configuration.

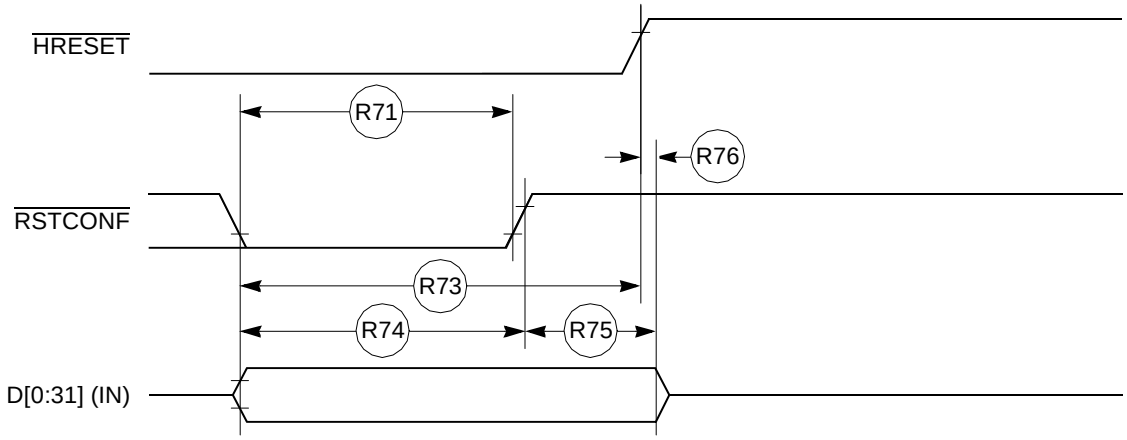

Figure 33. Reset Timing—Configuration from Data Bus

Figure 34 provides the reset timing for the data bus weak drive during configuration.

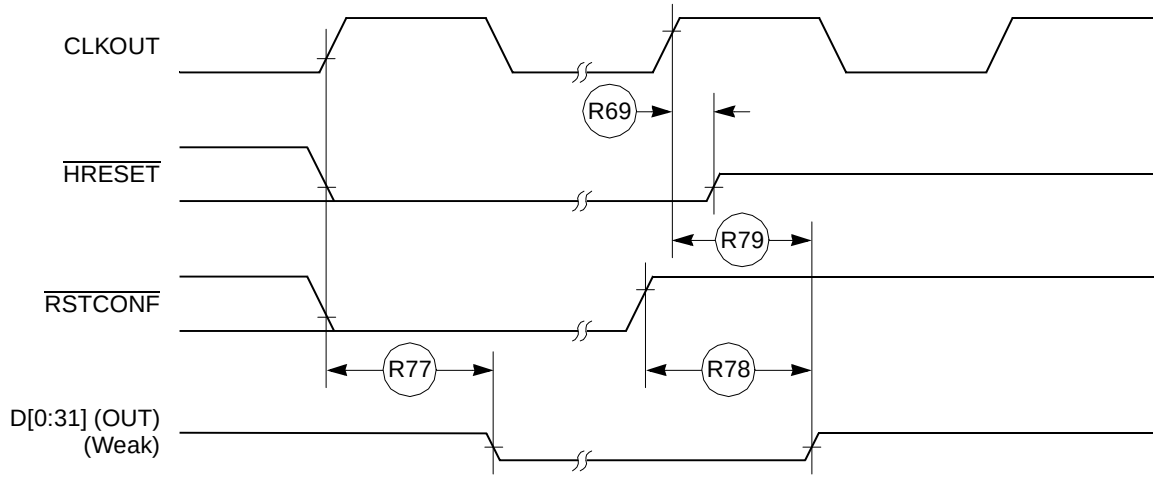

Figure 34. Reset Timing—Data Bus Weak Drive During Configuration

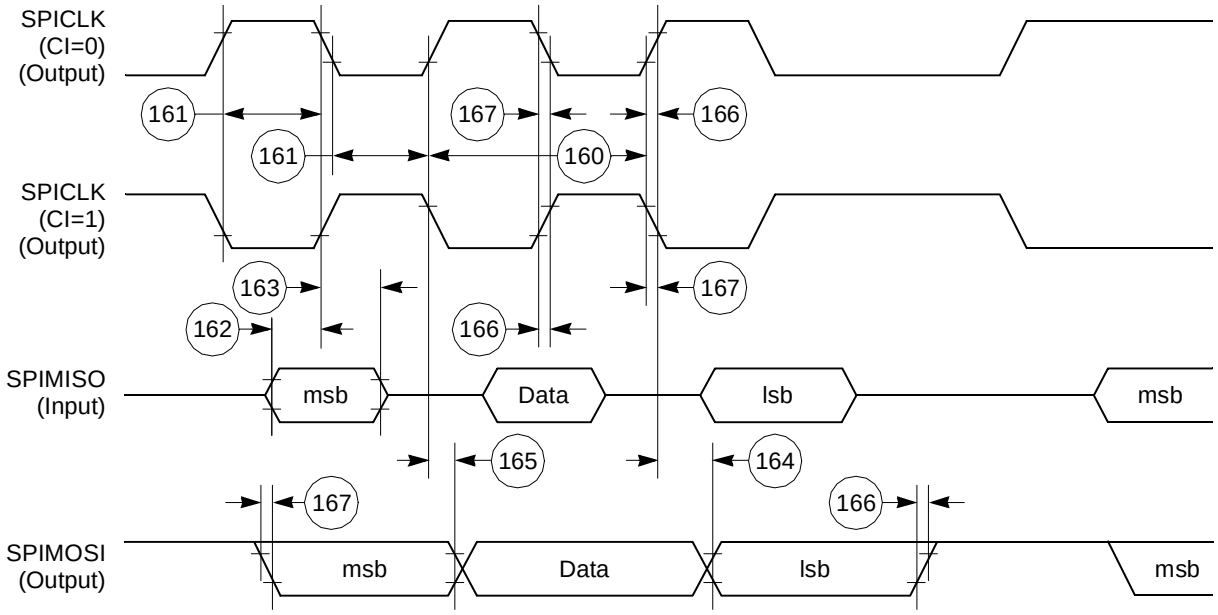

Figure 56. SPI Master (CP = 1) Timing Diagram

14.8 SPI Slave AC Electrical Specifications

Table 24 provides the SPI slave timings as shown in Figure 57 and Figure 58.

Table 24. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

Table 26 provides information about the MII transmit signal timing,.

Table 26. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	—
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 60 shows the MII transmit signal timing diagram.

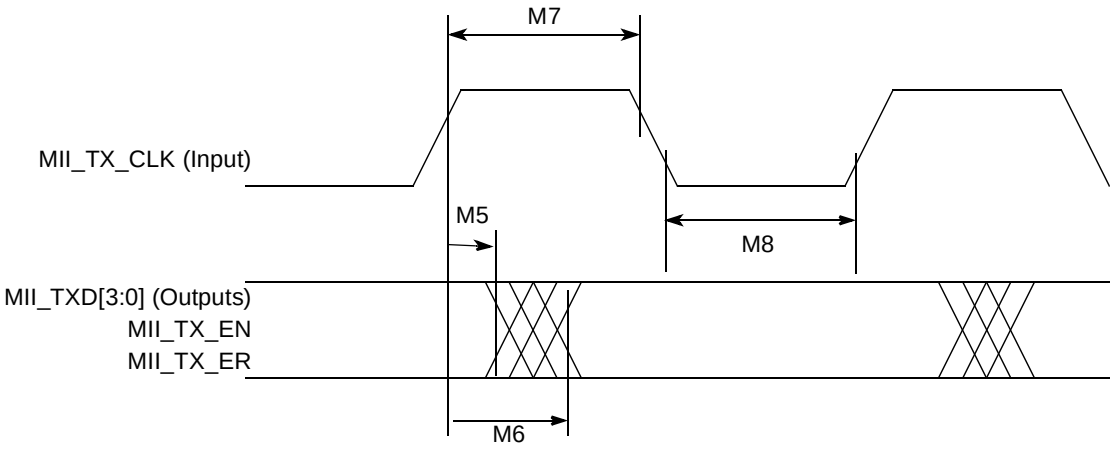

Figure 60. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 27 provides information about the MII async inputs signal timing.

Table 27. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 61 shows the MII asynchronous inputs signal timing diagram.

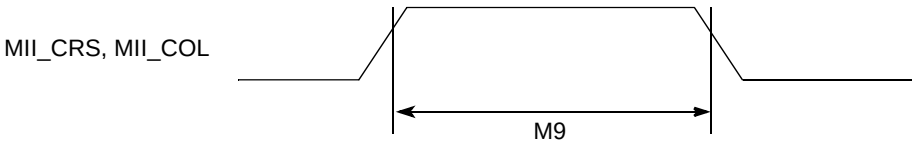

Figure 61. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 28 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 28. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 62 shows the MII serial management channel timing diagram.

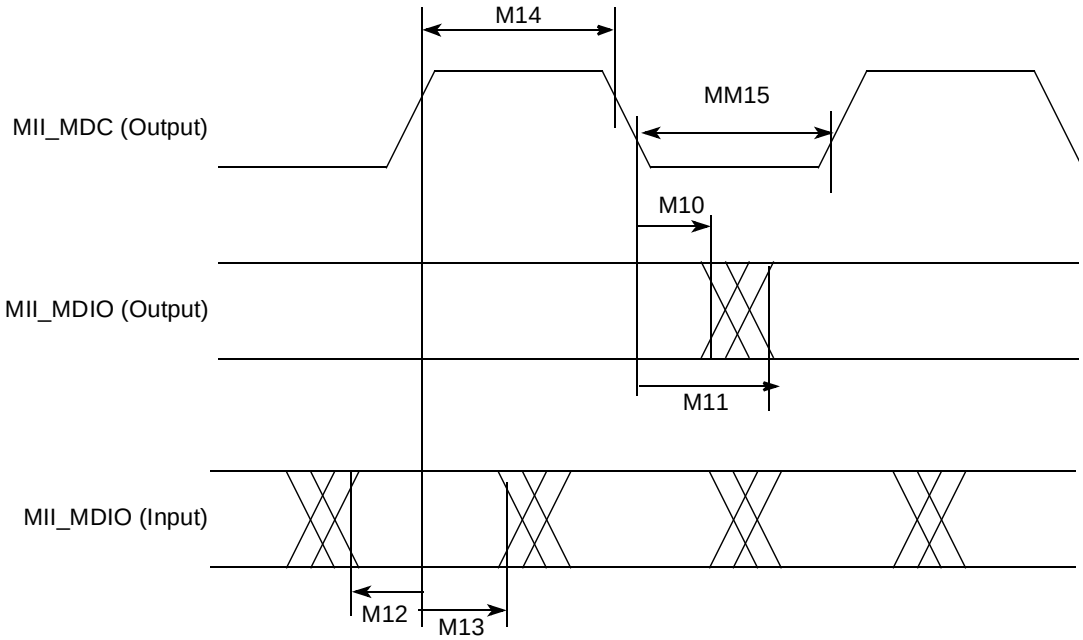

Figure 62. MII Serial Management Channel Timing Diagram

Table 30 contains a list of the MPC852T input and output signals and shows multiplexing and pin assignments.

Table 30. Pin Assignments—JEDEC Standard

Name	Pin Number	Type
A[0:31]	B15, A15, A14, C14, D13, E11, B14, A13, C13, B13, D12, E10, C12, B12, A12, D11, E9, C11, A9, A11, D10, C10, B8, A10, D9, C9, C8, B11, A8, B10, B9, D8	Bidirectional Three-state (3.3 V only)
TSIZ0, $\overline{\text{REG}}$	E8	Bidirectional Three-state (3.3 V only)
TSIZ1	E7	Bidirectional Three-state (3.3 V only)
RD/$\overline{\text{WR}}$	B1	Bidirectional Three-state (3.3 V only)
$\overline{\text{BURST}}$	G3	Bidirectional Three-state (3.3 V only)
$\overline{\text{BDIP}}$, $\overline{\text{GPL\_B5}}$	D1	Output
$\overline{\text{TS}}$	E2	Bidirectional Active Pull-up (3.3 V only)
$\overline{\text{TA}}$	F4	Bidirectional Active Pull-up (3.3 V only)
$\overline{\text{TEA}}$	E3	Open-drain
$\overline{\text{BI}}$	D2	Bidirectional Active Pull-up (3.3 V only)
$\overline{\text{IRQ2}}$ $\overline{\text{RSV}}$	G2	Bidirectional Three-state (3.3 V only)
$\overline{\text{IRQ4}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, SPKROUT	J1	Bidirectional Three-state (3.3 V only)
$\overline{\text{CR}}$, $\overline{\text{IRQ3}}$	F1	Input (3.3 V only)
D[0:31]	R13, T11, R10, T10, T12, R9, R7, T6, T13, M10, N10, P10, P12, R12, M9, N9, P9, N11, T9, R8, P8, N8, T7, P11, P7, N7, M8, R11, R6, P6, T5, R5	Bidirectional Three-state (3.3 V only)
DP0, $\overline{\text{IRQ3}}$	P4	Bidirectional Three-state (3.3 V only)
DP1, $\overline{\text{IRQ4}}$	P5	Bidirectional Three-state (3.3 V only)
DP2, $\overline{\text{IRQ5}}$	T4	Bidirectional Three-state (3.3 V only)
DP3, $\overline{\text{IRQ6}}$	R4	Bidirectional Three-state (3.3 V only)
$\overline{\text{BR}}$	E1	Bidirectional (3.3 V only)
$\overline{\text{BG}}$	G4	Bidirectional (3.3 V only)
$\overline{\text{BB}}$	F3	Bidirectional Active pull-up (3.3 V only)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
$\overline{BB}$	G4	Bidirectional Active Pull-up (3.3 V only)
FRZ, $\overline{IRQ6}$	J5	Bidirectional (3.3 V only)
$\overline{IRQ0}$	R14	Input (3.3 V only)
$\overline{IRQ1}$	N12	Input (3.3 V only)
$\overline{IRQ7}$, M_TX_CLK	P13	Input (3.3 V only)
$\overline{CS}$[0:5]	C3, B3, E4, D4, F7, D5	Output
$\overline{CS6}$	E5	Output
$\overline{CS7}$	B4	Output
$\overline{WE0}$, BS_B0, $\overline{IORD}$	E7	Output
$\overline{WE1}$, BS_B1, $\overline{IOWR}$	D7	Output
$\overline{WE2}$, BS_B2, $\overline{PCOE}$	B6	Output
$\overline{WE3}$, BS_B3, $\overline{PCWE}$	C6	Output
$\overline{BS\_A}$[0:3]	B7, E8, D8, C8	Output
$\overline{GPL\_A0}$, $\overline{GPL\_B0}$	D6	Output
$\overline{OE}$, $\overline{GPL\_A1}$, $\overline{GPL\_B1}$	E6	Output
$\overline{GPL\_A}$[2:3], $\overline{GPL\_B}$[2:3], $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA, $\overline{GPL\_A4}$	D3	Bidirectional (3.3 V only)
$\overline{GPL\_A5}$	F5	Output
$\overline{PORESET}$	R2	Input (3.3 V only)
$\overline{RSTCONF}$	L5	Input (3.3 V only)
$\overline{HRESET}$	K5	Open-drain
$\overline{SRESET}$	N4	Open-drain
XTAL	P2	Analog output
EXTAL	N2	Analog input (3.3 V only)
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{CE1\_A}$	F6	Output
$\overline{CE2\_A}$	C4	Output
$\overline{WAIT\_A}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PD12, MII_MDC	P16	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	R17	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	T16	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	P15	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	N14	Bidirectional (5-V tolerant)
PD7, $\overline{\text{RTS3}}$, MII_RX_ER	U16	Bidirectional (5-V tolerant)
PD6, $\overline{\text{RTS4}}$, MII_RX_DV	P14	Bidirectional (5-V tolerant)
PD5, MII_TXD3	T15	Bidirectional (5-V tolerant)
PD4, MII_TXD2	R15	Bidirectional (5-V tolerant)
PD3, MII_TXD1	N13	Bidirectional (5-V tolerant)
TMS	G16	Input (5-V tolerant)
TDI, DSDI	H15	Input (5-V tolerant)
TCK, DSCK	J14	Input (5-V tolerant)
$\overline{\text{TRST}}$	G17	Input (5-V tolerant)
TDO, DSDO	G15	Output (5-V tolerant)
MII_CRS	C7	Input
MII_MDIO	H17	Bidirectional (5-V tolerant)
MII_TX_EN	U15	Output (5-V tolerant)
MII_COL	G3	Input
V_{SSSYN}	P5	PLL analog GND

17 Document Revision History

Table 32 lists significant changes between revisions of this document.

Table 32. Document Revision History

Revision	Date	Changes
4		• Updated template. • On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 2) and renumbered the rest of the figures. • In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 4, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 17, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..." • In Figure 42, changed $\overline{TA}$ to reflect the rising edge of the clock.
3.1	1/18/2005	Document template update.
3.0	11/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values • Added a footnote to Spec 41 specifying that EDM = 1 • Broke the Section 16.1, "Pin Assignments," into 2 smaller sections for the JEDEC and non-JEDEC pinouts.
2.0	12/2003	Put 852T on the 1st page in place of 8245. Figure 62 on page 59 had overbars added on signals CR (pin G2) and WAIT_A (pin P4).
1.8	7/2003	Changed the pinout to be JEDEC Compliant, changed timing parameters B28a through B28d, and B29d to show that TRLX can be 0 or 1.
1.7	5/2003	Changed the SPI Master Timing Specs. 162 and 164
1.6	4/2003	Changed the package drawing in Figure 15-63
1.5	4/2003	Changed 5 Port C pins with interrupt capability to 7 Port C pins. Added the Note: solder sphere composition for MPC852TVR and MPC852TCVR devices is 95.5%Sn 45%Ag 0.5%Cu to Figure 15-63
1.4	2/2003	Changed Table 15-30 Pin Assignments for the PLL Pins V_{SSSYN1}, V_{SSSYN}, V_{DDSYN}
1.3	1/2003	Added subscripts to timing diagrams for B1-B35, to specify memory controller settings for the specific edges.
1.2	1/2003	In Table 15-30, specified EXTCLK as 3.3 V.
1.1	12/2002	Added fast Ethernet controller to the features
1	11/2002	Added values for 80 and 100 MHz
0	10/2002	Initial release

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