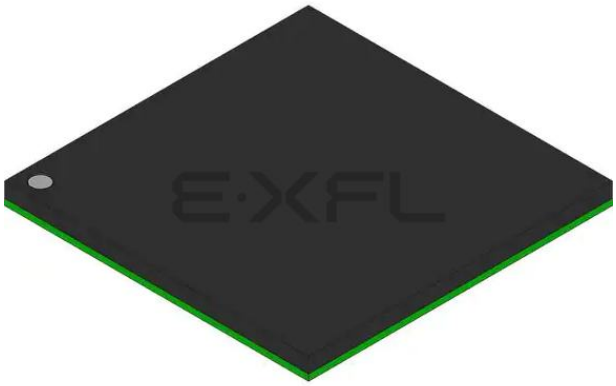

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc852tzt100a

1 Overview

The MPC852T is a 0.18-micron derivative of the MPC860 PowerQUICC™ family, and can operate up to 100 MHz on the MPC8xx core with a 66-MHz external bus. The MPC852T has a 1.8-V core and a 3.3-V I/O operation with 5-V TTL compatibility. The MPC852T integrated communications controller is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in Ethernet control applications, including CPE equipment, Ethernet routers and hubs, VoIP clients, and WiFi access points.

The MPC852T is a PowerPC architecture-based derivative of the MPC860 Quad Integrated Communications Controller (PowerQUICC). The CPU on the MPC852T is a MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches. The MPC852T is the subset of this family of devices.

2 Features

The MPC852T is comprised of three modules that each use a 32-bit internal bus: an MPC8xx core, system integration unit (SIU), and communication processor module (CPM).

The following list summarizes the key MPC852T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - 50/66 MHz core frequencies support both 1:1 and 2:1 modes
  - 80/100 MHz core frequencies support 2:1 mode only
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - 4-Kbyte instruction caches is two-way, set-associative with 128 sets
    - 4-Kbyte data cachesis two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis
  - MMUs with 32-entry TLB, fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces, and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank

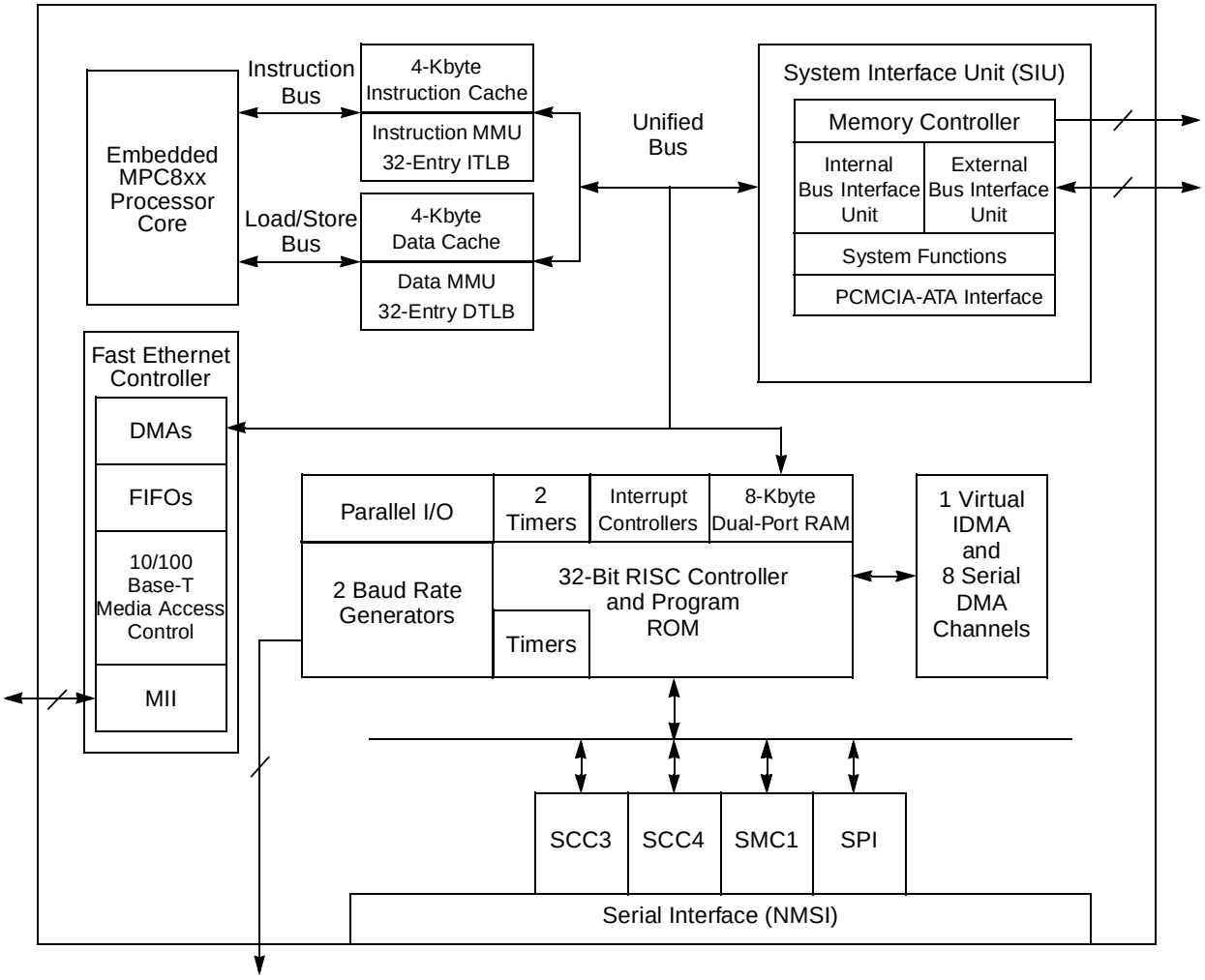


Figure 1. MPC852T Block Diagram

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ Valid[3] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	9.80	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30[2])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B37	UPWAIT valid to CLKOUT falling edge[10] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[10] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[11] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the maximum allowed jitter on EXTAL can be up to 2%.

2 For part speeds above 50MHz, use 9.80ns for B11a.

3 The timing required for $\overline{BR}$ input is relevant when the MPC852T is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC852T is selected to work with external bus arbiter.

4 For part speeds above 50MHz, use 2ns for B17.

5 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

6 For part speeds above 50MHz, use 2ns for B19.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 This formula applies to bus operation up to 50 MHz.

9 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

10 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 19.

11 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 22.

Figure 4 is the control timing diagram.

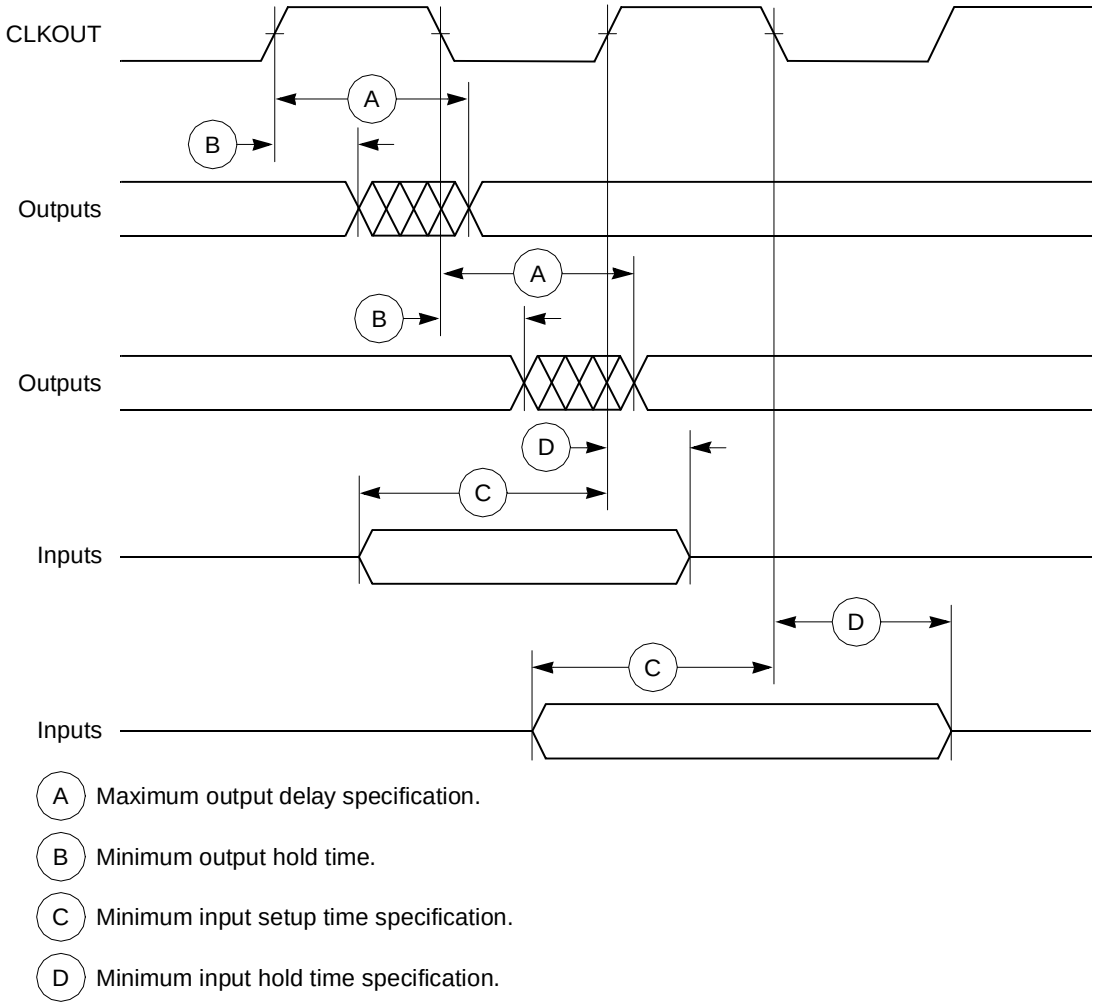


Figure 4. Control Timing

Figure 5 provides the timing for the external clock.

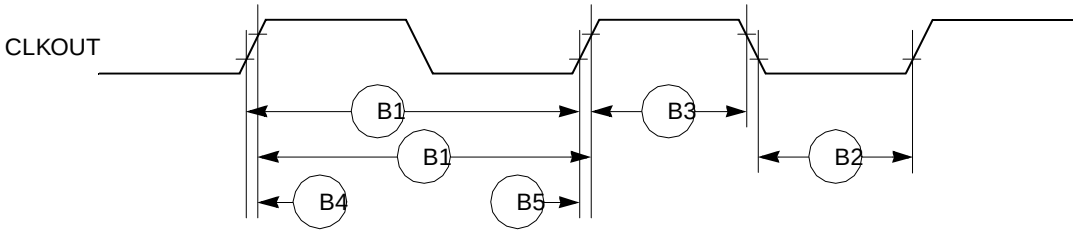


Figure 5. External Clock Timing

Figure 10 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

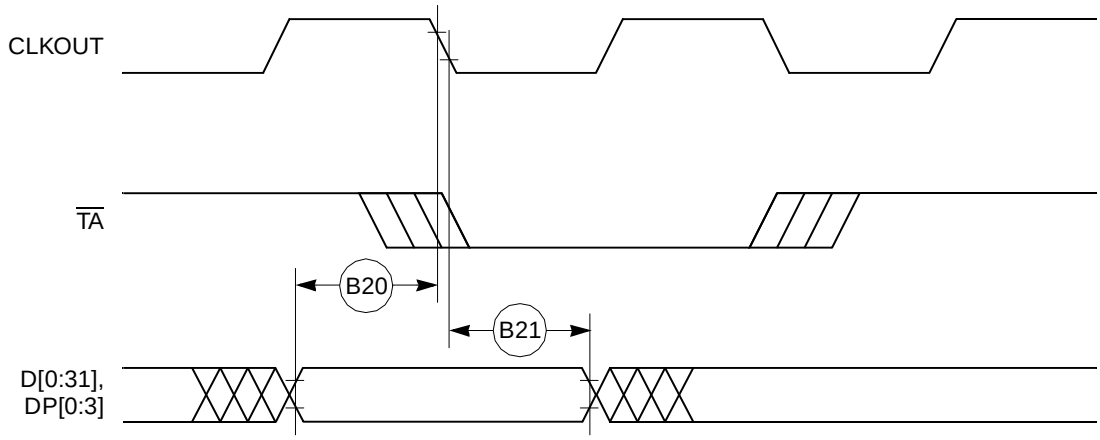


Figure 10. Input Data Timing When Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 11 through Figure 14 provide the timing for the external bus read that various GPCM factors control.

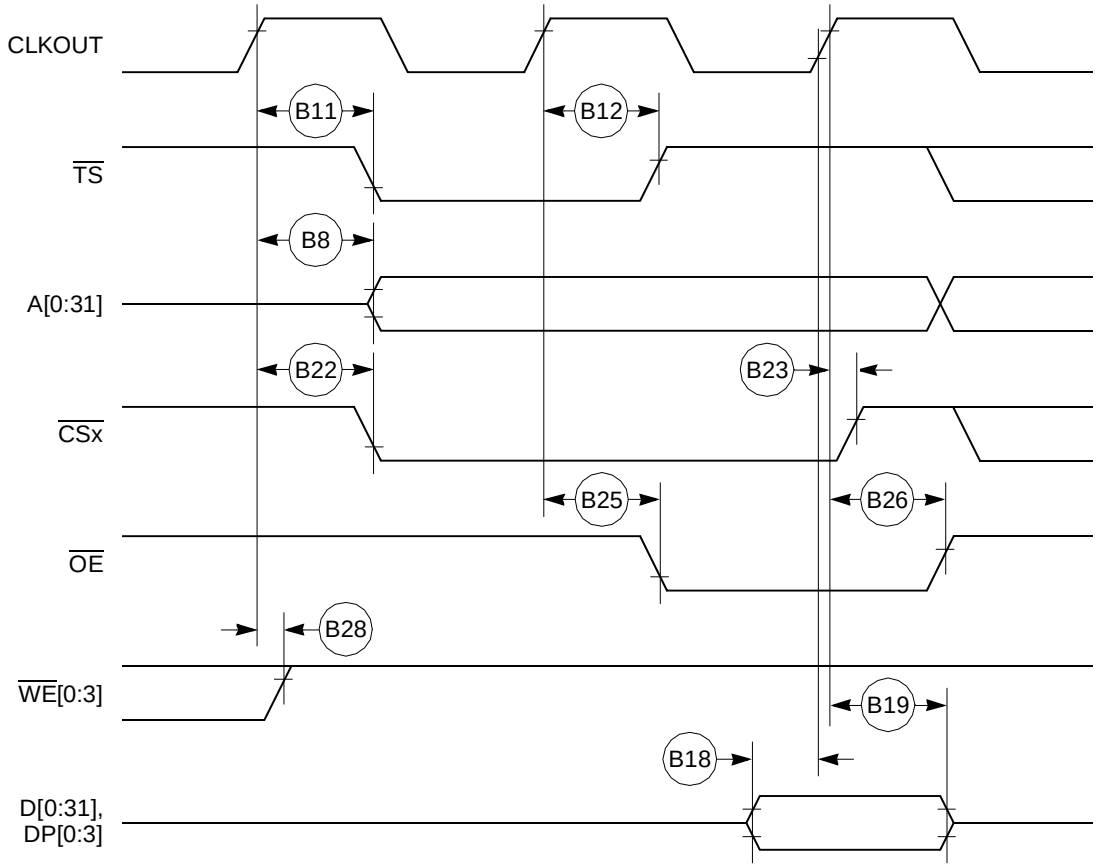


Figure 11. External Bus Read Timing (GPCM Controlled—ACS = 00)

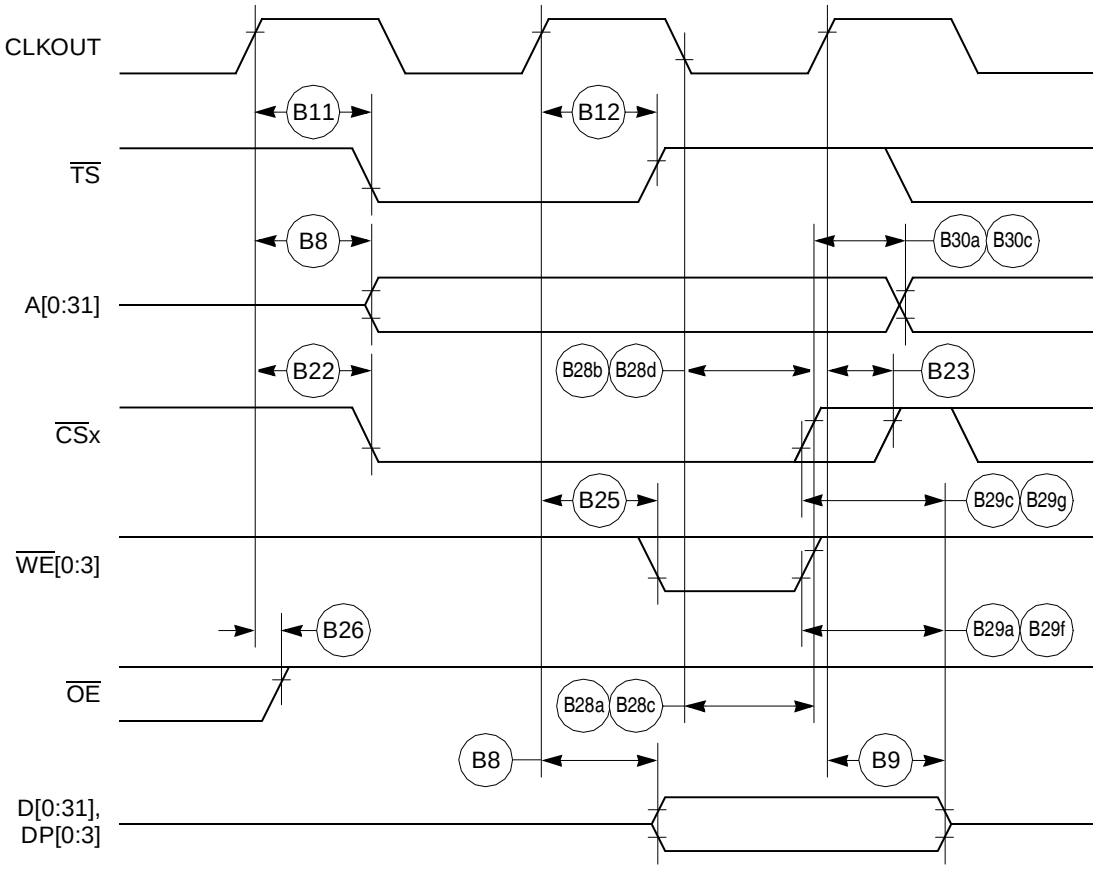


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Table 10 provides interrupt timing for the MPC852T.

Table 10. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (set up time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

1 The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and need not be asserted or negated with reference to the CLKOUT. The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and have no direct relation with the total system interrupt latency that the MPC852T is able to support.

Figure 24 provides the interrupt detection timing for the external level-sensitive lines.

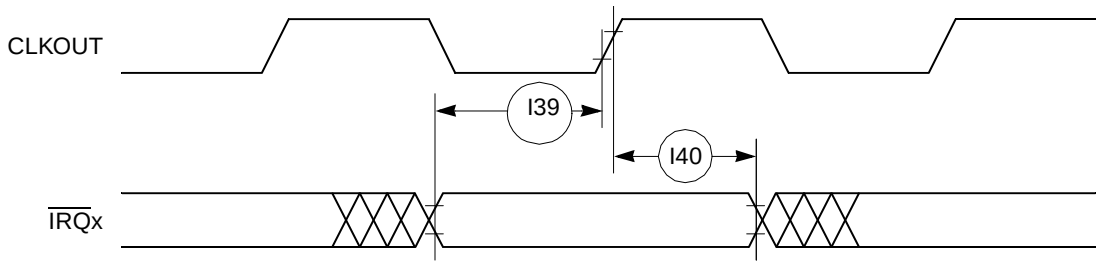


Figure 24. Interrupt Detection Timing for External Level Sensitive Lines

Figure 25 provides the interrupt detection timing for the external edge-sensitive lines.

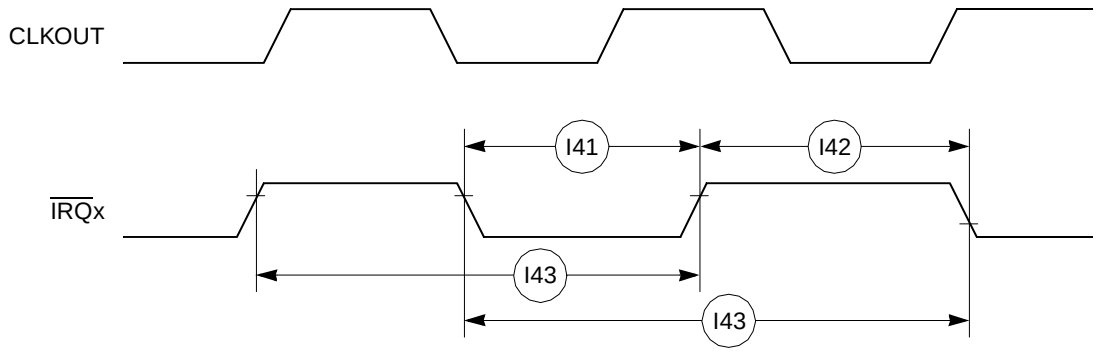


Figure 25. Interrupt Detection Timing for External Edge Sensitive Lines

Figure 26 provides the PCMCIA access cycle timing for the external bus read.

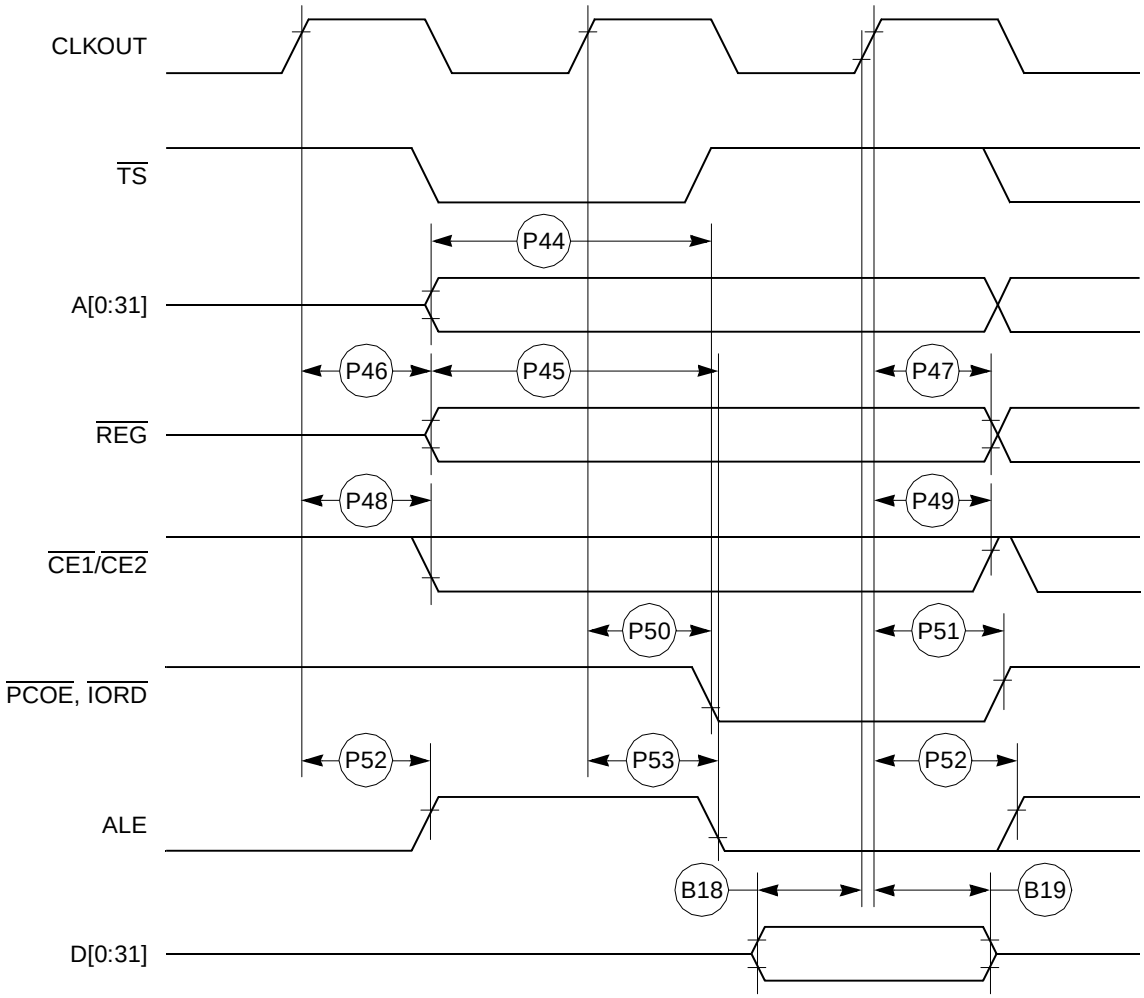


Figure 26. PCMCIA Access Cycles Timing External Bus Read

14.2 IDMA Controller AC Electrical Specifications

Table 17 provides the IDMA controller timings as shown in Figure 41 through Figure 44.

Table 17. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high [1]	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

1 Applies to high-to-low mode (EDM = 1).

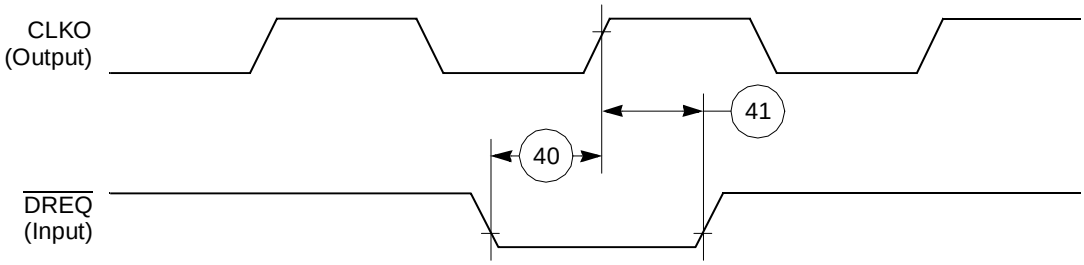


Figure 41. IDMA External Requests Timing Diagram

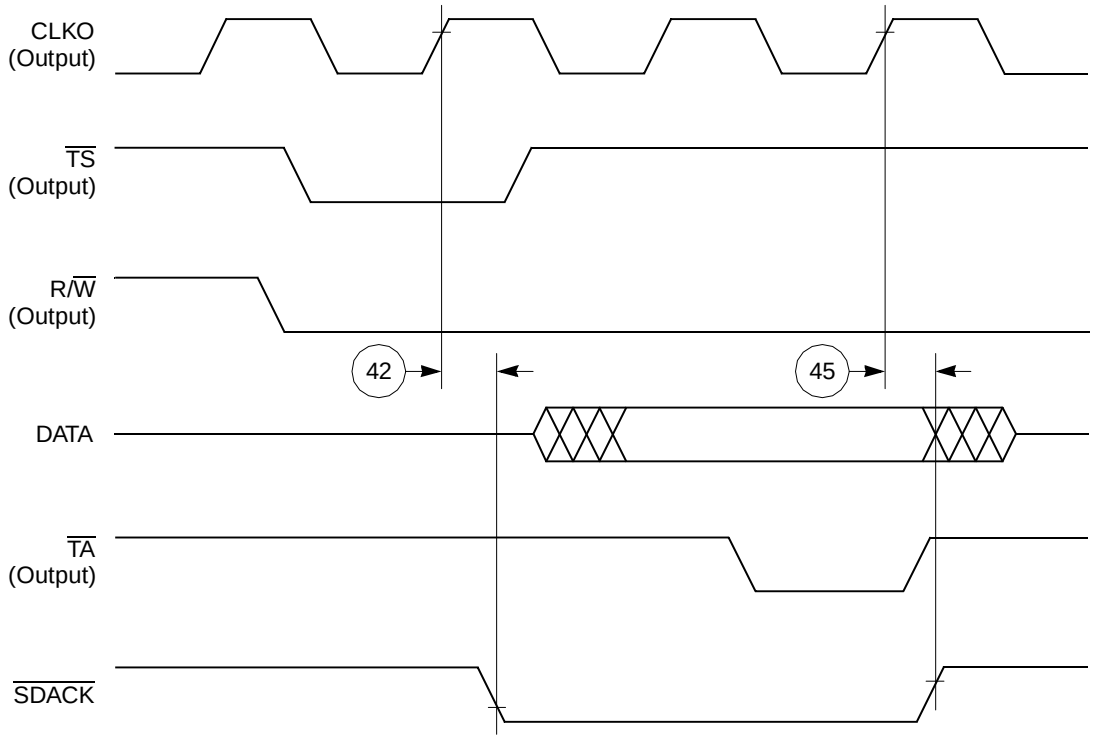


Figure 44. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

14.3 Baud Rate Generator AC Electrical Specifications

Table 18 provides the baud rate generator timings as shown in Figure 45.

Table 18. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

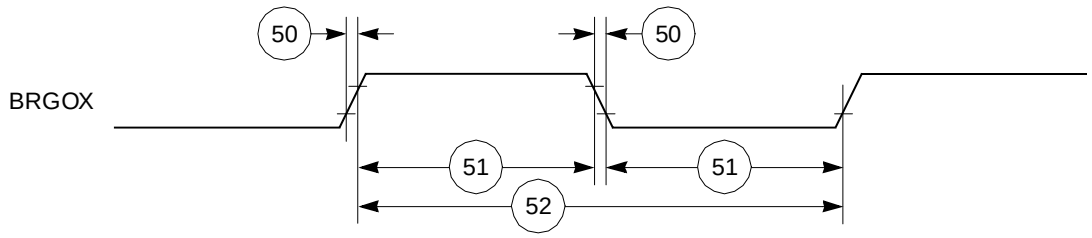


Figure 45. Baud Rate Generator Timing Diagram

14.4 Timer AC Electrical Specifications

Table 19 provides the general-purpose timer timings as shown in Figure 46.

Table 19. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

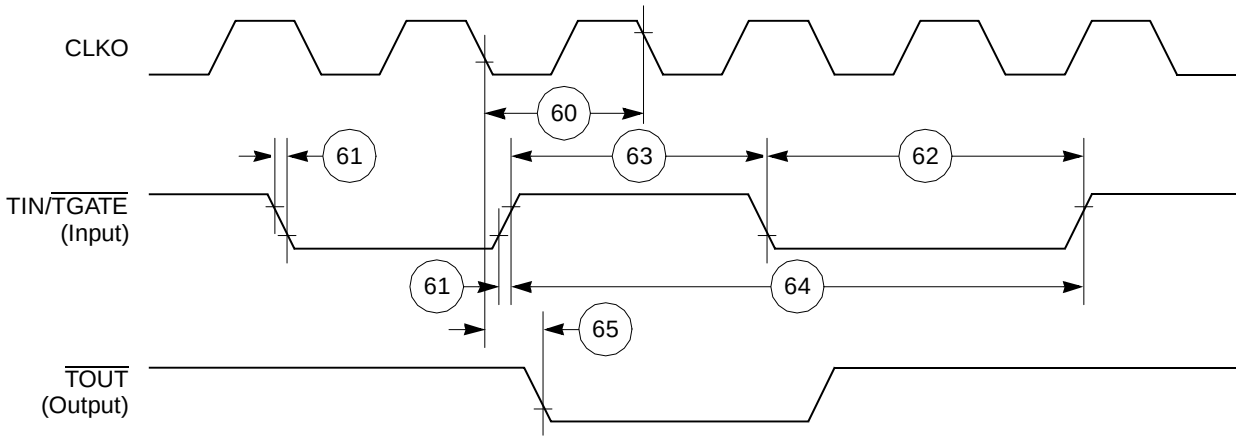


Figure 46. CPM General-Purpose Timers Timing Diagram

14.5 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high[1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK + 5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK3 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK3 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

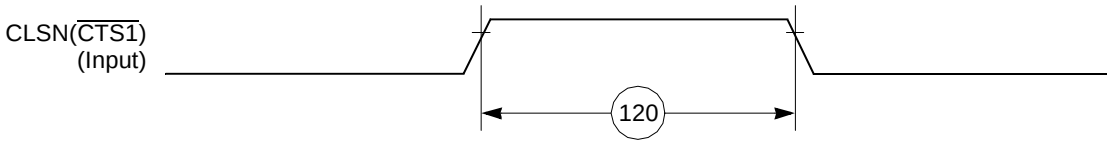


Figure 50. Ethernet Collision Timing Diagram

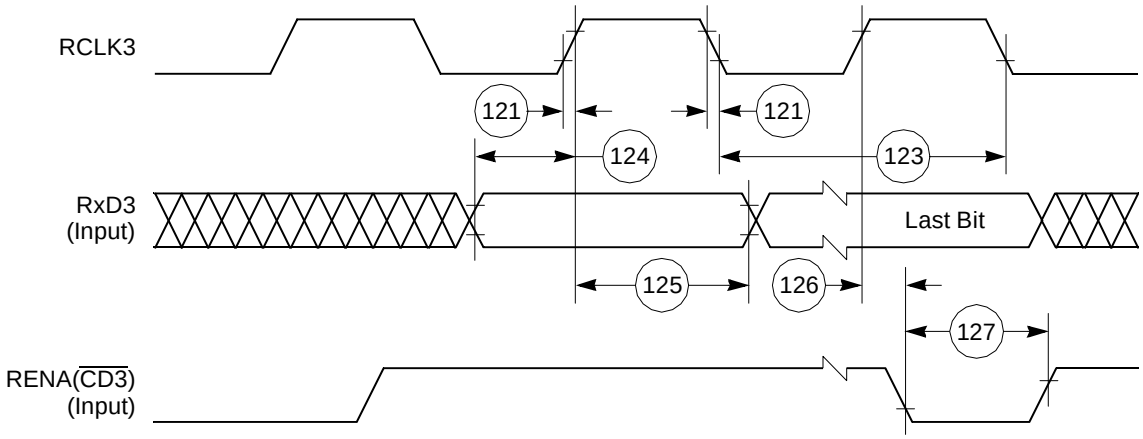


Figure 51. Ethernet Receive Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 28 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 28. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 62 shows the MII serial management channel timing diagram.

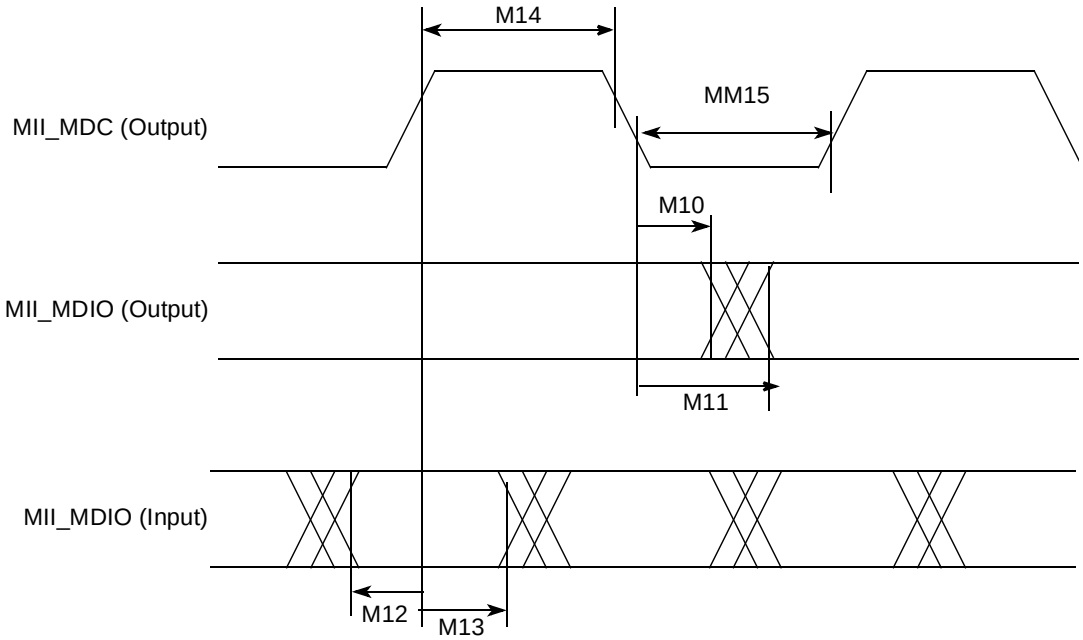


Figure 62. MII Serial Management Channel Timing Diagram

Table 30. Pin Assignments—JEDEC Standard (continued)

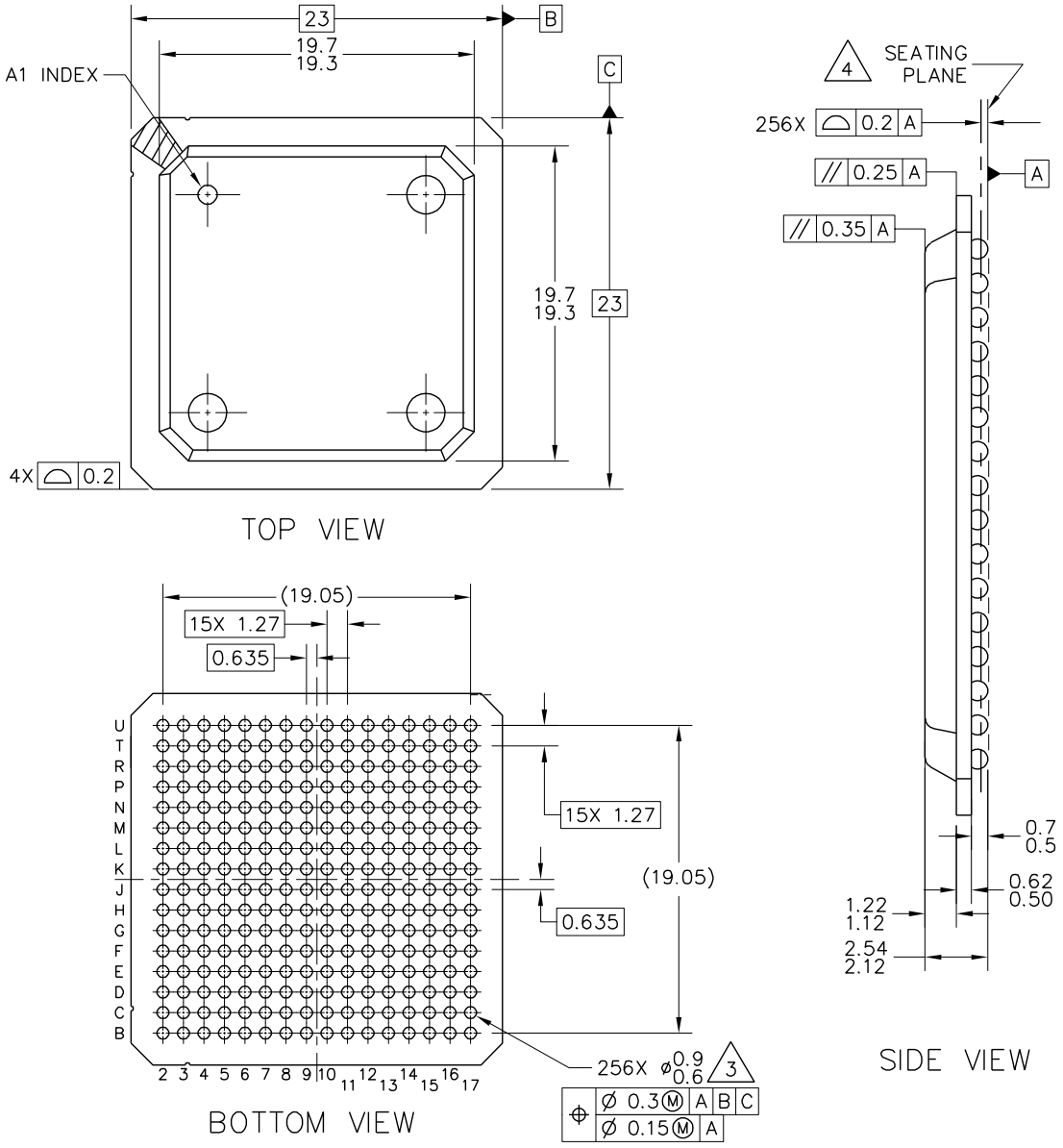
Name	Pin Number	Type
PA3, CLK5, BRGO3, TIN3	K16	Bidirectional (5-V tolerant)
PA2, CLK6, $\overline{\text{TOUT3}}$	K14	Bidirectional (5-V tolerant)
PA1, CLK7, BRGO4, TIN4	L15	Bidirectional (5-V tolerant)
PA0, CLK8, $\overline{\text{TOUT4}}$	M16	Bidirectional (5-V tolerant)
PB31, $\overline{\text{SPISEL}}$	E13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	F13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	D15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	G13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	H16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	L16	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	C16	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	E14	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	E15	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	J14	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	K15	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	J13	Bidirectional (5-V tolerant)

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PC4, $\overline{\text{CD4}}$	L14	Bidirectional (5-V tolerant)
PD15, MII_RXD3	M14	Bidirectional (5-V tolerant)
PD14, MII_RXD2	N16	Bidirectional (5-V tolerant)
PD13, MII_RXD1	K13	Bidirectional (5-V tolerant)
PD12, MII_MDC	N15	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	P16	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	R15	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	N14	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	M13	Bidirectional (5-V tolerant)
PD7, $\overline{\text{RTS3}}$, MII_RX_ER	T15	Bidirectional (5-V tolerant)
PD6, $\overline{\text{RTS4}}$, MII_RX_DV	N13	Bidirectional (5-V tolerant)
PD5, MII_TXD3	R14	Bidirectional (5-V tolerant)
PD4, MII_TXD2	P14	Bidirectional (5-V tolerant)
PD3, MII_TXD1	M12	Bidirectional (5-V tolerant)
TMS	F15	Input (5-V tolerant)
TDI, DSDI	G14	Input (5-V tolerant)
TCK, DSCK	H13	Input (5-V tolerant)
$\overline{\text{TRST}}$	F16	Input (5-V tolerant)
TDO, DSDO	F14	Output (5-V tolerant)
MII_CRS	B6	Input

16.2 Mechanical Dimensions of the PBGA Package

For more information on the printed-circuit board layout of the PBGA package, including thermal via design and suggested pad layout, refer to Plastic Ball Grid Array Application Note (order number: AN1231) that is available from your local Freescale sales office. Figure 65 shows the mechanical dimensions of the PBGA package.



Notes:

1. All dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M—1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.

Note: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC852TVRXXX.
Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC852TZTXXX.

Figure 65. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

17 Document Revision History

Table 32 lists significant changes between revisions of this document.

Table 32. Document Revision History

Revision	Date	Changes
4		• Updated template. • On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 2) and renumbered the rest of the figures. • In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 4, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 17, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..." • In Figure 42, changed $\overline{TA}$ to reflect the rising edge of the clock.
3.1	1/18/2005	Document template update.
3.0	11/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values • Added a footnote to Spec 41 specifying that EDM = 1 • Broke the Section 16.1, "Pin Assignments," into 2 smaller sections for the JEDEC and non-JEDEC pinouts.
2.0	12/2003	Put 852T on the 1st page in place of 8245. Figure 62 on page 59 had overbars added on signals CR (pin G2) and WAIT_A (pin P4).
1.8	7/2003	Changed the pinout to be JEDEC Compliant, changed timing parameters B28a through B28d, and B29d to show that TRLX can be 0 or 1.
1.7	5/2003	Changed the SPI Master Timing Specs. 162 and 164
1.6	4/2003	Changed the package drawing in Figure 15-63
1.5	4/2003	Changed 5 Port C pins with interrupt capability to 7 Port C pins. Added the Note: solder sphere composition for MPC852TVR and MPC852TCVR devices is 95.5%Sn 45%Ag 0.5%Cu to Figure 15-63
1.4	2/2003	Changed Table 15-30 Pin Assignments for the PLL Pins V_{SSSYN1}, V_{SSSYN}, V_{DDSYN}
1.3	1/2003	Added subscripts to timing diagrams for B1-B35, to specify memory controller settings for the specific edges.
1.2	1/2003	In Table 15-30, specified EXTCLK as 3.3 V.
1.1	12/2002	Added fast Ethernet controller to the features
1	11/2002	Added values for 80 and 100 MHz
0	10/2002	Initial release

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