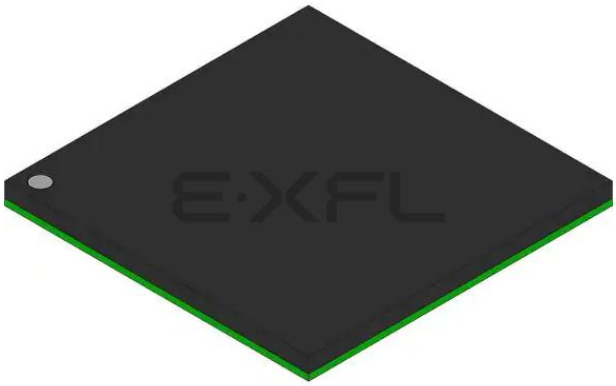

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc852tzt80a

  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller-programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet controller (FEC)
- General-purpose timers
  - Two 16-bit timers or one 32-bit timer
  - Gate mode can enable or disable counting
  - Interrupt can be masked on reference match and event capture
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1™ standard test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Seven port pins with interrupt capability
  - Eighteen internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest-priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Eight serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability

- Two baud rate generators
  - Independent (can be connected toany SCC3/4 or SMC1)
  - Allows changes during operation
  - Autobaud support option
- Two SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3® standard optional on SCC3 and SCC4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Universal asynchronous receiver transmitter (UART)
  - Totally transparent (bit streams)
  - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- One SMC (serial management channel)
  - UART
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one independent PCMCIA socket; 8-memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3-V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V tolerant pins.

Figure 1 shows the MPC852T block diagram.

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 4. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency (MHz)	Typical[1]	Maximum[2]	Unit
0	1:1	50	110	140	mW
		66	150	180	mW
	2:1	66	140	160	mW
		80	170	200	mW
		100	210	250	mW

1 Typical power dissipation is measured at 1.9 V.

2 Maximum power dissipation at V_{DDL} and V_{DDSYN} is at 1.9 V. and V_{DDH} is at 3.465 V.

NOTE

Values in Table 4 represent V_{DDL}-based power dissipation, and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application that buffer current can cause, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC852T.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH}	3.135	3.465	V
	V_{DDL}	1.7	1.9	V
	V_{DDSYN}	1.7	1.9	V
	Difference between V_{DDL} to V_{DDSYN}	—	100	mV
Input high voltage (all inputs except PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO)[1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input leakage current, Vin = 5.5 V (Except TMS, TRST, DSCK and DSDI pins) for 5-V tolerant pins [1]	I_{in}	—	100	µA
Input leakage current, Vin = V_{DDH} (Except TMS, TRST, DSCK, and DSDI)	I_{In}	—	10	µA
Input leakage current, Vin = 0 V (Except TMS, TRST, DSCK and DSDI pins)	I_{In}	—	10	µA
Input capacitance[2]	C_{in}	—	20	pF
Output high voltage, IOH = -2.0 mA, V_{DDH} = 3.0 V Except XTAL and open drain pins	VOH	2.4	—	V
Output low voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA[3] IOL = 5.3 mA[4] IOL = 7.0 mA (Txd1/pa14, txd2/pa12) IOL = 8.9 mA (TS, TA, TEA, BI, BB, HRESET, SRESET)	VOL	—	0.5	V

1 The PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, TRST, TMS, MII_TXEN, MII_MDIO are 5-V tolerant pins.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IWP(0:1)/VFLS(0:1), RXD3/PA11, TXD3/PA10, RXD4/PA9, TXD4/PA8, TIN3/BRGO3/CLK5/PA3, BRGCLK2/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, TOUT4/CLK8/PA0, SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, SMTXD1/PB25, SMRXD1/PB24, BRGO3/PB15, RTS1/DREQ0/PC15, RTS3/PC13, RTS4/PC12, CTS3/PC7, CD3/PC6, CTS4/SDACK1/PC5, CD4/PC4, MII-RXD3/PD15, MII-RXD2/PD14, MII-RXD1/PD13, MII-MDC/PD12, MII-TXERR/RXD3/PD11, MII-RX0/TXD3/PD10, MII-TXD0/RXD4/PD9, MII-RXCLK/TXD4/PD8, MII-TXD3/PD5, MII-RXDV/RTS4/PD6, MII-RXERR/RTS3/PD7, MII-TXD2/REJECT3/PD4, MII-TXD1/REJECT4/PD3, MII_CRS, MII_MDIO, MII_TXEN, and MII_COL

4 BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6), CS(7), WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/ BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, GPL_A5, ALE_A, CE1_A, CE2_A, DSCK, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, and BADDR(28:30)

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times IDDL) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter
T_T = thermocouple temperature on top of package
P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors that cooling effects of the thermocouple wire cause.

8 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) specifications (Available from Global Engineering documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

9 Power Supply and Power Sequencing

This section provides design considerations for the MPC852T power supply. The MPC852T has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}) that operates at a lower voltage than the I/O voltage V_{DDH}. The I/O section of the MPC852T is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15] PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO are 5-V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins can not exceed 5.5 V, and the remaining input pins cannot exceed 3.465 V. This restriction applies to power-on reset or power down and normal operation.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power-on reset or power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 3 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power-on reset, and the 1N5820 diodes regulate the maximum potential difference on power-down.

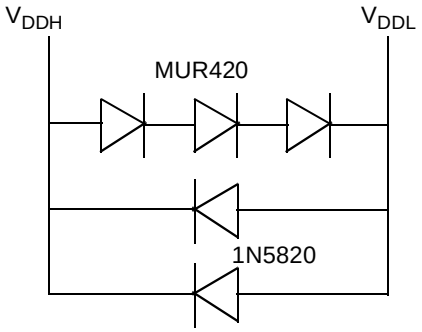

Figure 3. Example Voltage Sequencing Circuit

10 Mandatory Reset Configurations

The MPC852T requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion, the HRCW[DBGC] value that is needed to be set to binary X1 in the hardware reset configuration word (HRCW) and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset.

If hardware reset configuration word (HRCW) is disabled, by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30b	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B30c	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid- as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B37	UPWAIT valid to CLKOUT falling edge[10] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[10] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[11] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the maximum allowed jitter on EXTAL can be up to 2%.

2 For part speeds above 50MHz, use 9.80ns for B11a.

3 The timing required for $\overline{BR}$ input is relevant when the MPC852T is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC852T is selected to work with external bus arbiter.

4 For part speeds above 50MHz, use 2ns for B17.

5 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

6 For part speeds above 50MHz, use 2ns for B19.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 This formula applies to bus operation up to 50 MHz.

9 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

10 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 19.

11 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 22.

Figure 6 provides the timing for the synchronous output signals.

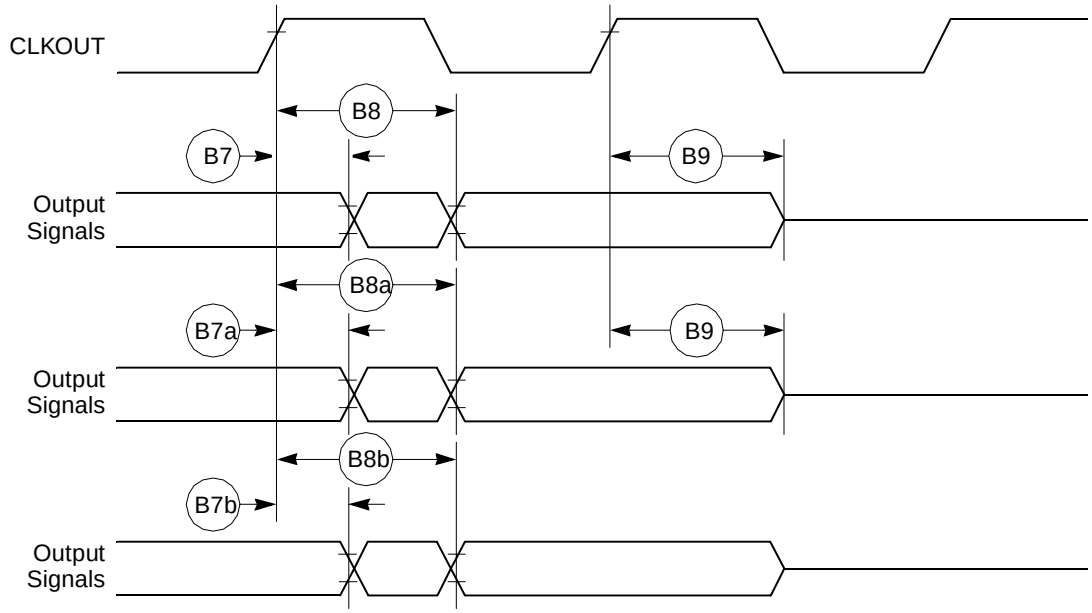

Figure 6. Synchronous Output Signals Timing

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

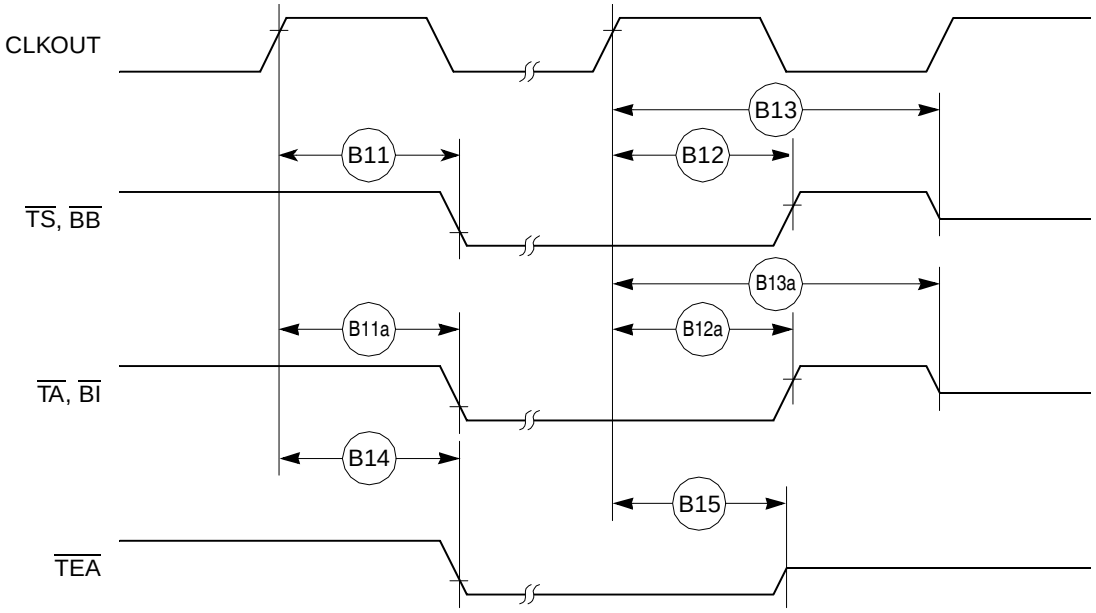

Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

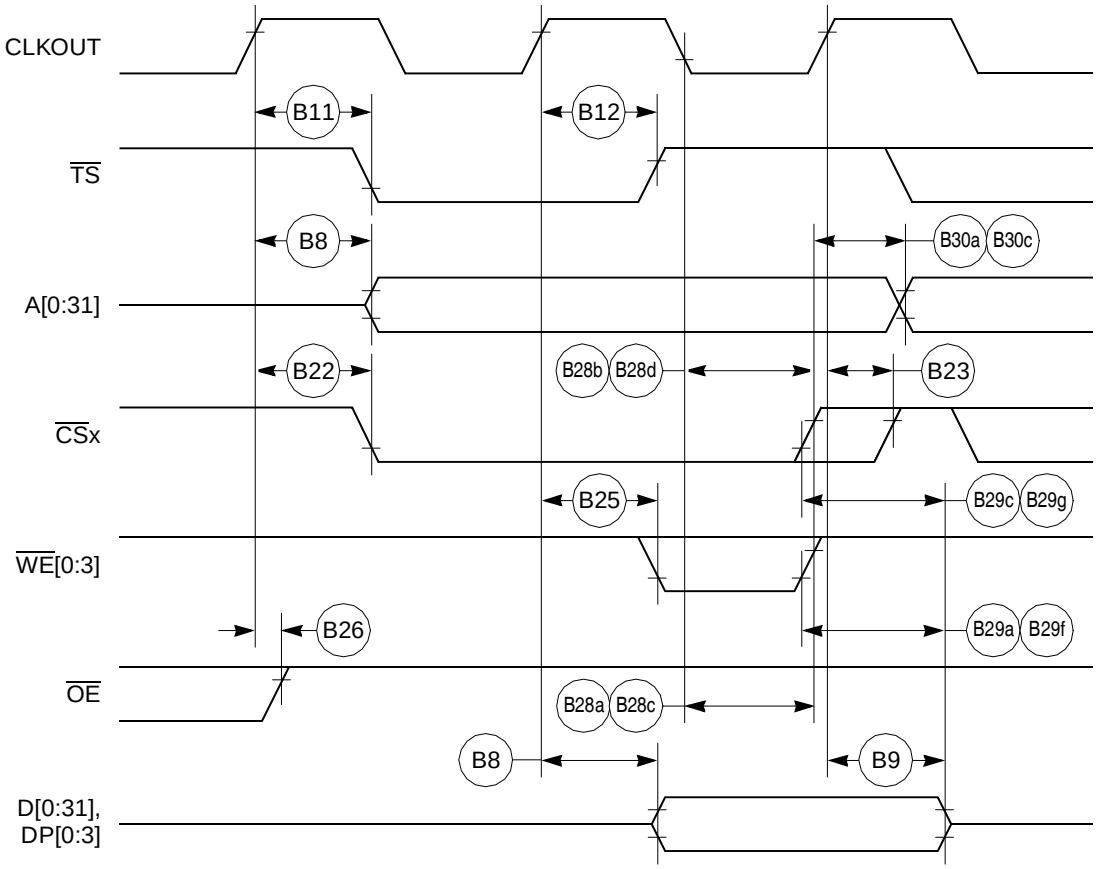

Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 19 provides the timing for the asynchronous asserted UPWAIT signal that the UPM controls.

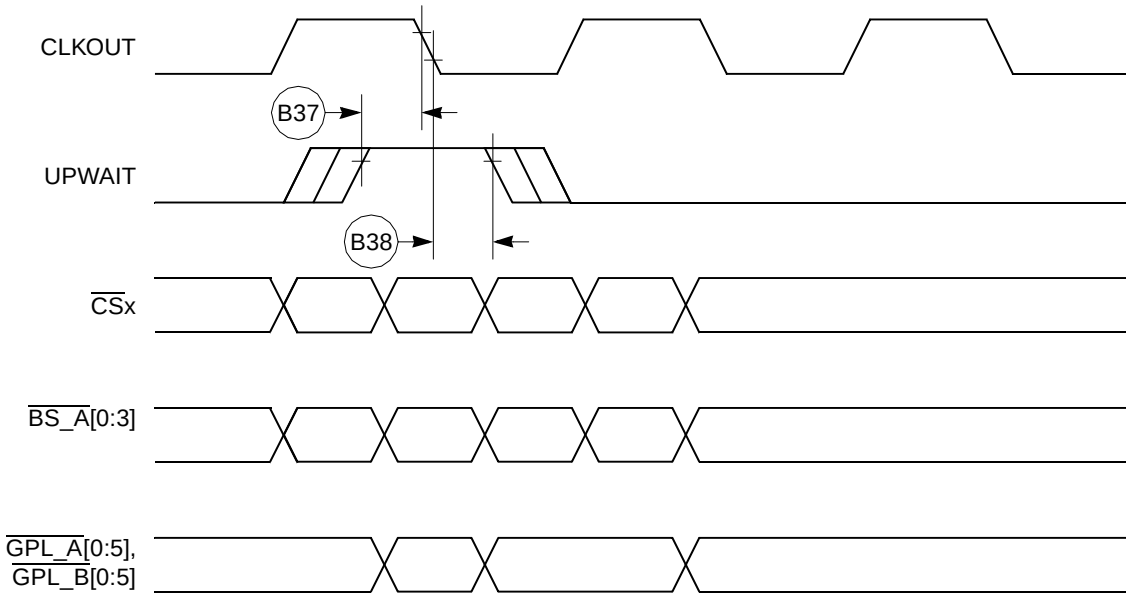

Figure 19. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 20 provides the timing for the asynchronous negated UPWAIT signal that the UPM controls.

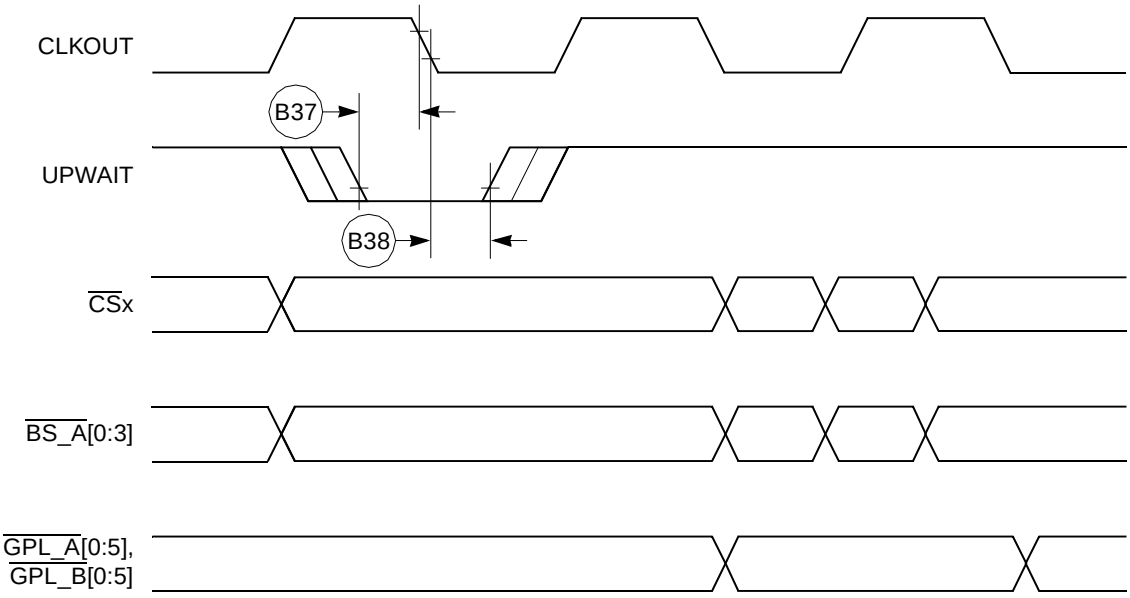

Figure 20. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Figure 21 provides the timing for the synchronous external master access that the GPCM controls.

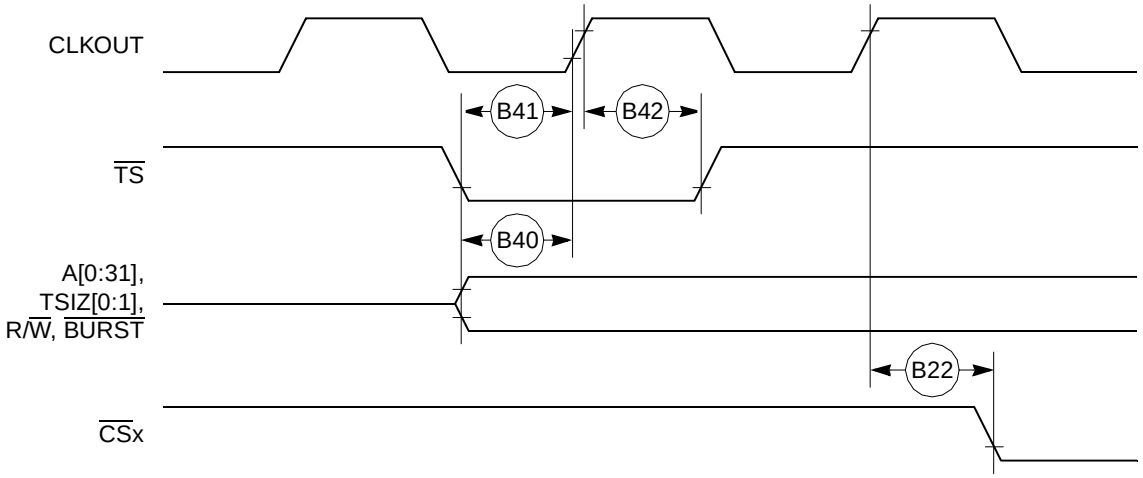

Figure 21. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 22 provides the timing for the asynchronous external master memory access that the GPCM controls.

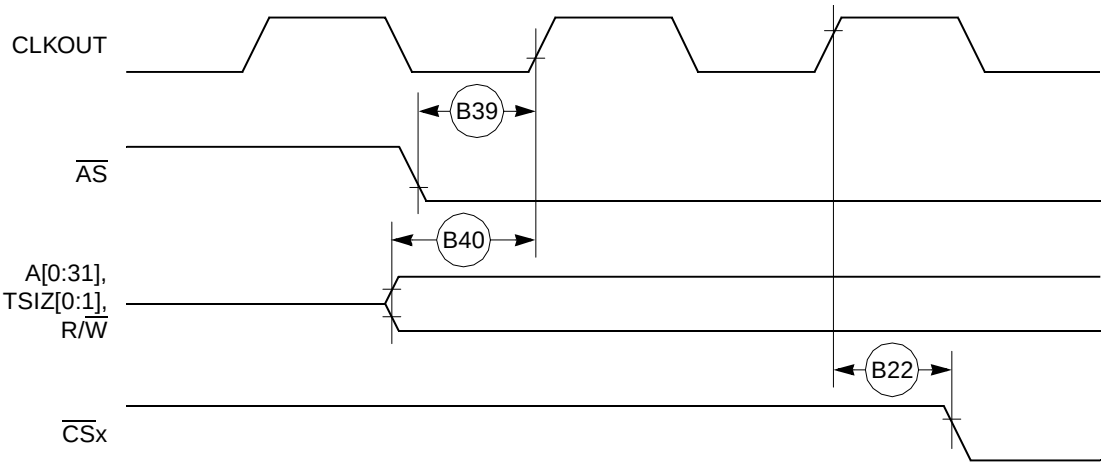

Figure 22. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 23 provides the timing for the asynchronous external master control signals negation.

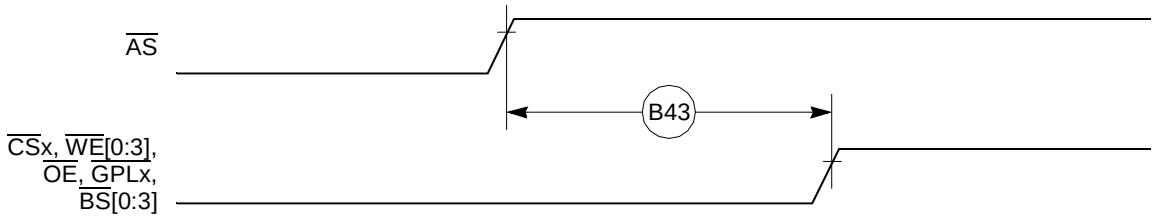

Figure 23. Asynchronous External Master—Control Signals Negation Timing

Figure 27 provides the PCMCIA access cycle timing for the external bus write.

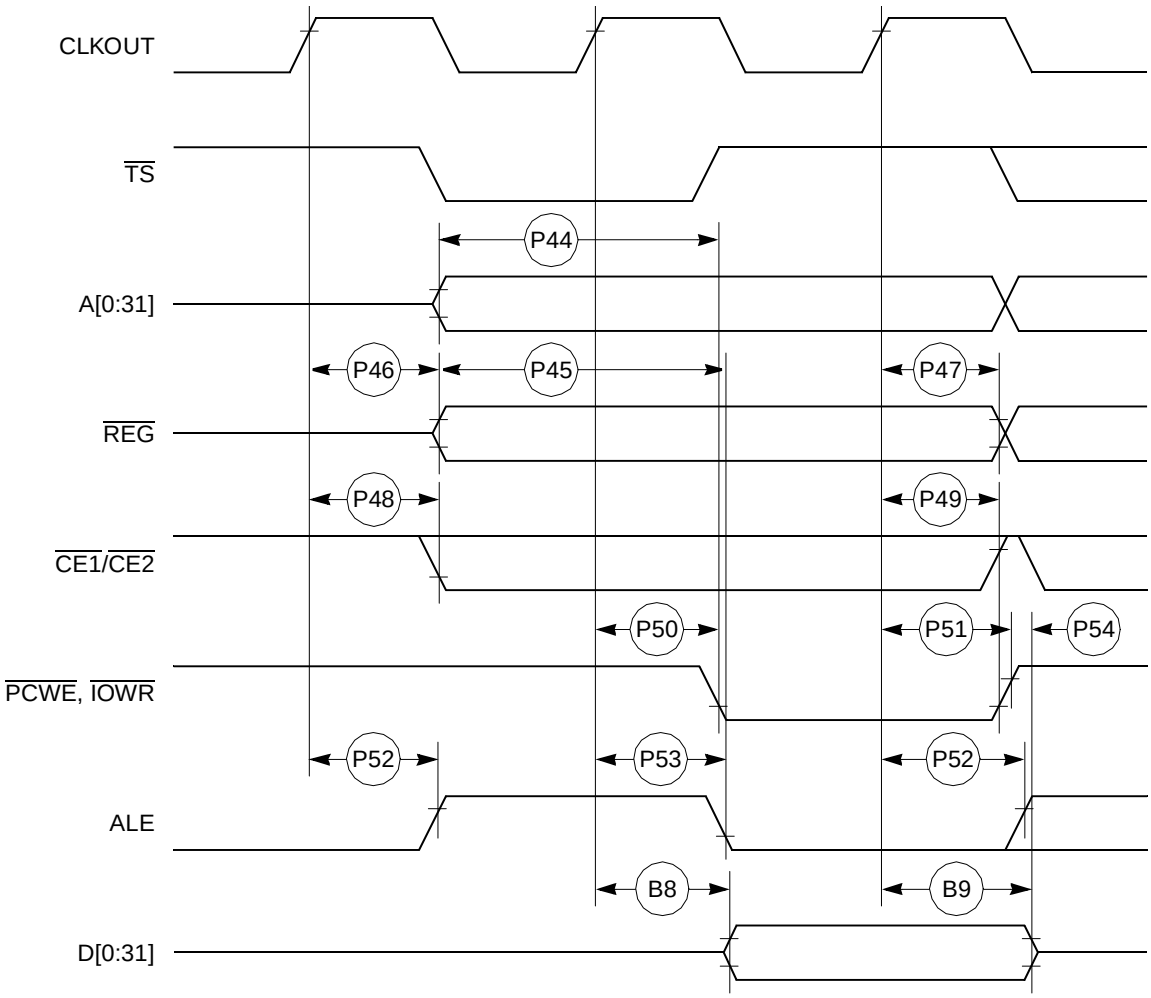

Figure 27. PCMCIA Access Cycles Timing External Bus Write

Figure 28 provides the PCMCIA WAIT signals detection timing.

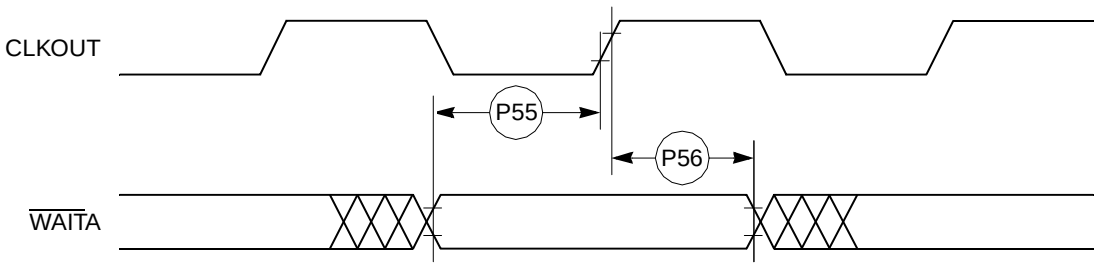

Figure 28. PCMCIA WAIT Signals Detection Timing

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
135	$\overline{\text{RSTRT}}$ active delay (from TCLK3 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK3 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

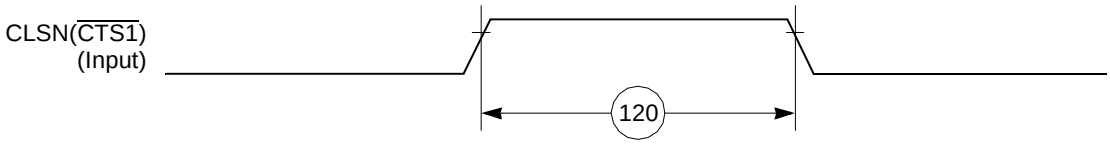

Figure 50. Ethernet Collision Timing Diagram

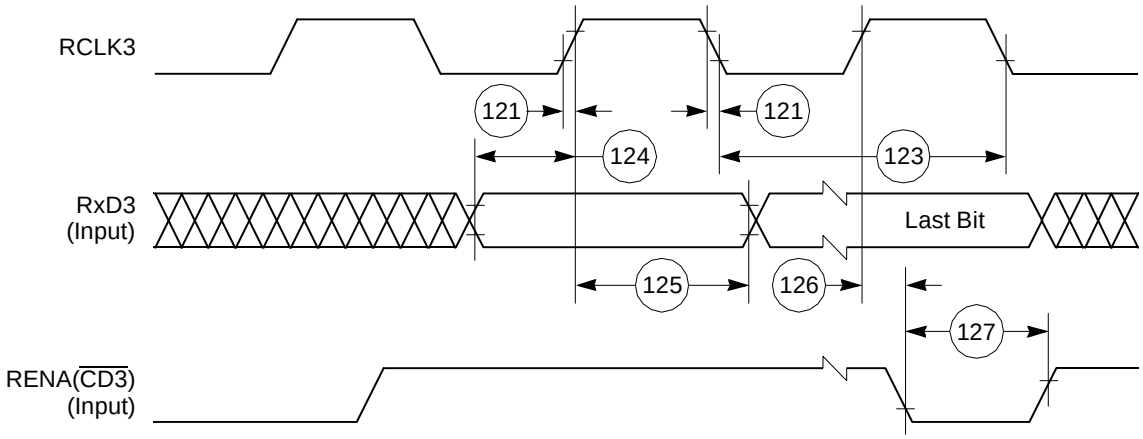

Figure 51. Ethernet Receive Timing Diagram

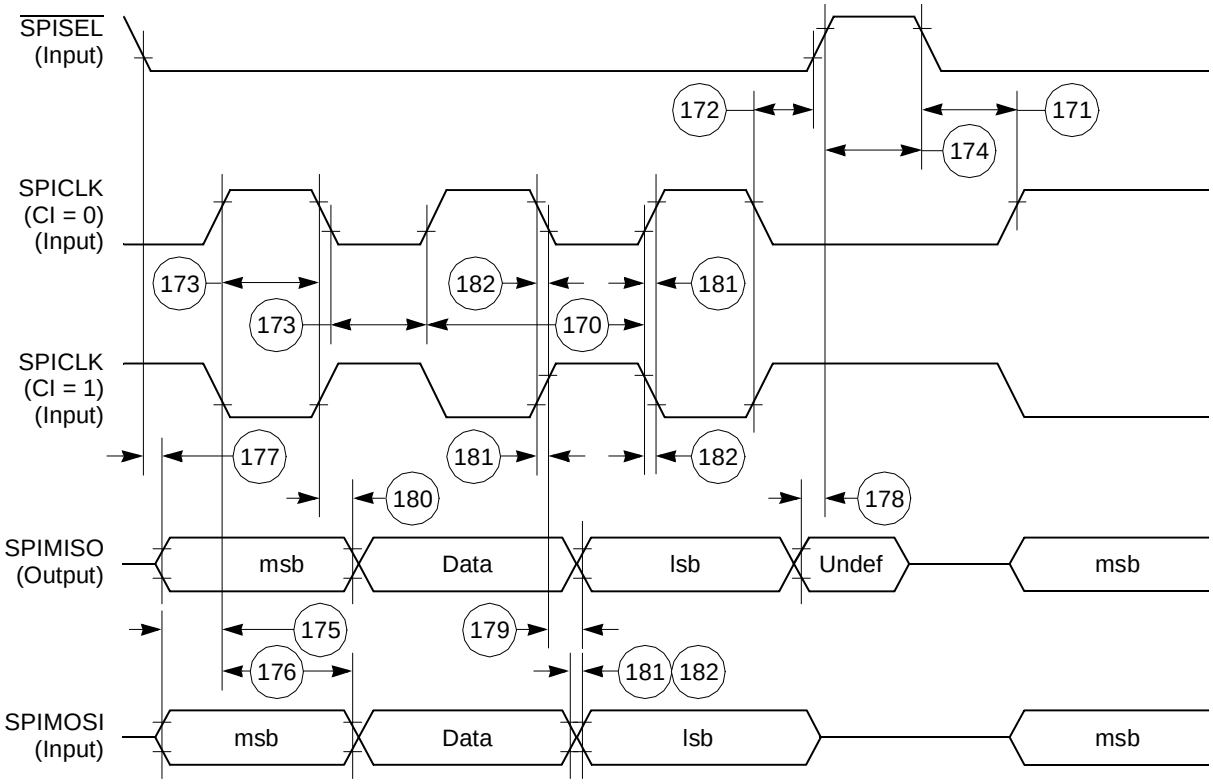

Figure 57. SPI Slave (CP = 0) Timing Diagram

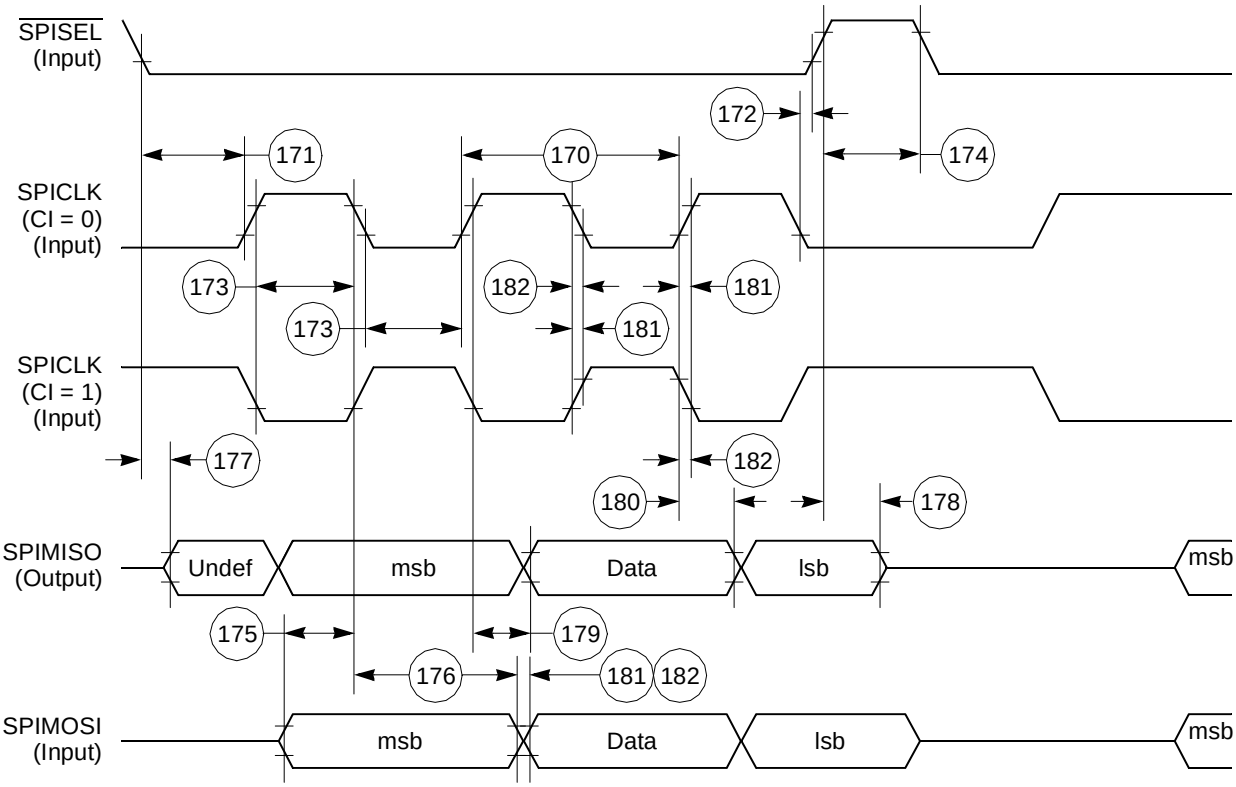

Figure 58. SPI Slave (CP = 1) Timing Diagram

Table 26 provides information about the MII transmit signal timing,.

Table 26. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	—
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 60 shows the MII transmit signal timing diagram.

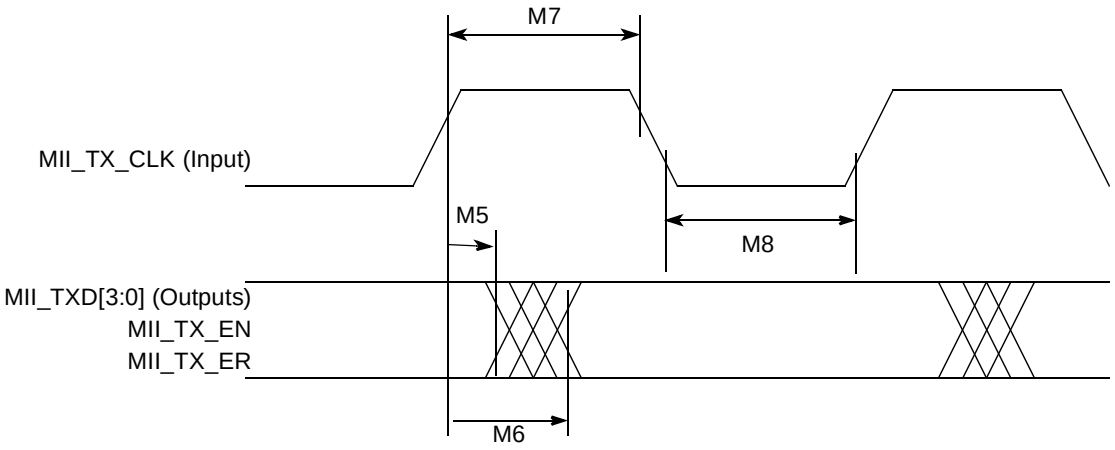

Figure 60. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 27 provides information about the MII async inputs signal timing.

Table 27. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 61 shows the MII asynchronous inputs signal timing diagram.

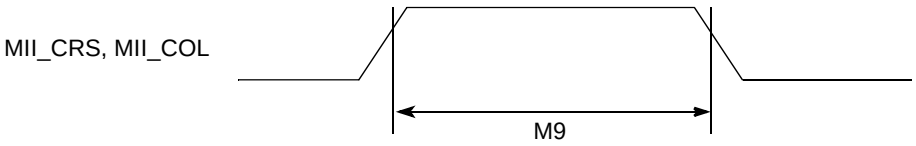

Figure 61. MII Async Inputs Timing Diagram

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PC4, $\overline{\text{CD4}}$	L14	Bidirectional (5-V tolerant)
PD15, MII_RXD3	M14	Bidirectional (5-V tolerant)
PD14, MII_RXD2	N16	Bidirectional (5-V tolerant)
PD13, MII_RXD1	K13	Bidirectional (5-V tolerant)
PD12, MII_MDC	N15	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	P16	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	R15	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	N14	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	M13	Bidirectional (5-V tolerant)
PD7, $\overline{\text{RTS3}}$, MII_RX_ER	T15	Bidirectional (5-V tolerant)
PD6, $\overline{\text{RTS4}}$, MII_RX_DV	N13	Bidirectional (5-V tolerant)
PD5, MII_TXD3	R14	Bidirectional (5-V tolerant)
PD4, MII_TXD2	P14	Bidirectional (5-V tolerant)
PD3, MII_TXD1	M12	Bidirectional (5-V tolerant)
TMS	F15	Input (5-V tolerant)
TDI, DSDI	G14	Input (5-V tolerant)
TCK, DSCK	H13	Input (5-V tolerant)
$\overline{\text{TRST}}$	F16	Input (5-V tolerant)
TDO, DSDO	F14	Output (5-V tolerant)
MII_CRS	B6	Input

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