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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

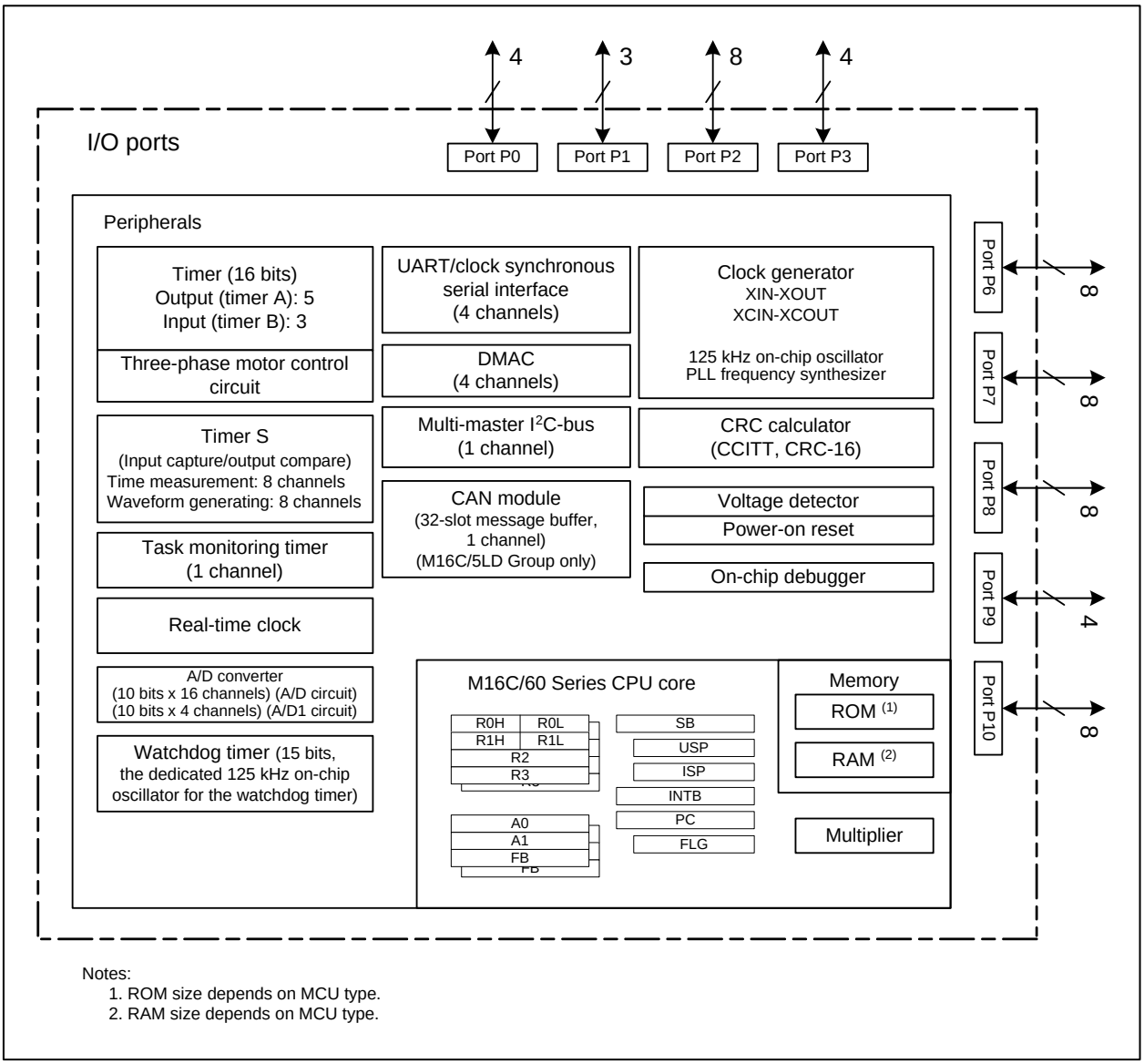
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f3562edfe-u0

Table 1.2 Specifications (80-pin Version) (2/2)

Item	Function	Specification
CRC Calculator		• 1 circuit • CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant • MSB/LSB selectable
Multi-master I^2C-bus Interface		1 channel
CAN Module		32-slot message buffer × 1 channel (M16C/5LD Group only)
Flash Memory		• Programming and erasure supply voltage: 2.7 to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V 25 MHz / 2.7 to 5.5 V
Current Consumption		Described in 5. “Electrical Characteristics”
Operating Temperature		-40°C to 85°C (1)
Package		80-pin plastic mold LQFP: PLQP0080KB-A (Previous package code: 80P6Q-A)

Note:
1. Refer to Table 1.5 “Product List of M16C/5LD Group” and Table 1.6 “Product List of M16C/56D Group” for the Operating Temperature.

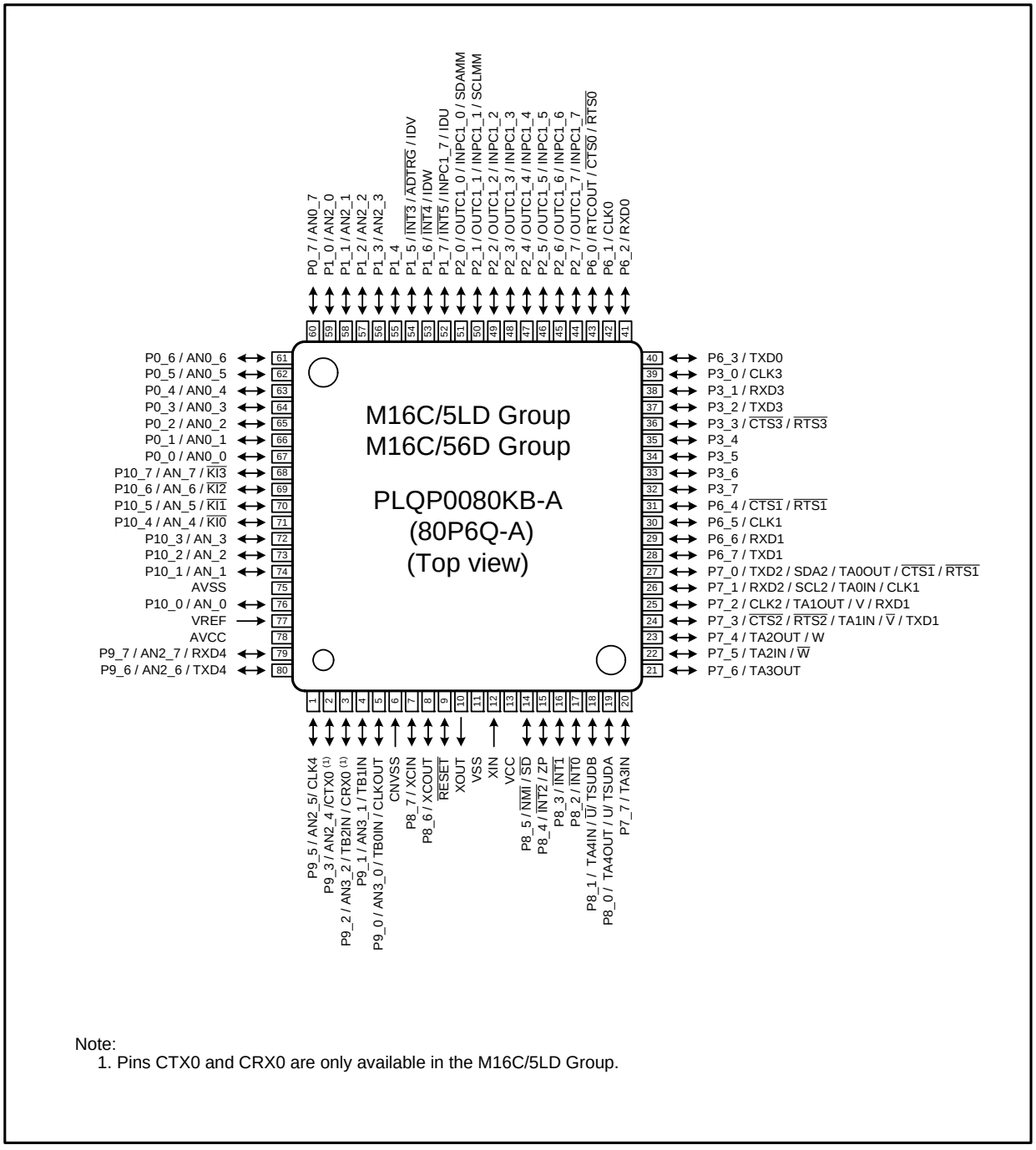


Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.4 64-Pin Block Diagram

1.5 Pin Assignments

Figure 1.5 shows the pin assignments for 80-pin package, and Table 1.7 and Table 1.8 list pin names for 80-pin package.



Note:
1. Pins CTX0 and CRX0 are only available in the M16C/5LD Group.

Figure 1.5 Pin Assignment for 80-Pin Package (Top View)

Set bits PACR2 to PACR0 in the PACR register to 010b before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some of the pins.

Table 1.7 Pin Names, 80-Pin Package (1/2)

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I2C-bus pin	Analog Pin
1		P9_5				CLK4		AN2_5
2		P9_3				CTX0 (1)		AN2_4
3		P9_2		TB2IN		CRX0 (1)		AN3_2
4		P9_1		TB1IN				AN3_1
5	CLKOUT	P9_0		TB0IN				AN3_0
6	CNVSS							
7	XCIN	P8_7						
8	XCOUT	P8_6						
9	$\overline{\text{RESET}}$							
10	XOUT							
11	VSS							
12	XIN							
13	VCC							
14		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$				
15		P8_4	$\overline{\text{INT2}}$	ZP				
16		P8_3	$\overline{\text{INT1}}$					
17		P8_2	$\overline{\text{INT0}}$					
18		P8_1		TA4IN/$\overline{\text{U}}$	TSUDB			
19		P8_0		TA4OUT/U	TSUDA			
20		P7_7		TA3IN				
21		P7_6		TA3OUT				
22		P7_5		TA2IN/$\overline{\text{W}}$				
23		P7_4		TA2OUT/W				
24		P7_3		TA1IN/$\overline{\text{V}}$		$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TXD1		
25		P7_2		TA1OUT/V		CLK2/RXD1		
26		P7_1		TA0IN		RXD2/SCL2/CLK1		
27		P7_0		TA0OUT		TXD2/SDA2/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
28		P6_7				TXD1		
29		P6_6				RXD1		
30		P6_5				CLK1		
31		P6_4				$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
32		P3_7						
33		P3_6						
34		P3_5						
35		P3_4						
36		P3_3				$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$		
37		P3_2				TXD3		
38		P3_1				RXD3		
39		P3_0				CLK3		
40		P6_3				TXD0		

Note 1. There are pins CTX0 and CRX0 only in the M16C/5LD Group.

Table 1.10 Pin Names, 64-Pin Package (2/2)

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I^2C-bus pin	Analog Pin
41		P2_3			OUTC1_3/INPC1_3			
42		P2_2			OUTC1_2/INPC1_2			
43		P2_1			OUTC1_1/INPC1_1		SCLMM	
44		P2_0			OUTC1_0/INPC1_0		SDAMM	
45		P1_7	$\overline{INT5}$	IDU	INPC1_7			
46		P1_6	$\overline{INT4}$	IDW				
47		P1_5	$\overline{INT3}$	IDV				$\overline{ADTRG}$
48		P0_3						AN0_3
49		P0_2						AN0_2
50		P0_1						AN0_1
51		P0_0						AN0_0
52		P10_7	$\overline{KI3}$					AN_7
53		P10_6	$\overline{KI2}$					AN_6
54		P10_5	$\overline{KI1}$					AN_5
55		P10_4	$\overline{KI0}$					AN_4
56		P10_3						AN_3
57		P10_2						AN_2
58		P10_1						AN_1
59	AVSS							
60		P10_0						AN_0
61	VREF							
62	AVCC							
63		P9_3				CTX0 (1)		AN2_4
64		P9_2		TB2IN		CRX0 (1)		AN3_2

Note 1. There are pins CTX0 and CRX0 only in the M16C/5LD Group.

Table 1.13 Pin Functions (80-Pin Package Only)

Signal Name	Pin Name	I/O	Description
Serial Interface UART4	CLK4	I/O	Transfer clock input/output
	RXD4	I	Serial data input
	TXD4	O	Serial data output
A/D converter	AN0_4 to AN0_7 AN2_0 to AN2_3 AN2_5 to AN2_7	I	Analog input for the A/D converter
I/O port	P0_4 to P0_7 P1_0 to P1_4 P3_4 to P3_7 P9_5 to P9_7	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, pull-up resistor is selectable for every unit of 4 bits.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	Reset Value
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b
033Fh			
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh			
035Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	Reset Value
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h			
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.18 SFR Information (18) (1)

Address	Register	Symbol	Reset Value
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h	A/D Trigger Control Register	ADTRGCON	XXXX 00XXb
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b
03D8h			
03D9h			
03DAh			
03DBh			
03DCh			
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h			
03E9h			
03EAh			
03EBh			
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.27 SFR Information (27) (1)

Address	Register	Symbol	Reset Value
D650h	CAN0 Mailbox 21: Message Identifier	C0MB21	XXh
D651h			XXh
D652h			XXh
D653h			XXh
D654h			
D655h	CAN0 Mailbox 21: Data Length		XXh
D656h	CAN0 Mailbox 21: Data Field		XXh
D657h			XXh
D658h			XXh
D659h			XXh
D65Ah			XXh
D65Bh			XXh
D65Ch			XXh
D65Dh			XXh
D65Eh	CAN0 Mailbox 21: Time Stamp		XXh
D65Fh			XXh
D660h	CAN0 Mailbox 22: Message Identifier	C0MB22	XXh
D661h			XXh
D662h			XXh
D663h			XXh
D664h			
D665h	CAN0 Mailbox 22: Data Length		XXh
D666h	CAN0 Mailbox 22: Data Field		XXh
D667h			XXh
D668h			XXh
D669h			XXh
D66Ah			XXh
D66Bh			XXh
D66Ch			XXh
D66Dh			XXh
D66Eh	CAN0 Mailbox 22: Time Stamp		XXh
D66Fh			XXh
D670h	CAN0 Mailbox 23: Message Identifier	C0MB23	XXh
D671h			XXh
D672h			XXh
D673h			XXh
D674h			
D675h	CAN0 Mailbox 23: Data Length		XXh
D676h	CAN0 Mailbox 23: Data Field		XXh
D677h			XXh
D678h			XXh
D679h			XXh
D67Ah			XXh
D67Bh			XXh
D67Ch			XXh
D67Dh			XXh
D67Eh	CAN0 Mailbox 23: Time Stamp		XXh
D67Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.28 SFR Information (28) (1)

Address	Register	Symbol	Reset Value
D680h	CAN0 Mailbox 24: Message Identifier	C0MB24	XXh
D681h			XXh
D682h			XXh
D683h			XXh
D684h			
D685h	CAN0 Mailbox 24: Data Length		XXh
D686h	CAN0 Mailbox 24: Data Field		XXh
D687h			XXh
D688h			XXh
D689h			XXh
D68Ah			XXh
D68Bh			XXh
D68Ch			XXh
D68Dh			XXh
D68Eh	CAN0 Mailbox 24: Time Stamp		XXh
D68Fh			XXh
D690h	CAN0 Mailbox 25: Message Identifier	C0MB25	XXh
D691h			XXh
D692h			XXh
D693h			XXh
D694h			
D695h	CAN0 Mailbox 25: Data Length		XXh
D696h	CAN0 Mailbox 25: Data Field		XXh
D697h			XXh
D698h			XXh
D699h			XXh
D69Ah			XXh
D69Bh			XXh
D69Ch			XXh
D69Dh			XXh
D69Eh	CAN0 Mailbox 25: Time Stamp		XXh
D69Fh			XXh
D6A0h	CAN0 Mailbox 26: Message Identifier	C0MB26	XXh
D6A1h			XXh
D6A2h			XXh
D6A3h			XXh
D6A4h			
D6A5h	CAN0 Mailbox 26: Data Length		XXh
D6A6h	CAN0 Mailbox 26: Data Field		XXh
D6A7h			XXh
D6A8h			XXh
D6A9h			XXh
D6AAh			XXh
D6ABh			XXh
D6ACh			XXh
D6ADh			XXh
D6AEh	CAN0 Mailbox 26: Time Stamp		XXh
D6AFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 5.10 Power-On Reset Circuit

The measurement condition is T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		2.0		50000	mV/ms
t_{fth}	External power V_{CC} fall gradient				50000	mV/ms
V_{por}	Voltage at which power-on reset enabled (1)				0.1	V
$t_{w(por)}$	Hold time at which power-on reset enabled		1.0			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0.

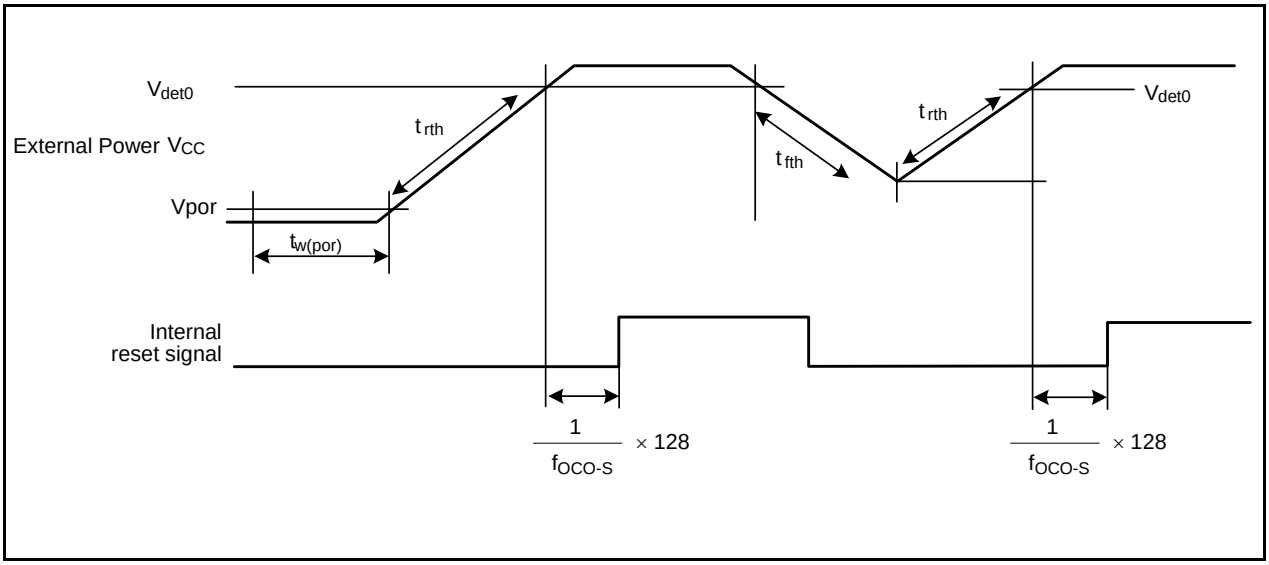


Figure 5.4 Power-On Reset Circuit Electrical Characteristics

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	VCC = 3.0 V to 5.5V			5	ms
$t_{d(R-S)}$	STOP release time				300	µs
$td_{(W-S)}$	Low power mode wait mode release time				300	µs

Note:
1. When V_{CC} = 5 V.

V_{CC} = 5 V

5.2.2 Timing Requirements (Peripheral Functions and Others)

(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = -40°C to 85°C unless otherwise specified)

5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.15 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

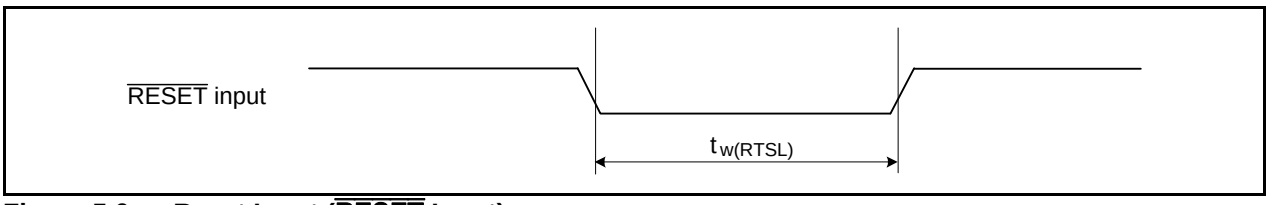


Figure 5.6 Reset Input ($\overline{\text{RESET}}$ Input)

5.2.2.2 External Clock Input

Table 5.16 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is V_{CC} = 3.0V to 5.0V

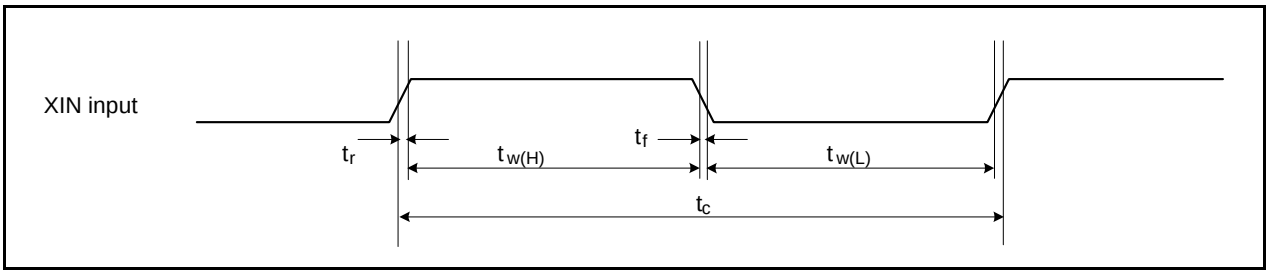


Figure 5.7 External Clock Input (XIN Input)

V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

Table 5.21 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

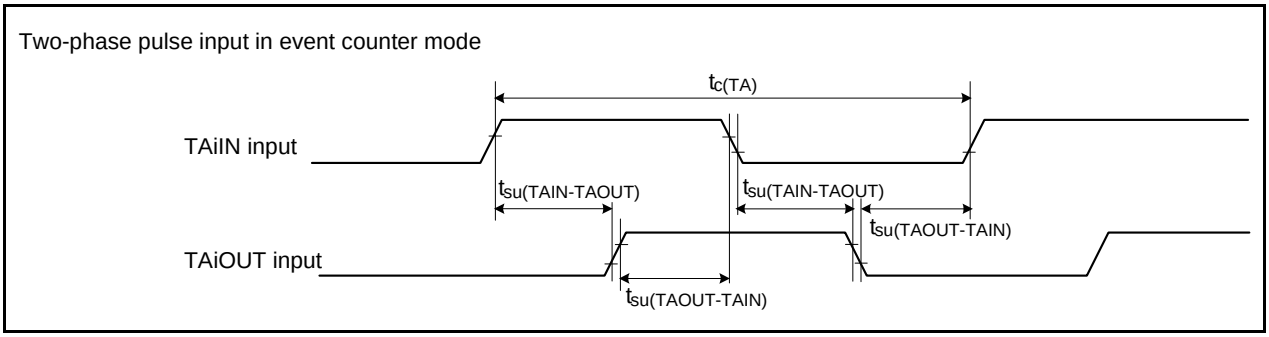


Figure 5.9 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

V_{CC} = 5 V

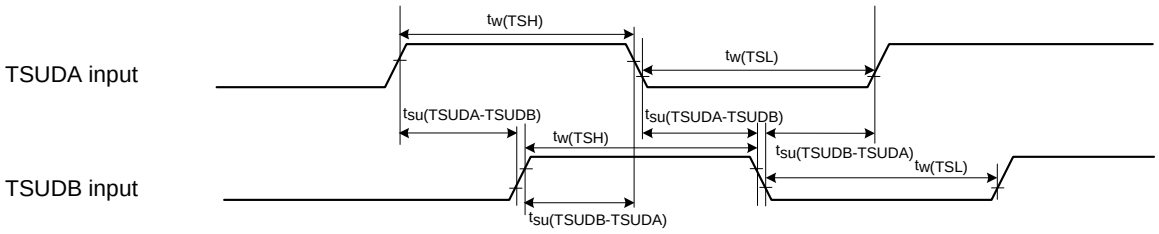
Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.2.2.5 Timer S Input

Table 5.25 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 5.11 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

5.3 Electrical Characteristics (V_{CC} = 3 V)

5.3.1 Electrical Characteristics

V_{CC} = 3 V

Table 5.29 Electrical Characteristics (1)

V_{CC} = 2.7 to 3.3V, V_{SS} = 0 V at T_{opr} = −40°C to 85°C, $f_{(BCLK)}$=25 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7		I_{OH} = −1 mA	V_{CC}−0.5		V_{CC}	V
V_{OH}	HIGH output voltage XOUT		HIGH POWER	I_{OH} = −0.1 mA	V_{CC}−0.5		V_{CC}	V
			LOW POWER	I_{OH} = −50 µA	V_{CC}−0.5		V_{CC}	
	HIGH output voltage XCOUT		HIGH POWER	With no load applied		2.5		V
			LOW POWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7		I_{OL} = 1mA			0.5	V
V_{OL}	LOW output voltage XOUT		HIGH POWER	I_{OL} = 0.1mA			0.5	V
			LOW POWER	I_{OL} = 50µA			0.5	
	LOW output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS3}$, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0					0.4V_{CC}	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$					1.8	V
V_{T+}-V_{T-}	Hysteresis	XIN					0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 3V			4.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 0V			−4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7		V_I = 0V	50	100	500	kΩ
R_{fXIN}	Feedback resistance XIN					3.0		MΩ
R_{fXCIN}	Feedback resistance XCIN					25		MΩ
V_{RAM}	RAM retention voltage			At stop mode	2.0			V

V_{CC} = 3 V

Table 5.30 Electrical Characteristics (2)

Topr = –40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.0 V to 3.6 V) In single-chip mode, the output pins are open and other pins are VSS	High speed mode	$f_{(BCLK)}$ = 25 MHz, XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operates		26	40	mA
			$f_{(BCLK)}$ = 20 MHz, XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operates		19	28	mA
			$f_{(BCLK)}$ = 16 MHz, XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operates		15		mA
		125 kHz on-chip oscillator mode	Main clock stops 125 kHz on-chip oscillator operates Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		150	500	µA
		Low power mode	$f_{(BCLK)}$ = 32 kHz On Flash memory (1) FMR22 = FMR23 = 1 (Low-current consumption read mode)		160		µA
		Wait mode	Main clock stops 125 kHz on-chip oscillator operates Peripheral clock operates Topr = 25°C		20		µA
			Main clock stops 125 kHz on-chip oscillator operates Peripheral clock operates T_{opr} = 85°C		50		µA
		Stop mode	T_{opr} = 25°C		17	27	µA
			T_{opr} = 85°C		45		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 3.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 3.0 V		30.0		mA
I_{det2}	Low voltage detection dissipation current				3		µA
I_{det0}	Reset area detection dissipation current				6		µA

Note:

1. This indicates the memory in which the program to be executed exists.

V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

Table 5.37 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

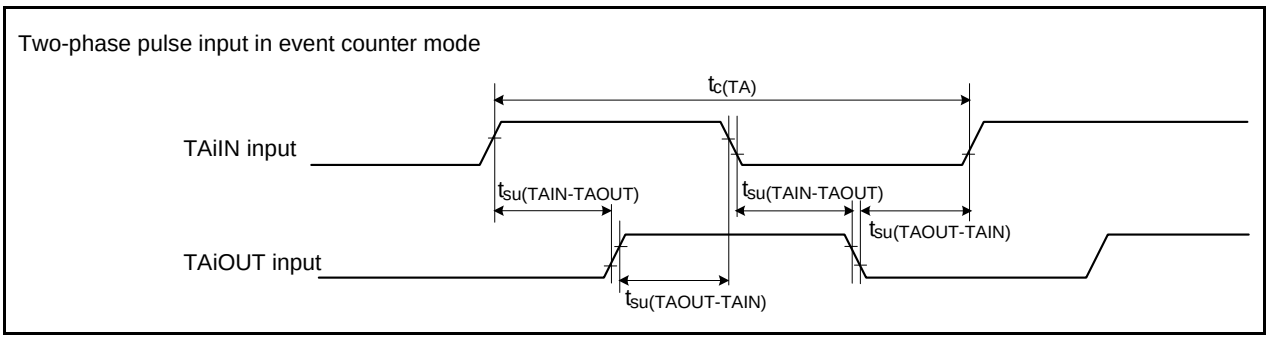


Figure 5.18 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

V_{CC} = 3 V

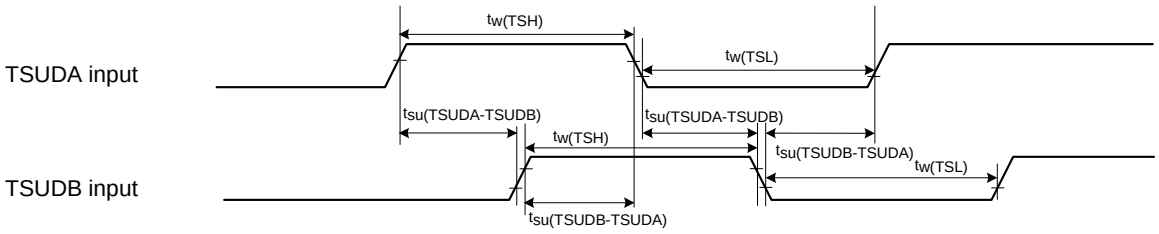
Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.3.2.5 Timer S Input

Table 5.41 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 5.20 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.