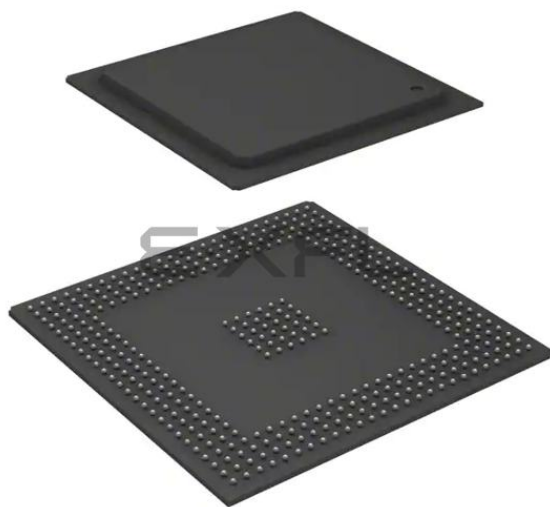




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Details

Product Status	Not For New Designs
Core Processor	Coldfire V4E
Core Size	32-Bit Single-Core
Speed	266MHz
Connectivity	EBI/EMI, Ethernet, I ² C, SPI, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	99
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5474vr266

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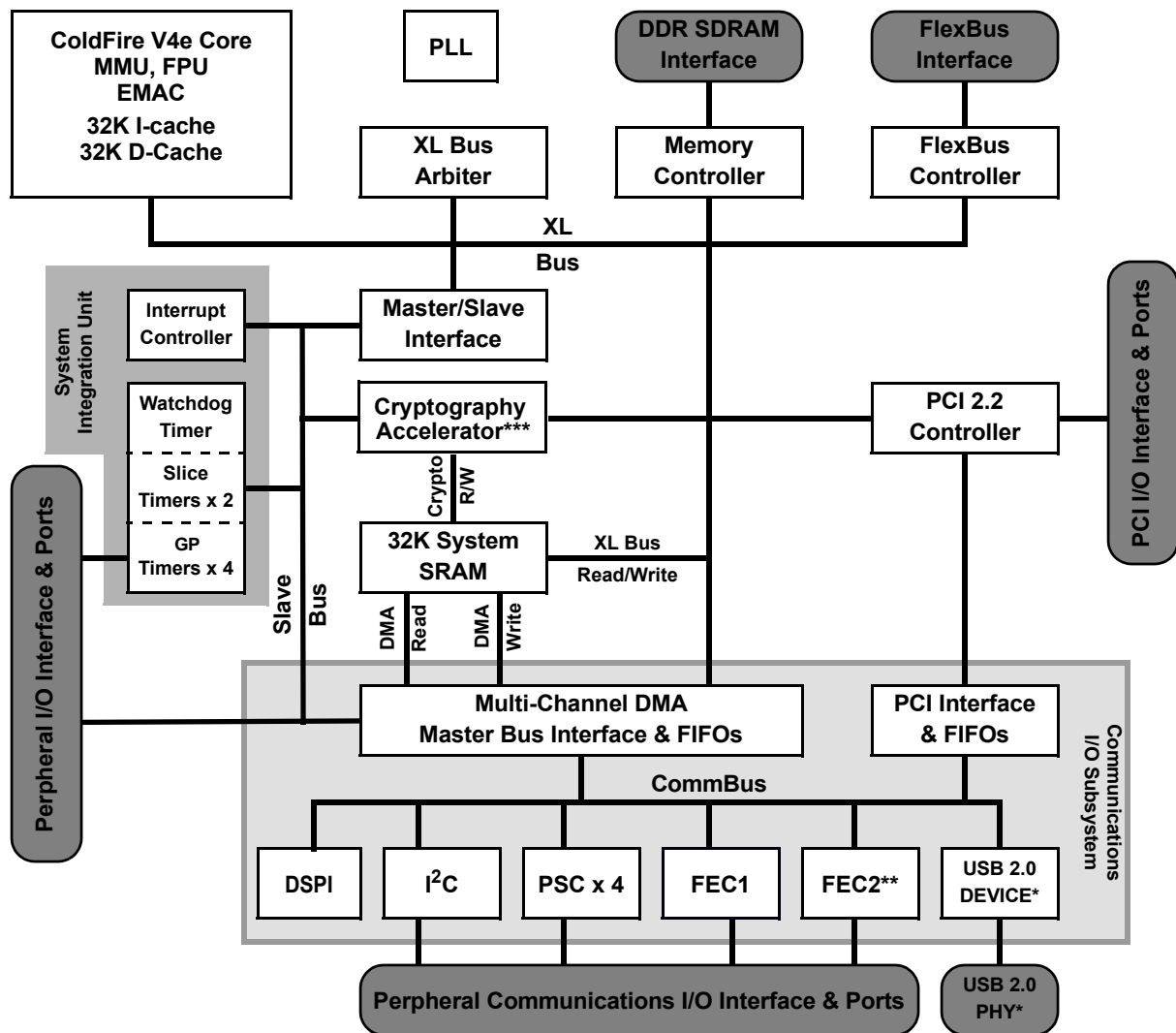


Figure 1. MCF547X Block Diagram

1 Maximum Ratings

Table 1 lists maximum and minimum ratings for supply and operating voltages and storage temperature. Operating outside of these ranges may cause erratic behavior or damage to the processor.

Table 1. Absolute Maximum Ratings

Rating	Symbol	Value	Units
External (I/O pads) supply voltage (3.3-V power pins)	EV _{DD}	−0.3 to +4.0	V
Internal logic supply voltage	IV _{DD}	−0.5 to +2.0	V
Memory (I/O pads) supply voltage (2.5-V power pins)	SD V _{DD}	−0.3 to +4.0 SDR Memory −0.3 to +2.8 DDR Memory	V
PLL supply voltage	PLL V _{DD}	−0.5 to +2.0	V
Internal logic supply voltage, input voltage level	V _{in}	−0.5 to +3.6	V
Storage temperature range	T _{stg}	−55 to +150	°C

2 Thermal Characteristics

2.1 Operating Temperatures

Table 2 lists junction and ambient operating temperatures.

Table 2. Operating Temperatures

Characteristic	Symbol	Value	Units
Maximum operating junction temperature	T _j	105	°C
Maximum operating ambient temperature	T _{Amax}	<70 ¹	°C
Minimum operating ambient temperature	T _{Amin}	−0	°C

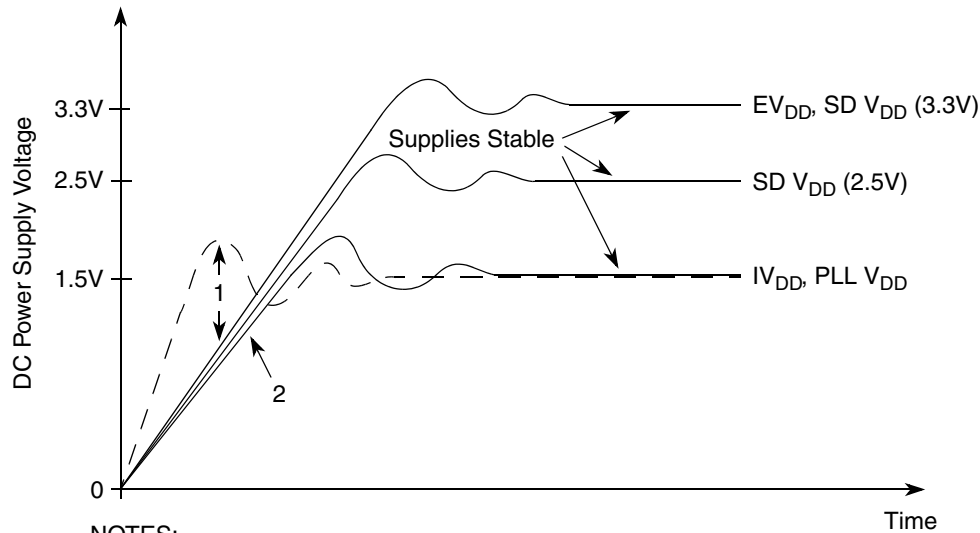
¹ This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.

2.2 Thermal Resistance

Table 3 lists thermal resistance values.

Table 3. Thermal Resistance

Characteristic		Symbol	Value	Unit
324 pin TEPBGA — Junction to ambient, natural convection	Four layer board (2s2p)	θ _{JMA}	20–22 ^{1,2}	°CW
388 pin TEPBGA — Junction to ambient, natural convection	Four layer board (2s2p)	θ _{JMA}	19 ^{1,2}	°CW



NOTES:

1. IVDD should not exceed EVDD or SD VDD by more than 0.4V at any time, including power-up.
2. Recommended that IVDD/PLL VDD should track EVDD/SD VDD up to 0.9V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (EVDD, SD VDD, IVDD, or PLL VDD) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

The relationship between SD VDD and EVDD is non-critical during power-up and power-down sequences. SD VDD (2.5V or 3.3V) and EVDD are specified relative to IVDD.

4.2.1 Power Up Sequence

If EVDD/SD VDD are powered up with the IVDD at 0V, the sense circuits in the I/O pads cause all pad output drivers connected to the EVDD/SD VDD to be in a high impedance state. There is no limit to how long after EVDD/SD VDD powers up before IVDD must power up. IVDD should not lead the EVDD, SD VDD, or PLL VDD by more than 0.4V during power ramp up or there is high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IVDD/PLL VDD and EVDD/SD VDD should track up to 0.9V, then separate for the completion of ramps with EVDD/SD VDD going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

4.2.2 Power Down Sequence

If IVDD/PLL VDD are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IVDD and PLL VDD power down before EVDD or SD VDD must power down. IVDD should not lag EVDD, SD VDD, or PLL VDD going low by more than 0.4V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IVDD/PLL VDD to 0V
2. Drop EVDD/SD VDD supplies

4.4 USB Power Filtering

To minimize noise, an external filter is required for each of the USB power pins. The filter shown in [Figure 6](#) should be connected between the board EV_{DD} or IV_{DD} and each of the USB V_{DD} pins.

- The resistor and capacitors should be placed as close to the dedicated USB V_{DD} pin as possible.
- A separate filter circuit should be included for each USB V_{DD} pin, a total of five circuits.
- All traces should be as low impedance as possible, especially ground pins to the ground plane.
- The filter for USB_PHYVDD to VSS should be connected to the power and ground planes, respectively, not fingers of the planes.
- In addition to keeping the filter components for the USB_PLLVDD as close as practical to the body of the processor as previously mentioned, special care should be taken to avoid coupling switching power supply noise or digital switching noise onto the portion of that supply between the filter and the processor.
- The capacitors for C2 in the table below should be rated X5R or better due to temperature performance.

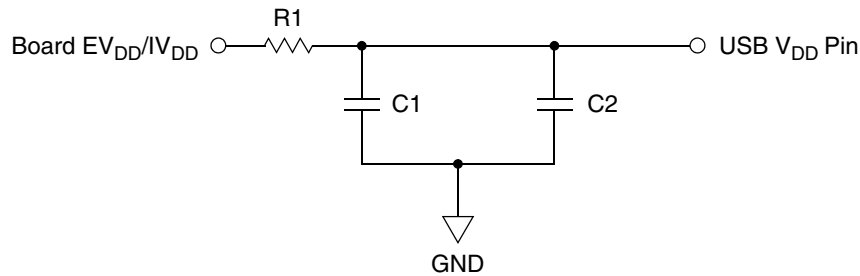


Figure 6. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

[Table 5](#) lists the resistor values and supply voltages to be used in the circuit for each of the USB V_{DD} pins.

Table 5. USB Filter Circuit Values

USB V_{DD} Pin	Nominal Voltage	R1 (Ω)	C1 (μ F)	C2 (μ F)
USBVDD (Bias generator supply)	3.3V	10	10	0.1
USB_PHYVDD (Main transceiver supply)	3.3V	0	10	0.1
USB_PLLVDD (PLL supply)	1.5V	10	1	0.1
USB_OSCVDD (Oscillator supply)	3.3V	0	10	0.1
USB_OSCAVDD (Oscillator analog supply)	1.5V	0	10	0.1

4.4.1 Bias Resistor

The USBRBIAS resistor should be placed as close to the dedicated USB 2.0 pins as possible. The tolerance should be $\pm 1\%$.

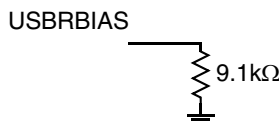


Figure 7. USBRBIAS Connection

5 Output Driver Capability and Loading

Table 6 lists values for drive capability and output loading.

Table 6. I/O Driver Capability¹

Signal	Drive Capability	Output Load (C_L)
SDRAMC (SDADDR[12:0], SDDATA[31:0], $\overline{RAS}$, $\overline{CAS}$, SDDM[3:0], $\overline{SDWE}$, SDBA[1:0])	24 mA	15 pF
SDRAMC DQS and clocks (SDDQS[3:0], SDRDQS, SDCLK[1:0], $\overline{SDCLK}$ [1:0], SDCKE)	24 mA	15 pF
SDRAMC chip selects ($\overline{SDCS}$ [3:0])	24 mA	15 pF
FlexBus (AD[31:0], $\overline{FBCS}$ [5:0], ALE, $\overline{R/W}$, $\overline{BE/BWE}$ [3:0], $\overline{OE}$)	16 mA	30 pF
FEC (EnMDIO, EnMDC, EnTXEN, EnTXD[3:0], EnTXER)	8 mA	15 pF
Timer (TOUT[3:0])	8 mA	50 pF
$\overline{DACK}$ [1:0]	8 mA	30 pF
PSC (PSCnTXD[3:0], $\overline{PSCnRTS}$ /PSCnFSYNC,	8 mA	30 pF
DSPI (DSPISOUT, DSPICS0/SS, DSPICS[2:3], DSPICS5/PCSS)	24 mA	50 pF
PCI (PCIAD[31:0], PCIBG[4:1], PCIBG0/PCIREQOUT, PCIDEVSEL, PCICXBE[3:0], PCIFRM, PCIPERR, PCIRESET, PCISERR, PCISTOP, PCIPAR, PCITRDY, PCIIRDY)	16 mA	50 pF
I2C (SCL, SDA)	8 mA	50 pF
BDM (PSTCLK, PSTDDATA[7:0], DSO/TDO,	8 mA	25 pF
RSTO	8 mA	50 pF

¹ The device's pads have balanced sink and source current. The drive capability is the same as the sink capability.

6 PLL Timing Specifications

The specifications in Table 7 are for the CLKIN pin.

Table 7. Clock Timing Specifications

Num	Characteristic	Min	Max	Units
C1	Cycle time	15.0	40	ns
C2	Rise time (20% of Vdd to 80% of vdd)	—	2	ns
C3	Fall time (80% of Vdd to 20% of Vdd)	—	2	ns
C4	Duty cycle (at 50% of Vdd)	40	60	%

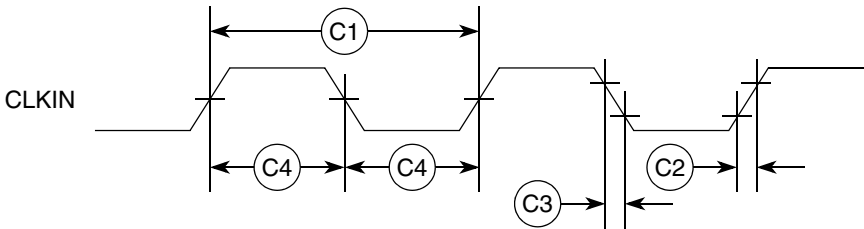


Figure 8. Input Clock Timing Diagram

Table 8 shows the supported PLL encodings.

Table 8. MCF547x Divide Ratio Encodings

AD[12:8] ¹	Clock Ratio	CLKIN—PCI and FlexBus Frequency Range (MHz)	Internal XLB, SDRAM Bus, and PSTCLK Frequency Range (MHz)	Core Frequency Range (MHz)
00011	1:2	41.67–66.66	83.33–133.33	166.66–266.66
00101	1:2	25.0–44.42	50.0–88.83 ²	100.0–177.66
01111	1:4	25.0–33.3	100–133.33	200–266.66

¹ All other values of AD[12:8] are reserved.

² DDR memories typically have a minimum speed of 83 MHz. Some vendors specify down to 75 MHz. Check with the memory component specifications to verify.

Figure 9 correlates CLKIN, internal bus, and core clock frequencies for the 1x–4x multipliers.

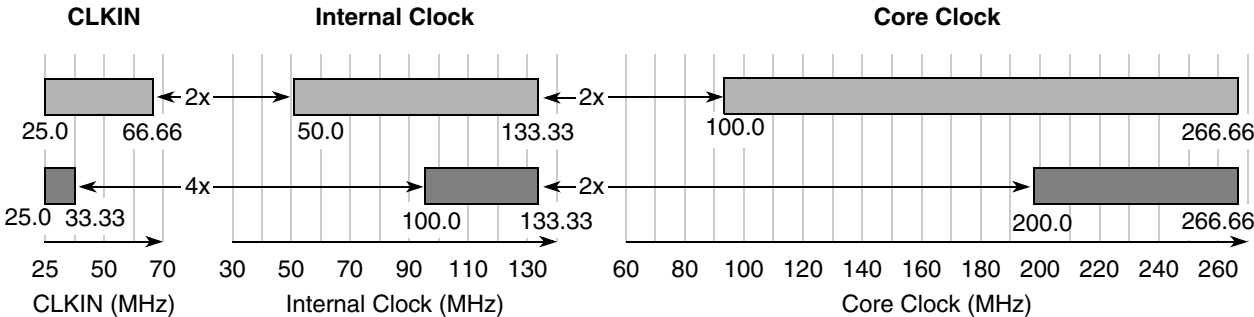


Figure 9. CLKIN, Internal Bus, and Core Clock Ratios

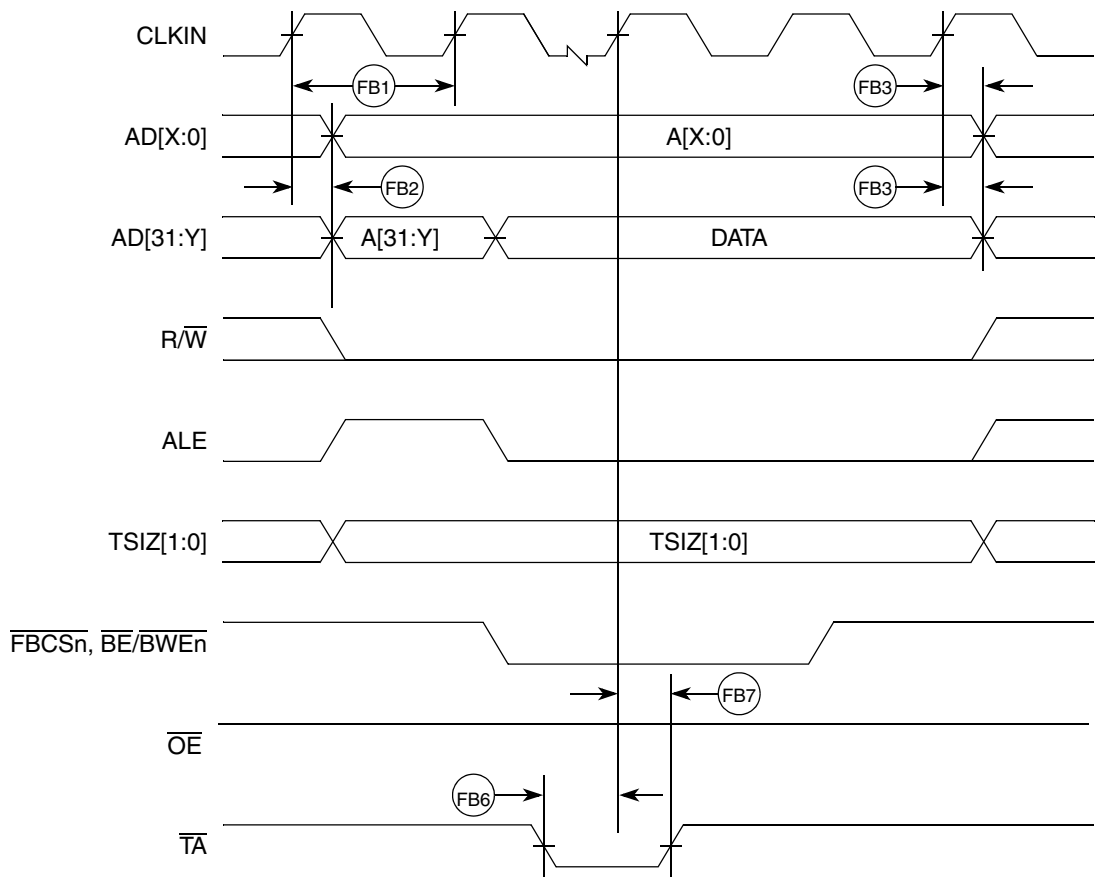


Figure 12. FlexBus Write Timing

9 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time. The SDRAM controller uses SSTL2 and SSTL3 I/O drivers. Both SSTL drive modes are programmable for Class I or Class II drive strength.

9.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SDR_DQS on read cycles. The MCF547x SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must be supplied to the MCF547x for each data beat of an SDR read. The MCF547x accomplishes this by asserting a signal called SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SDR_DQS signal and its usage.

9.2 DDR SDRAM AC Timing Characteristics

When using the DDR SDRAM controller, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 12 shows the DDR clock crossover specifications.

Table 12. DDR Clock Crossover Specifications

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	-0.3	SD_VDD + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SD_VDD + 0.6	V
V_{IX}	Clock crossing point voltage ¹	1.05	1.45	V

¹ The clock crossover voltage is only guaranteed when using the highest drive strength option for the SDCLK[1:0] and SDCLK[1:0] signals.

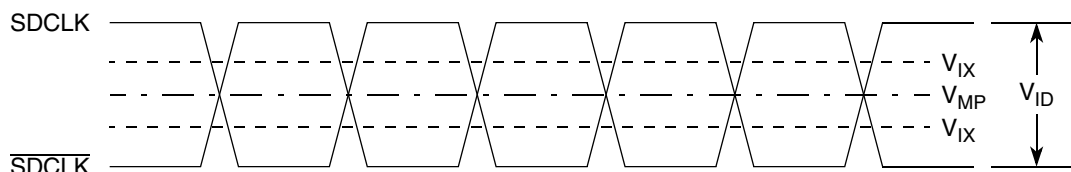


Figure 15. DDR Clock Timing Diagram

Table 13. DDR Timing Specifications

Symbol	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	50 ¹	133	MHz	²
DD1	Clock Period (t_{CK})	7.52	12	ns	³
DD2	Pulse Width High (t_{CKH})	0.45	0.55	SDCLK	⁴
DD3	Pulse Width Low (t_{CKL})	0.45	0.55	SDCLK	⁵
DD4	Address, SDCKE, $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$, SDBA, $\overline{SDCS}$ —Output Valid (t_{CMV})	—	$0.5 \times \text{SDCLK} + 1.0 \text{ ns}$	ns	⁶
DD5	Address, SDCKE, $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$, SDBA, $\overline{SDCS}$ —Output Hold (t_{CMH})	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition (t_{DQSS})	—	1.25	SDCLK	
DD7	Data and Data Mask Output Setup (DQ→DQS) Relative to DQS (DDR Write Mode) (t_{QS})	1.0	—	ns	⁷ ⁸
DD8	Data and Data Mask Output Hold (DQS→DQ) Relative to DQS (DDR Write Mode) (t_{QH})	1.0	—	ns	⁹
DD9	Input Data Skew Relative to DQS (Input Setup) (t_{IS})		1	ns	¹⁰
DD10	Input Data Hold Relative to DQS (t_{IH})	$0.25 \times \text{SDCLK} + 0.5 \text{ ns}$	—	ns	¹¹
DD11	DQS falling edge to SDCLK rising (output setup time) (t_{DSS})	0.5	—	ns	
DD12	DQS falling edge from SDCLK rising (output hold time) (t_{DSH})	0.5	—	ns	

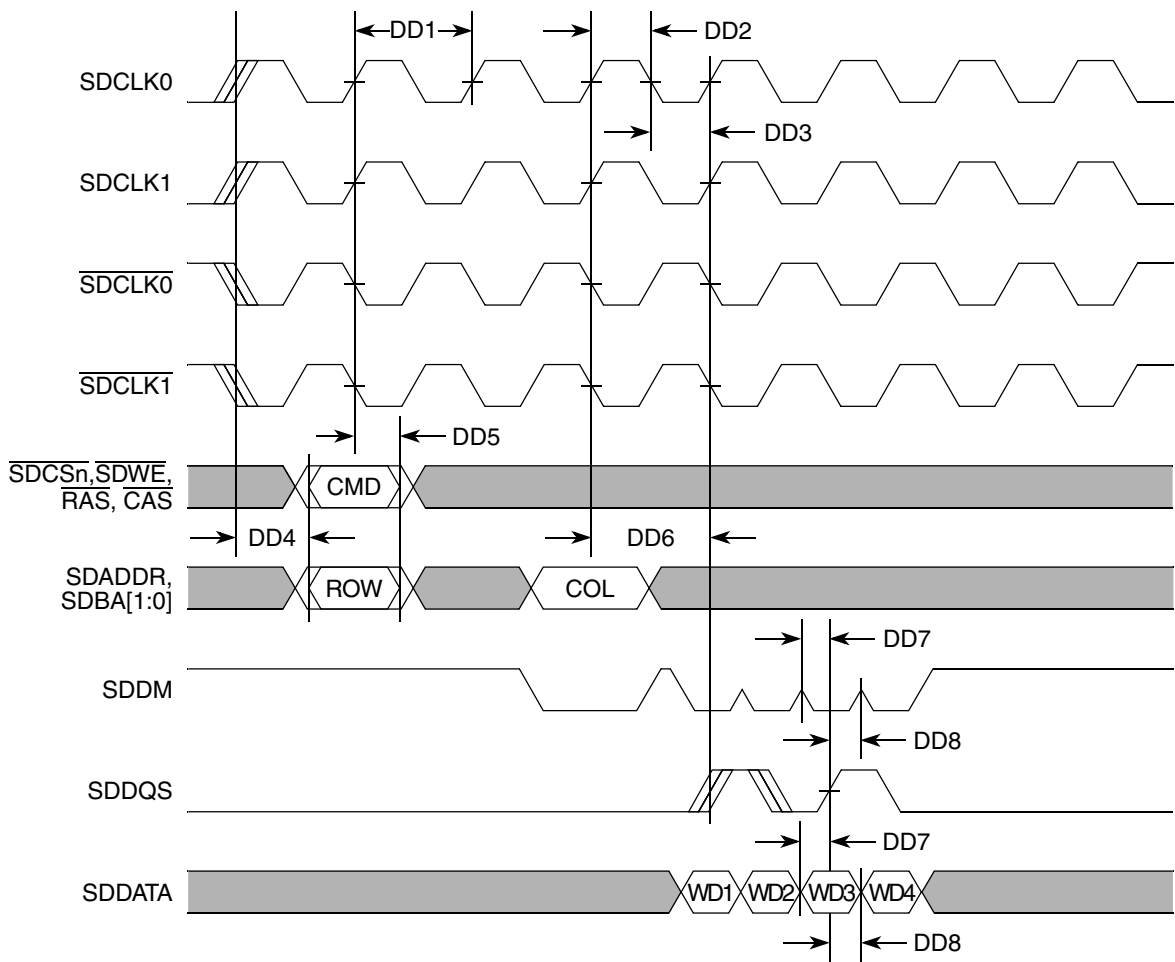


Figure 16. DDR Write Timing

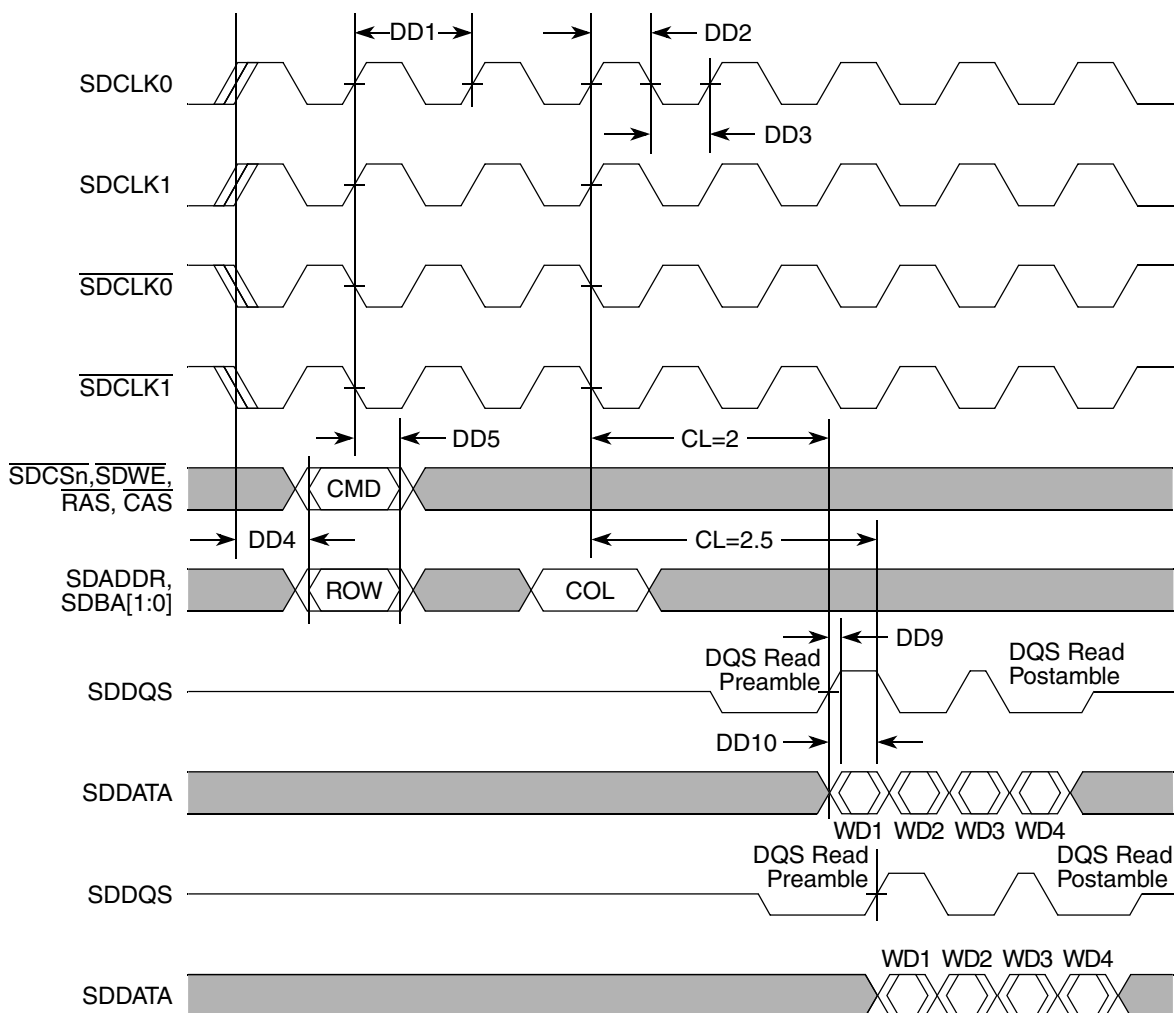


Figure 17. DDR Read Timing

10 PCI Bus

The PCI bus on the MCF547x is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Please refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	66	MHz	¹
P1	Clock Period (t_{CK})	15.15	40	ns	²
P2	Address, Data, and Command ($33 < \text{PCI} \leq 66 \text{ Mhz}$)—Input Setup (t_{IS})	3.0	—	ns	
P3	Address, Data, and Command ($0 < \text{PCI} \leq 33 \text{ Mhz}$)—Input Setup (t_{IS})	7.0	—	ns	
P4	Address, Data, and Command ($33\text{--}66 \text{ Mhz}$)—Output Valid (t_{DV})	—	6.0	ns	³
P5	Address, Data, and Command ($0\text{--}33 \text{ Mhz}$) - Output Valid (t_{DV})	—	11.0	ns	
P6	PCI signals ($0\text{--}66 \text{ Mhz}$) - Output Hold (t_{DH})	0	—	ns	⁴

Table 15. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
M2	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
M3	RXCLK pulse width high	35%	65%	RXCLK period
M4	RXCLK pulse width low	35%	65%	RXCLK period

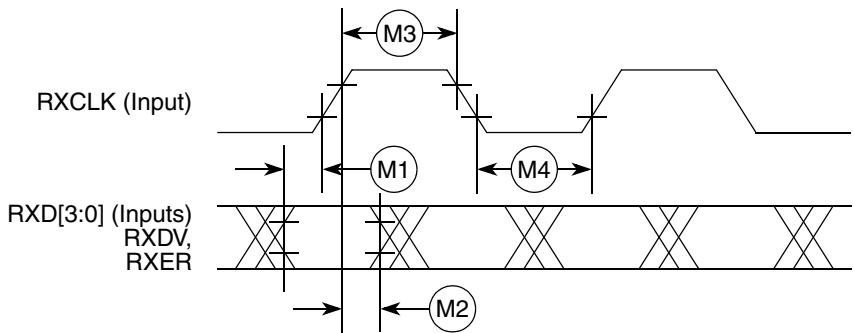


Figure 19. MII Receive Signal Timing Diagram

11.2 MII Transmit Signal Timing

Table 16. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	TXCLK to TXD[3:0], TXEN, TXER invalid	0	—	ns
M6	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns
M7	TXCLK pulse width high	35%	65%	TXCLK period
M8	TXCLK pulse width low	35%	65%	TXCLK period

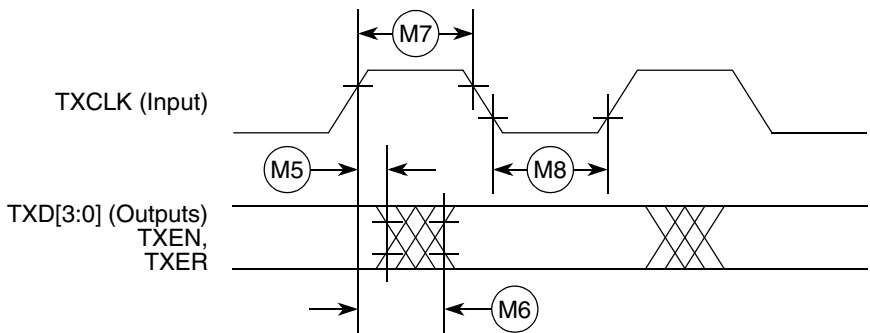


Figure 20. MII Transmit Signal Timing Diagram

11.3 MII Async Inputs Signal Timing (CRS, COL)

Table 17. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

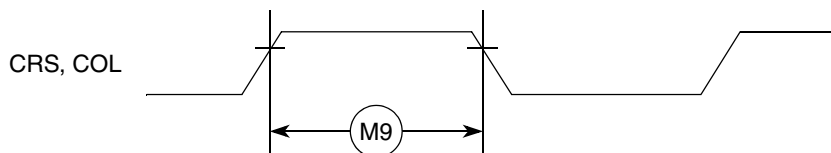


Figure 21. MII Async Inputs Timing Diagram

11.4 MII Serial Management Channel Timing (MDIO,MDC)

Table 18. MII Serial Management Channel Signal Timing

Num	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (min prop delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

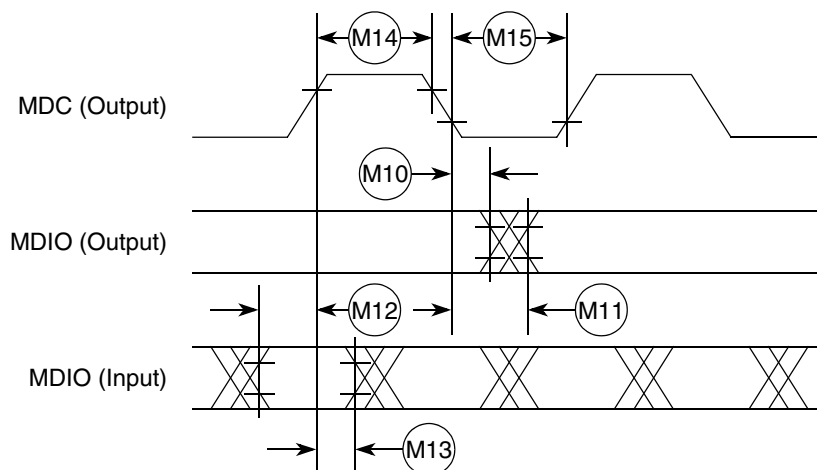


Figure 22. MII Serial Management Channel Timing Diagram

12 General Timing Specifications

Table 19 lists timing specifications for the GPIO, PSC, $\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and external interrupts.

Table 19. General AC Timing Specifications

Name	Characteristic	Min	Max	Unit
G1	CLKIN high to signal output valid	—	2	PSTCLK
G2	CLKIN high to signal invalid (output hold)	0	—	ns
G3	Signal input pulse width	2	—	PSTCLK

13 I²C Input/Output Timing Specifications

Table 20 lists specifications for the I²C input timing parameters shown in Figure 23.

Table 20. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	Bus clocks
I2	Clock low period	8	—	Bus clocks
I3	SCL/SDA rise time ($V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$)	—	1	mS
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time ($V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$)	—	1	mS
I6	Clock high time	4	—	Bus clocks
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	Bus clocks
I9	Stop condition setup time	2	—	Bus clocks

Table 21 lists specifications for the I²C output timing parameters shown in Figure 23.

Table 21. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1 ¹	Start condition hold time	6	—	Bus clocks
I2 ¹	Clock low period	10	—	Bus clocks
I3 ²	SCL/SDA rise time ($V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$)	—	—	μS
I4 ¹	Data hold time	7	—	Bus clocks
I5 ³	SCL/SDA fall time ($V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$)	—	3	ns
I6 ¹	Clock high time	10	—	Bus clocks
I7 ¹	Data setup time	2	—	Bus clocks
I8 ¹	Start condition setup time (for repeated start condition only)	20	—	Bus clocks
I9 ¹	Stop condition setup time	10	—	Bus clocks

- ¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 21. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 21 are minimum values.
- ² Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
- ³ Specified at a nominal 50-pF load.

Figure 23 shows timing for the values in Table 20 and Table 21.

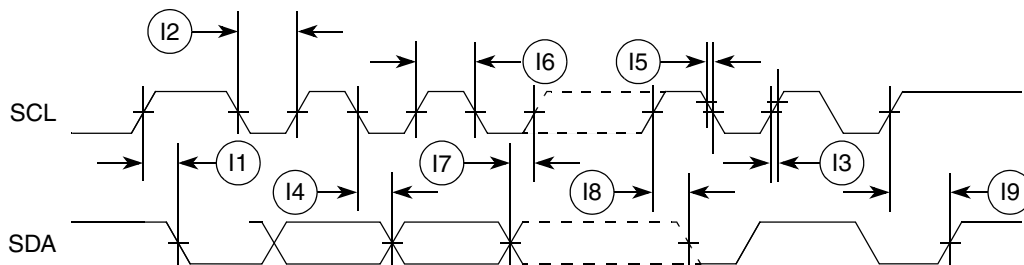


Figure 23. I²C Input/Output Timings

14 JTAG and Boundary Scan Timing

Table 22. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f _{JCYC}	DC	10	MHz
J2	TCLK Cycle Period	t _{JCYC}	2	—	t _{CK}
J3	TCLK Clock Pulse Width	t _{JCW}	15.15	—	ns
J4	TCLK Rise and Fall Times	t _{JCRF}	0.0	3.0	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t _{BSDST}	5.0	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t _{BSDHT}	24.0	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t _{BSDV}	0.0	15.0	ns
J8	TCLK Low to Boundary Scan Output High Z	t _{BSDZ}	0.0	15.0	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t _{TAPBST}	5.0	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t _{TAPBHT}	10.0	—	ns
J11	TCLK Low to TDO Data Valid	t _{TDODV}	0.0	20.0	ns
J12	TCLK Low to TDO High Z	t _{TDODZ}	0.0	15.0	ns
J13	$\overline{\text{TRST}}$ Assert Time	t _{TRSTAT}	100.0	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t _{TRSTST}	10.0	—	ns

¹ MTMOD is expected to be a static signal. Hence, it is not associated with any timing

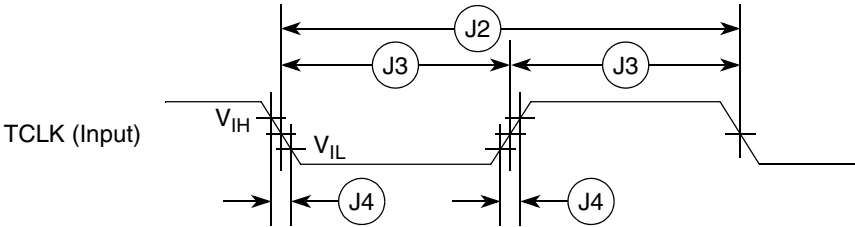


Figure 24. Test Clock Input Timing

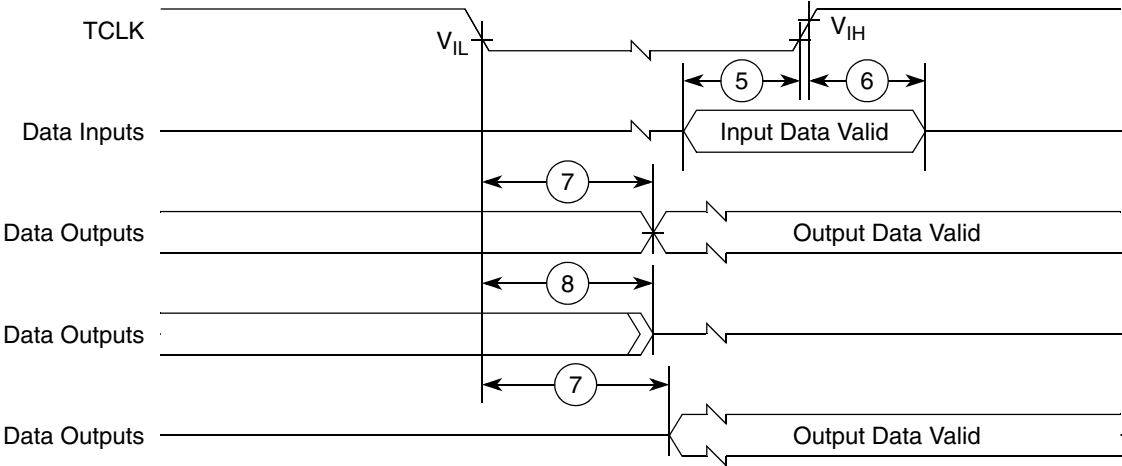


Figure 25. Boundary Scan (JTAG) Timing

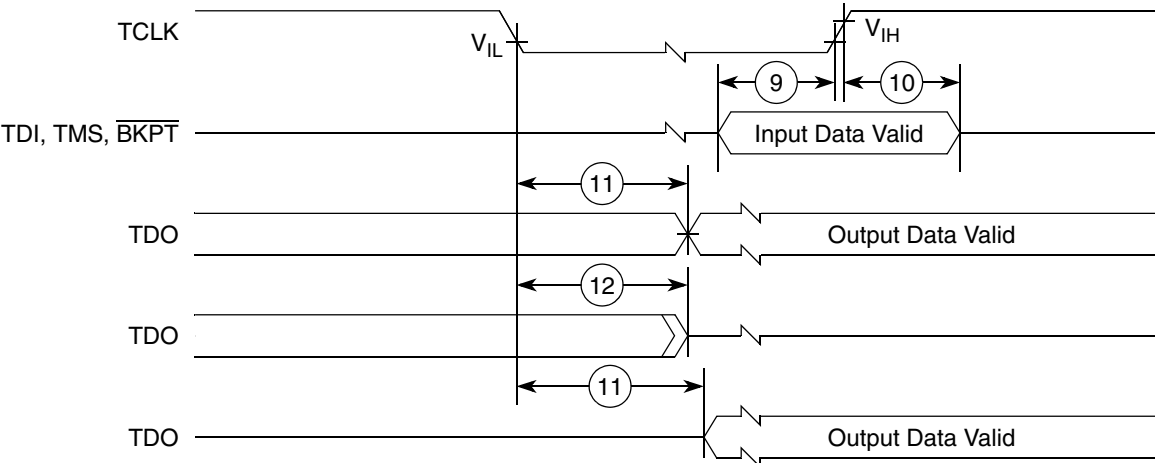


Figure 26. Test Access Port Timing

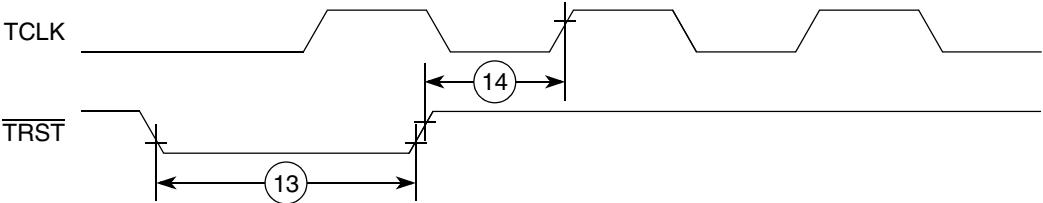


Figure 27. TRST Timing Debug AC Timing Specifications

Table 23 lists specifications for the debug AC timing parameters shown in Figure 29.

Table 23. Debug AC Timing Specifications

Num	Characteristic	66 MHz		Units
		Min	Max	
D1	PSTDDATA to PSTCLK setup	4.5	—	ns
D2	PSTCLK to PSTDDATA hold	4.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLKs
D4 ¹	DSCLK-to-DSO hold	4	—	PSTCLKs
D5	DSCLK cycle time	5	—	PSTCLKs

¹ DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 23.

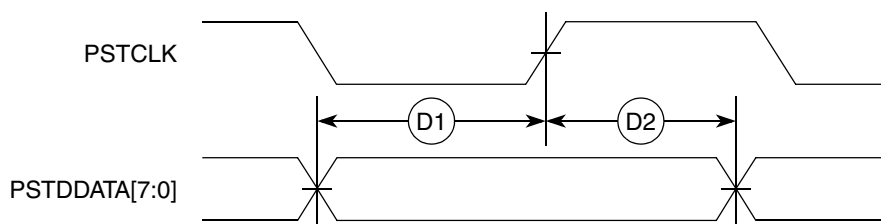


Figure 28. Real-Time Trace AC Timing

Figure 29 shows BDM serial port AC timing for the values in Table 23.

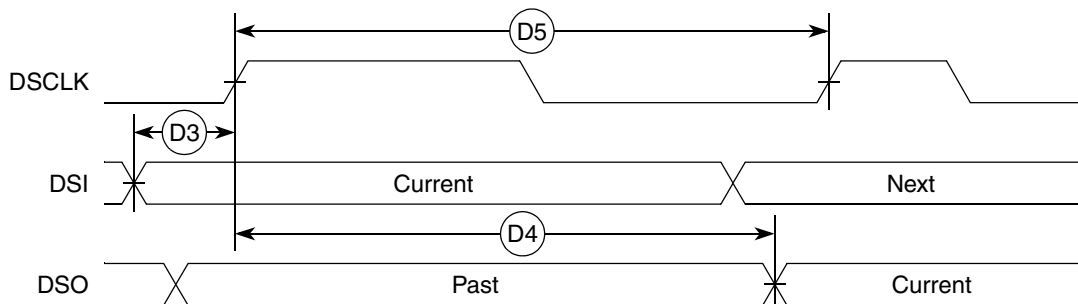
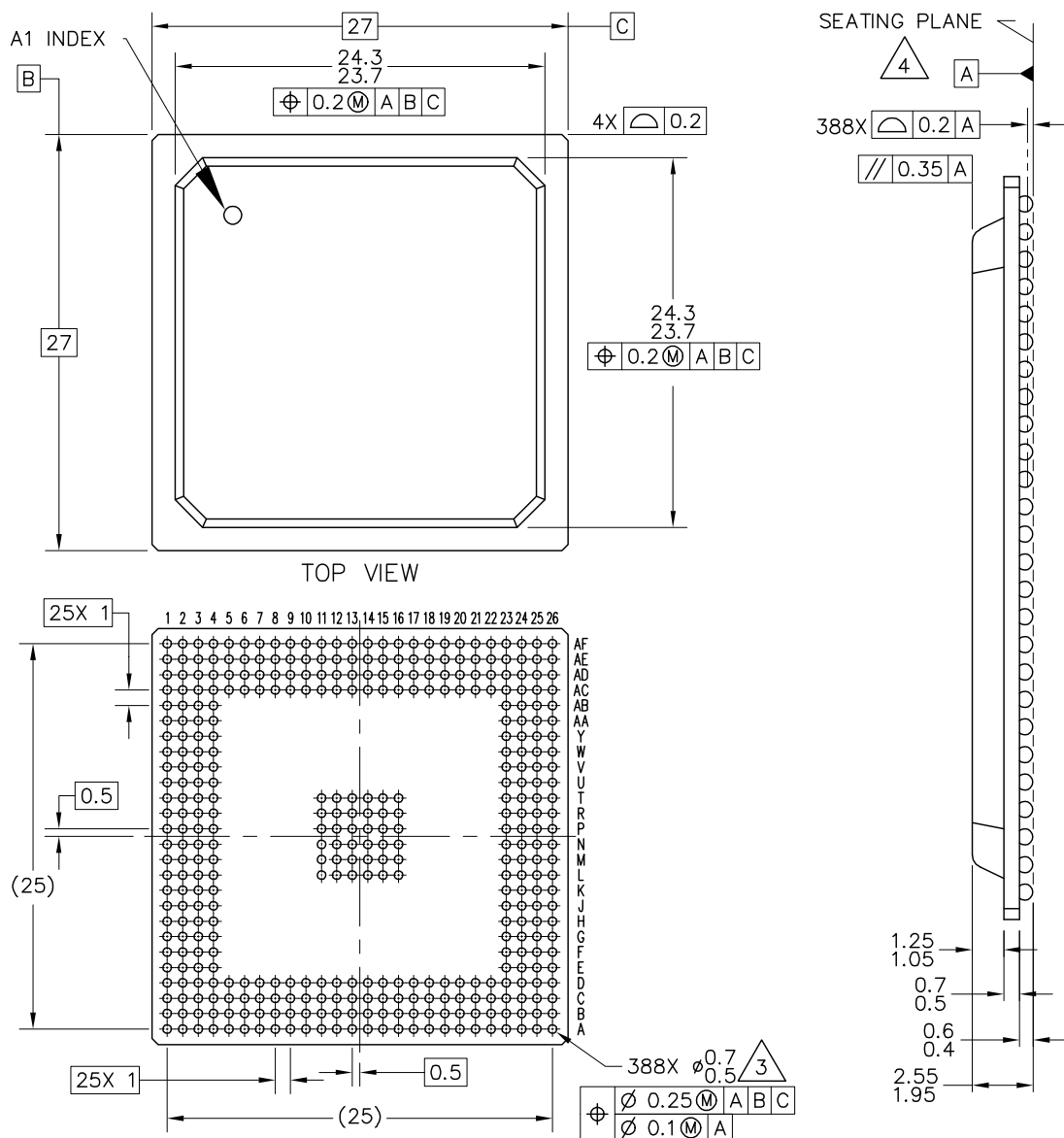


Figure 29. BDM Serial Port AC Timing

17 Case Drawing



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TITLE: 388 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)				DOCUMENT NO: 98ARS23880W			REV: C		
				CASE NUMBER: 1164-02			25 JAN 2007		
				STANDARD: JEDEC MS-034 AAL-1					

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