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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	Coldfire V4E
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I ² C, SPI, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	99
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5475vr200

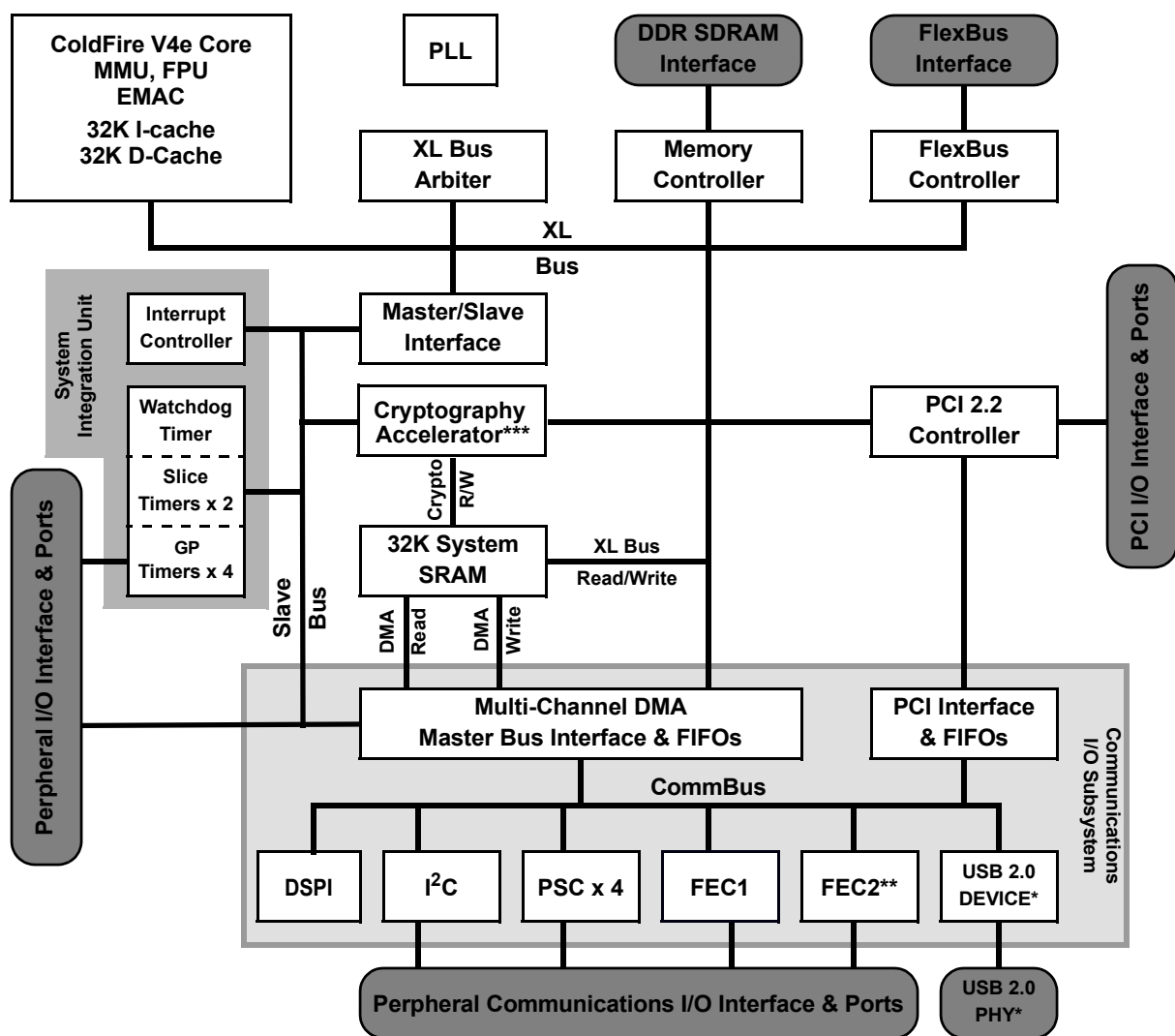


Figure 1. MCF547X Block Diagram

1 Maximum Ratings

Table 1 lists maximum and minimum ratings for supply and operating voltages and storage temperature. Operating outside of these ranges may cause erratic behavior or damage to the processor.

Table 1. Absolute Maximum Ratings

Rating	Symbol	Value	Units
External (I/O pads) supply voltage (3.3-V power pins)	EV _{DD}	−0.3 to +4.0	V
Internal logic supply voltage	IV _{DD}	−0.5 to +2.0	V
Memory (I/O pads) supply voltage (2.5-V power pins)	SD V _{DD}	−0.3 to +4.0 SDR Memory −0.3 to +2.8 DDR Memory	V
PLL supply voltage	PLL V _{DD}	−0.5 to +2.0	V
Internal logic supply voltage, input voltage level	V _{in}	−0.5 to +3.6	V
Storage temperature range	T _{stg}	−55 to +150	°C

2 Thermal Characteristics

2.1 Operating Temperatures

Table 2 lists junction and ambient operating temperatures.

Table 2. Operating Temperatures

Characteristic	Symbol	Value	Units
Maximum operating junction temperature	T _j	105	°C
Maximum operating ambient temperature	T _{Amax}	<70 ¹	°C
Minimum operating ambient temperature	T _{Amin}	−0	°C

¹ This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.

2.2 Thermal Resistance

Table 3 lists thermal resistance values.

Table 3. Thermal Resistance

Characteristic		Symbol	Value	Unit
324 pin TEPBGA — Junction to ambient, natural convection	Four layer board (2s2p)	θ _{JMA}	20–22 ^{1,2}	°CW
388 pin TEPBGA — Junction to ambient, natural convection	Four layer board (2s2p)	θ _{JMA}	19 ^{1,2}	°CW

Table 4. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Units
Output high voltage $I_{OH} = 8 \text{ mA}, 16 \text{ mA}, 24 \text{ mA}$	V_{OH}	2.4	—	V
Output low voltage $I_{OL} = 8 \text{ mA}, 16 \text{ mA}, 24 \text{ mA}^5$	V_{OL}	—	0.5	V
Capacitance ³ , $V_{in} = 0 \text{ V}$, $f = 1 \text{ MHz}$	C_{IN}	—	TBD	pF
Input leakage current	I_{in}	-1.0	1.0	μA

¹ IV_{DD} and PLL V_{DD} should be at the same voltage. PLL V_{DD} should have a filtered input. Please see [Figure 2](#) for an example circuit. There are three PLL V_{DD} inputs. A filter circuit should be used on each PLL V_{DD} input.

² This specification is guaranteed by design and is not 100% tested.

³ Capacitance C_{IN} is periodically sampled rather than 100% tested.

4 Hardware Design Considerations

4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in [Figure 2](#) should be connected between the board V_{DD} and the PLL V_{DD} pins. The resistor and capacitors should be placed as close to the dedicated PLL V_{DD} pin as possible.

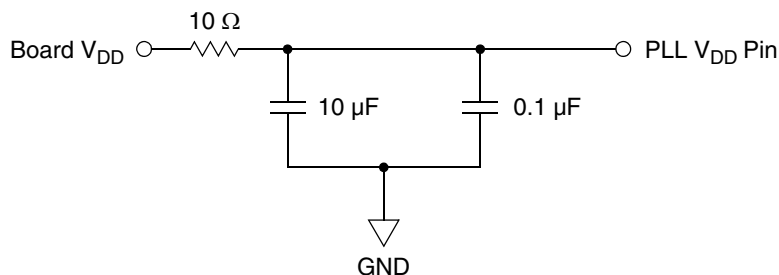
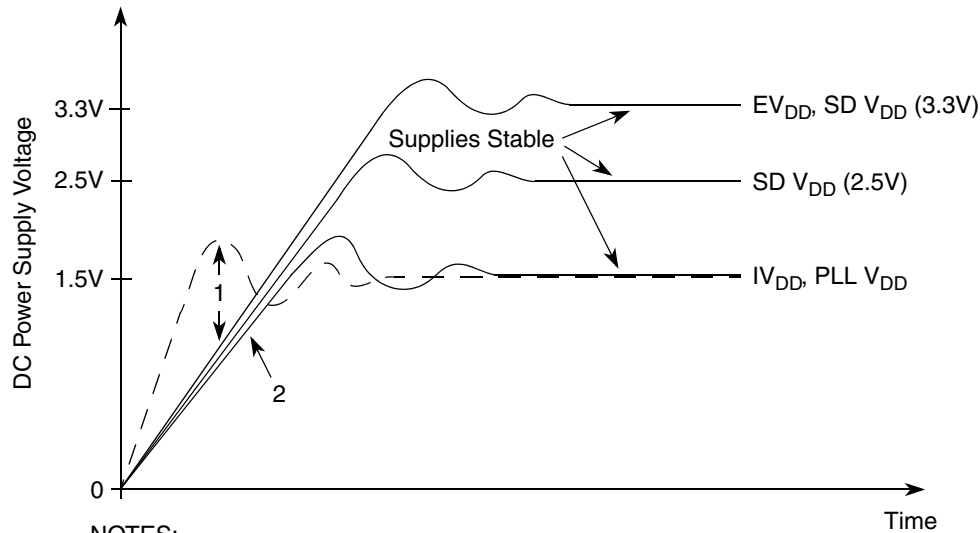


Figure 2. System PLL V_{DD} Power Filter

4.2 Supply Voltage Sequencing and Separation Cautions

[Figure 3](#) shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} ($SD V_{DD}$), PLL V_{DD} ($PLL V_{DD}$), and Core V_{DD} (IV_{DD}).



NOTES:

1. IV_{DD} should not exceed EV_{DD} or $SD V_{DD}$ by more than 0.4V at any time, including power-up.
2. Recommended that $IV_{DD}/PLL V_{DD}$ should track $EV_{DD}/SD V_{DD}$ up to 0.9V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (EV_{DD} , $SD V_{DD}$, IV_{DD} , or $PLL V_{DD}$) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

The relationship between $SD V_{DD}$ and EV_{DD} is non-critical during power-up and power-down sequences. $SD V_{DD}$ (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD} .

4.2.1 Power Up Sequence

If $EV_{DD}/SD V_{DD}$ are powered up with the IV_{DD} at 0V, the sense circuits in the I/O pads cause all pad output drivers connected to the $EV_{DD}/SD V_{DD}$ to be in a high impedance state. There is no limit to how long after $EV_{DD}/SD V_{DD}$ powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD} , $SD V_{DD}$, or $PLL V_{DD}$ by more than 0.4V during power ramp up or there is high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. $IV_{DD}/PLL V_{DD}$ and $EV_{DD}/SD V_{DD}$ should track up to 0.9V, then separate for the completion of ramps with $EV_{DD}/SD V_{DD}$ going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

4.2.2 Power Down Sequence

If $IV_{DD}/PLL V_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLL V_{DD}$ power down before EV_{DD} or $SD V_{DD}$ must power down. IV_{DD} should not lag EV_{DD} , $SD V_{DD}$, or $PLL V_{DD}$ going low by more than 0.4V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $IV_{DD}/PLL V_{DD}$ to 0V
2. Drop $EV_{DD}/SD V_{DD}$ supplies

4.3 General USB Layout Guidelines

4.3.1 USB D+ and D- High-Speed Traces

1. High speed clock and the USBD+ and USBD- differential pair should be routed first.
2. Route USBD+ and USBD- signals on the top layer of the board.
3. The trace width and spacing of the USBD+ and USBD- signals should be such that the differential impedance is 90Ω .
4. Route traces over continuous planes (power and ground)—they should not pass over any power/ground plane slots or anti-etch. When placing connectors, make sure the ground plane clear-outs around each pin have ground continuity between all pins.
5. Maintain the parallelism (skew matched) between USBD+ and USBD-. These traces should be the same overall length.
6. Do not route USBD+ and USBD- traces under oscillators or parallel to clock traces and/or data buses. Minimize the lengths of high speed signals that run parallel to the USBD+ and USBD- pair. Maintain a minimum 50mil spacing to clock signals.
7. Keep USBD+ and USBD- traces as short as possible.
8. Route USBD+, USBD-, and USBVBUS signals with a minimum amount of vias and corners. Use 45° turns.
9. Stubs should be avoided as much as possible. If they cannot be avoided, stubs should be no greater than 200mils.

4.3.2 USB VBUS Traces

Connecting the USBVBUS pin directly to the 5V VBUS signal from the USB connector can cause long-term reliability problems in the ESD network of the processor. Therefore, use of an external voltage divider for VBUS is recommended. [Figure 4](#) and [Figure 5](#) depict possible connections for VBUS. Point A, marked in each figure, is where a 5V version of VBUS should connect. Point B, marked in each figure, is where a 3.3V version of VBUS should connect to the USBVBUS pin on the device.

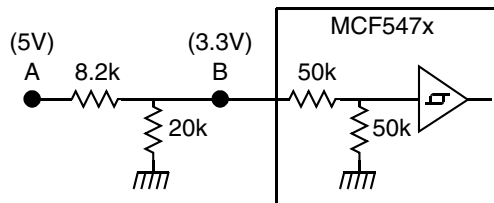


Figure 4. Preferred VBUS Connections

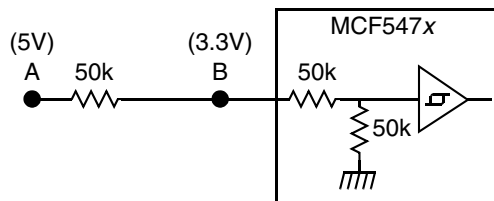


Figure 5. Alternate VBUS Connections

4.3.3 USB Receptacle Connections

It is recommended to connect the shield and the ground pin of the B USB receptacle for upstream ports to the board ground plane. The ground pin of the A USB receptacles for downstream ports should also be connected to the board ground plane, but industry practice varies widely on the connection of the shield of the A USB receptacles to other system grounds. Take precautions for control of ground loops between hosts and self-powered USB devices through the cable shield.

4.4 USB Power Filtering

To minimize noise, an external filter is required for each of the USB power pins. The filter shown in [Figure 6](#) should be connected between the board EV_{DD} or IV_{DD} and each of the USB V_{DD} pins.

- The resistor and capacitors should be placed as close to the dedicated USB V_{DD} pin as possible.
- A separate filter circuit should be included for each USB V_{DD} pin, a total of five circuits.
- All traces should be as low impedance as possible, especially ground pins to the ground plane.
- The filter for USB_PHYVDD to VSS should be connected to the power and ground planes, respectively, not fingers of the planes.
- In addition to keeping the filter components for the USB_PLLVDD as close as practical to the body of the processor as previously mentioned, special care should be taken to avoid coupling switching power supply noise or digital switching noise onto the portion of that supply between the filter and the processor.
- The capacitors for C2 in the table below should be rated X5R or better due to temperature performance.

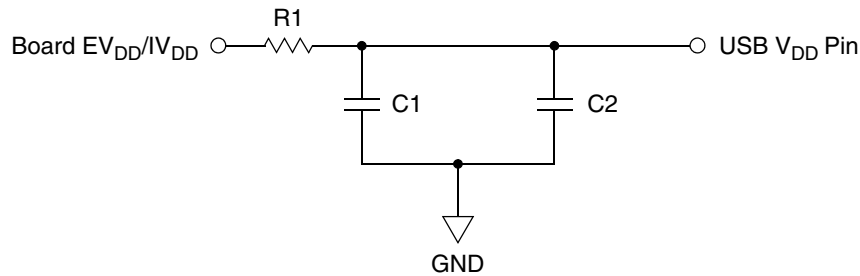


Figure 6. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

[Table 5](#) lists the resistor values and supply voltages to be used in the circuit for each of the USB V_{DD} pins.

Table 5. USB Filter Circuit Values

USB V_{DD} Pin	Nominal Voltage	R1 (Ω)	C1 (μ F)	C2 (μ F)
USBVDD (Bias generator supply)	3.3V	10	10	0.1
USB_PHYVDD (Main transceiver supply)	3.3V	0	10	0.1
USB_PLLVDD (PLL supply)	1.5V	10	1	0.1
USB_OSCVDD (Oscillator supply)	3.3V	0	10	0.1
USB_OSCAVDD (Oscillator analog supply)	1.5V	0	10	0.1

6 PLL Timing Specifications

The specifications in Table 7 are for the CLKIN pin.

Table 7. Clock Timing Specifications

Num	Characteristic	Min	Max	Units
C1	Cycle time	15.0	40	ns
C2	Rise time (20% of Vdd to 80% of vdd)	—	2	ns
C3	Fall time (80% of Vdd to 20% of Vdd)	—	2	ns
C4	Duty cycle (at 50% of Vdd)	40	60	%

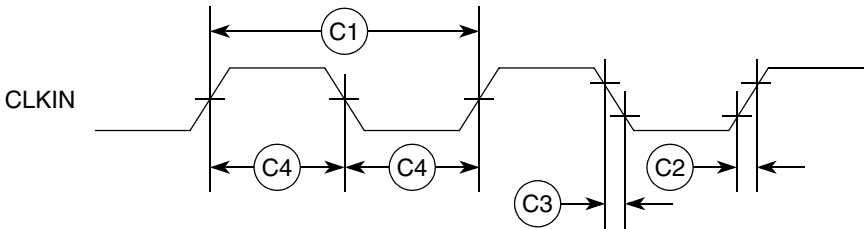


Figure 8. Input Clock Timing Diagram

Table 8 shows the supported PLL encodings.

Table 8. MCF547x Divide Ratio Encodings

AD[12:8] ¹	Clock Ratio	CLKIN—PCI and FlexBus Frequency Range (MHz)	Internal XLB, SDRAM Bus, and PSTCLK Frequency Range (MHz)	Core Frequency Range (MHz)
00011	1:2	41.67–66.66	83.33–133.33	166.66–266.66
00101	1:2	25.0–44.42	50.0–88.83 ²	100.0–177.66
01111	1:4	25.0–33.3	100–133.33	200–266.66

¹ All other values of AD[12:8] are reserved.

² DDR memories typically have a minimum speed of 83 MHz. Some vendors specify down to 75 MHz. Check with the memory component specifications to verify.

Figure 9 correlates CLKIN, internal bus, and core clock frequencies for the 1x–4x multipliers.

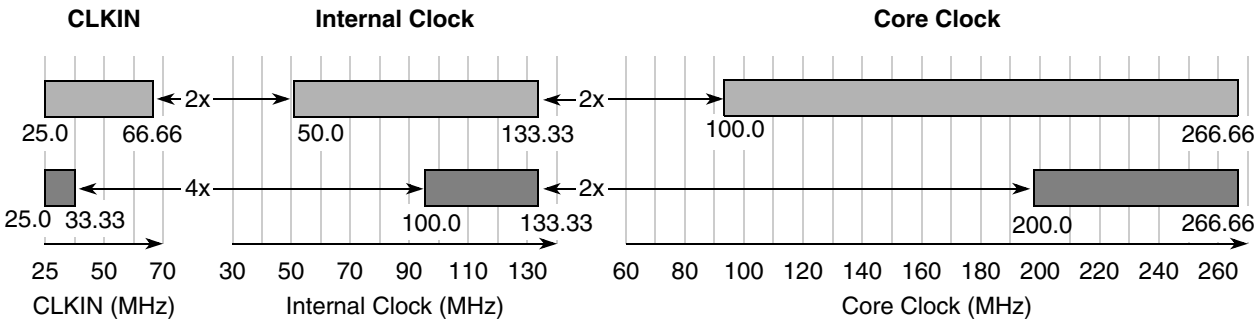


Figure 9. CLKIN, Internal Bus, and Core Clock Ratios

7 Reset Timing Specifications

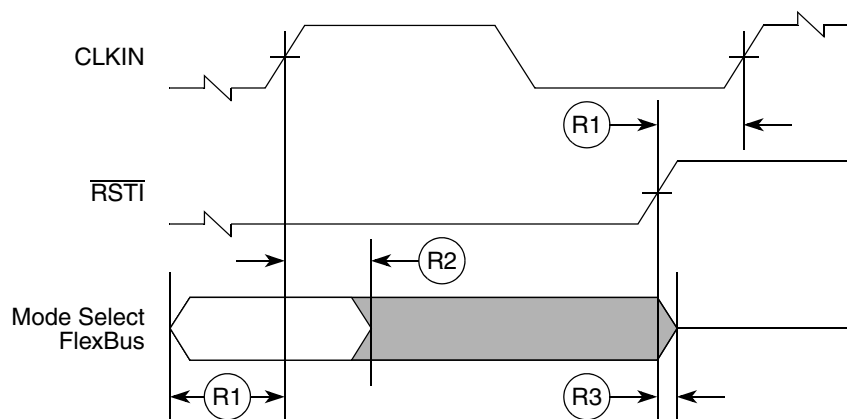
Table 9 lists specifications for the reset timing parameters shown in Figure 10

Table 9. Reset Timing Specifications

Num	Characteristic	66 MHz CLKIN		Units
		Min	Max	
R1 ¹	Valid to CLKIN (setup)	8	—	ns
R2	CLKIN to invalid (hold)	1.0	—	ns
R3	$\overline{\text{RSTI}}$ to invalid (hold)	1.0	—	ns
	$\overline{\text{RSTI}}$ pulse duration	5	—	CLKIN cycles

¹ $\overline{\text{RSTI}}$ and FlexBus data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

Figure 10 shows reset timing for the values in Table 9.



NOTE:

Mode selects are registered on the rising clock edge before the cycle in which $\overline{\text{RSTI}}$ is recognized as being negated.

Figure 10. Reset Timing

8 FlexBus

A multi-function external bus interface called FlexBus is provided on the MCF5472 with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FBCS}}[5:0]$). Chip-select $\overline{\text{FBCS0}}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM / flash memories.

8.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the system clock.

Table 10. FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	66	Mhz	¹
FB1	Clock Period (CLKIN)	15.15	40	ns	²
FB2	Address, Data, and Control Output Valid (AD[31:0], $\overline{\text{FBCS}}[5:0]$, R/W, ALE, TSIZ[1:0], $\overline{\text{BE}}/\text{BWE}[3:0]$, $\overline{\text{OE}}$, and $\overline{\text{TBST}}$)	—	7.0	ns	³
FB3	Address, Data, and Control Output Hold ((AD[31:0], $\overline{\text{FBCS}}[5:0]$, R/W, ALE, TSIZ[1:0], $\overline{\text{BE}}/\text{BWE}[3:0]$, $\overline{\text{OE}}$, and $\overline{\text{TBST}}$)	1	—	ns	^{3, 4}
FB4	Data Input Setup	3.5	—	ns	
FB5	Data Input Hold	0	—	ns	
FB6	Transfer Acknowledge ($\overline{\text{TA}}$) Input Setup	4	—	ns	
FB7	Transfer Acknowledge ($\overline{\text{TA}}$) Input Hold	0	—	ns	
FB8	Address Output Valid (PCIAD[31:0])	—	7.0	ns	⁵
FB9	Address Output Hold (PCIAD[31:0])	0	—	ns	⁵

¹ The frequency of operation is the same as the PCI frequency of operation. The MCF547X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI.

² Max cycle rate is determined by CLKIN and how the user has the system PLL configured.

³ Timing for chip selects only applies to the $\overline{\text{FBCS}}[5:0]$ signals. Please see [Section 9.2, “DDR SDRAM AC Timing Characteristics”](#) for SDCS[3:0] timing.

⁴ The FlexBus supports programming an extension of the address hold. Please consult the MCF547X specification manual for more information.

⁵ These specs are used when the PCIAD[31:0] signals are configured as 32-bit, non-muxed FlexBus address signals.

9.2 DDR SDRAM AC Timing Characteristics

When using the DDR SDRAM controller, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 12 shows the DDR clock crossover specifications.

Table 12. DDR Clock Crossover Specifications

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	-0.3	SD_VDD + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SD_VDD + 0.6	V
V_{IX}	Clock crossing point voltage ¹	1.05	1.45	V

¹ The clock crossover voltage is only guaranteed when using the highest drive strength option for the SDCLK[1:0] and SDCLK[1:0] signals.

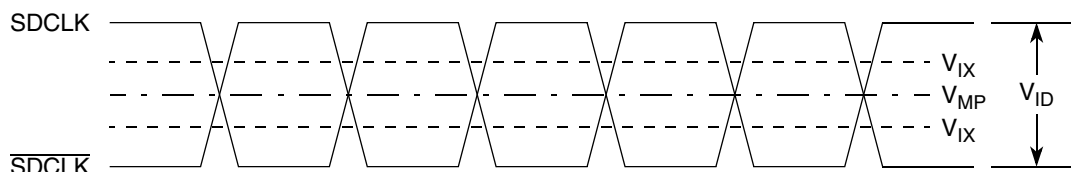


Figure 15. DDR Clock Timing Diagram

Table 13. DDR Timing Specifications

Symbol	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	50 ¹	133	MHz	²
DD1	Clock Period (t_{CK})	7.52	12	ns	³
DD2	Pulse Width High (t_{CKH})	0.45	0.55	SDCLK	⁴
DD3	Pulse Width Low (t_{CKL})	0.45	0.55	SDCLK	⁵
DD4	Address, SDCKE, \overline{CAS} , \overline{RAS} , \overline{WE} , SDBA, \overline{SDCS} —Output Valid (t_{CMV})	—	$0.5 \times \text{SDCLK} + 1.0 \text{ ns}$	ns	⁶
DD5	Address, SDCKE, \overline{CAS} , \overline{RAS} , \overline{WE} , SDBA, \overline{SDCS} —Output Hold (t_{CMH})	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition (t_{DQSS})	—	1.25	SDCLK	
DD7	Data and Data Mask Output Setup (DQ→DQS) Relative to DQS (DDR Write Mode) (t_{QS})	1.0	—	ns	⁷ ⁸
DD8	Data and Data Mask Output Hold (DQS→DQ) Relative to DQS (DDR Write Mode) (t_{QH})	1.0	—	ns	⁹
DD9	Input Data Skew Relative to DQS (Input Setup) (t_{IS})		1	ns	¹⁰
DD10	Input Data Hold Relative to DQS (t_{IH})	$0.25 \times \text{SDCLK} + 0.5 \text{ ns}$	—	ns	¹¹
DD11	DQS falling edge to SDCLK rising (output setup time) (t_{DSS})	0.5	—	ns	
DD12	DQS falling edge from SDCLK rising (output hold time) (t_{DSH})	0.5	—	ns	

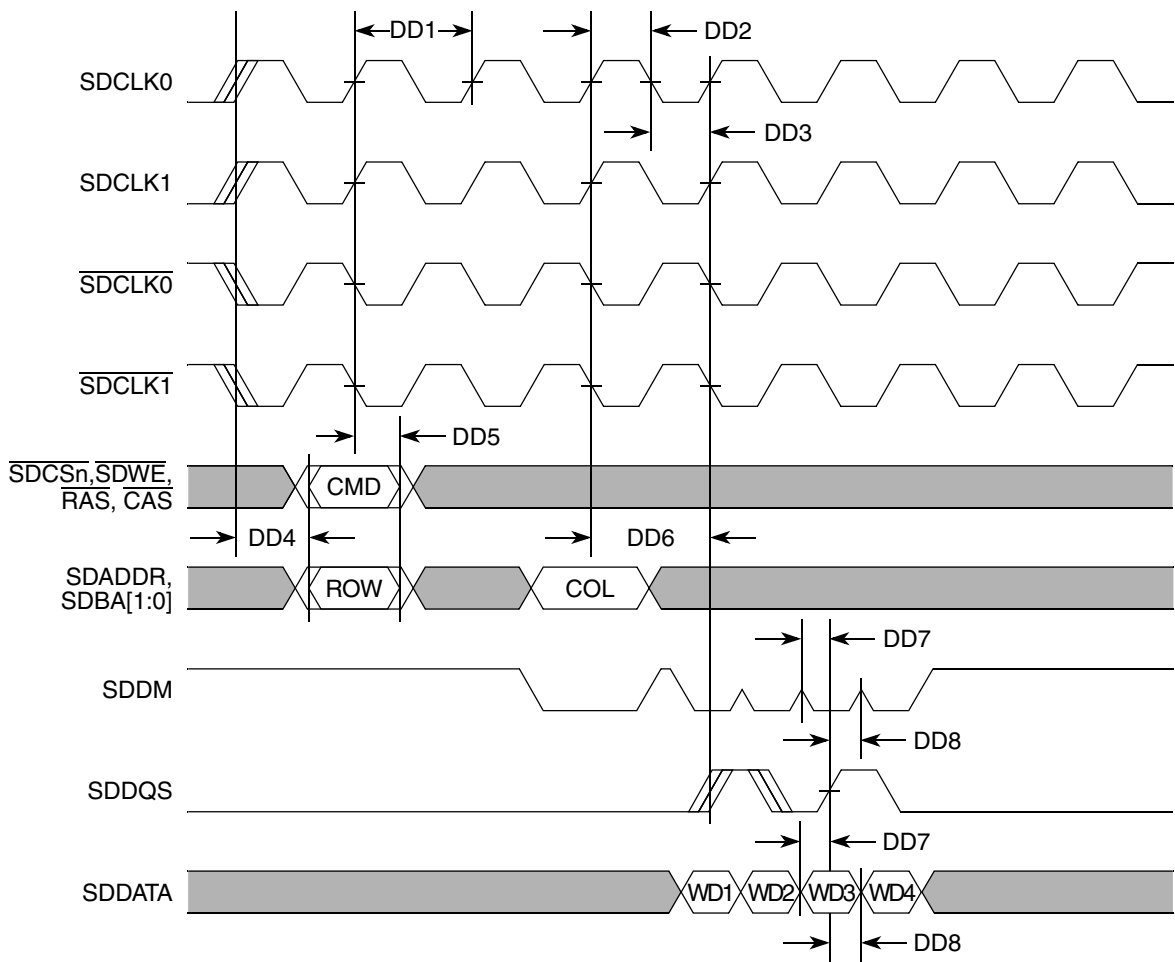


Figure 16. DDR Write Timing

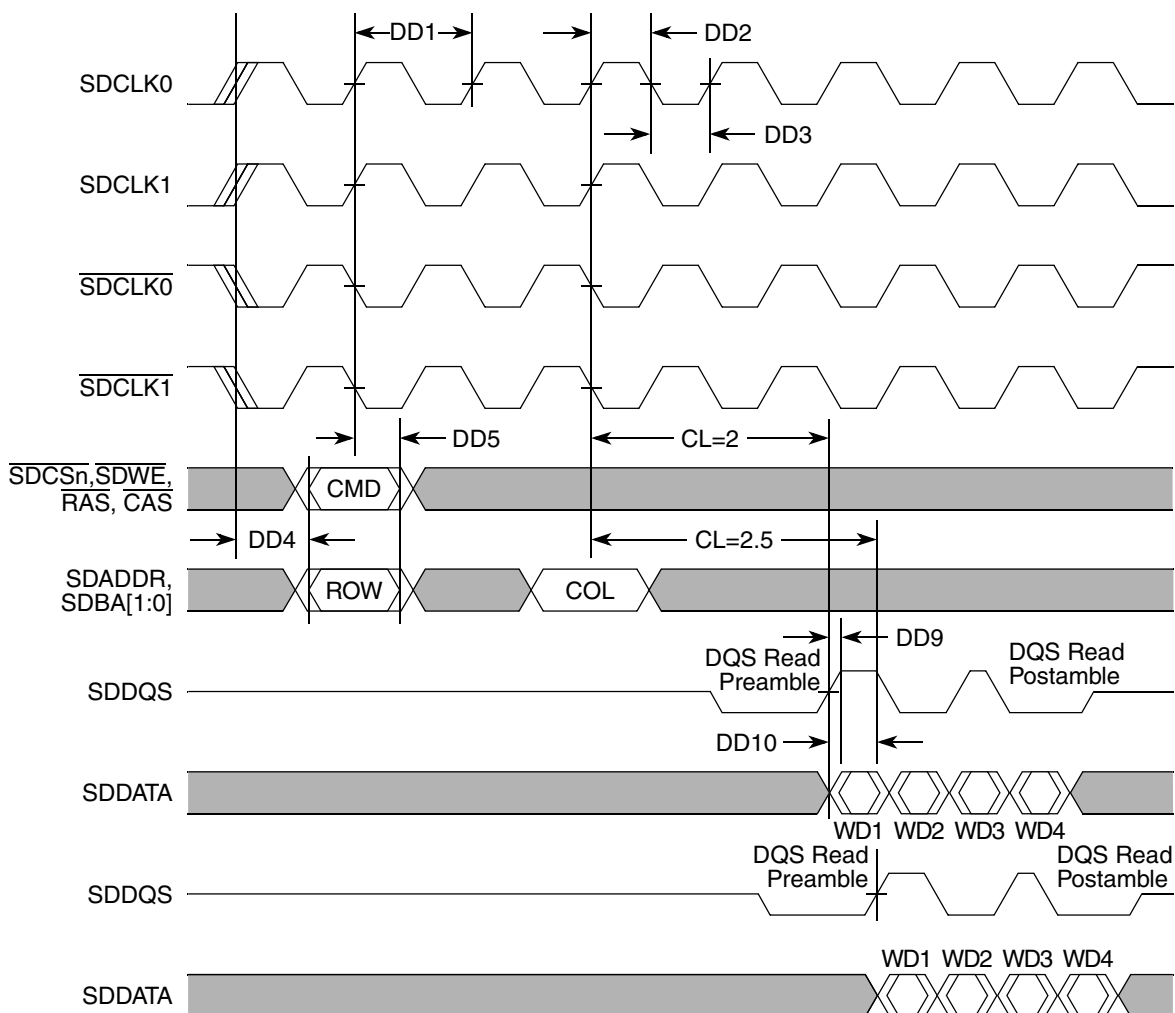


Figure 17. DDR Read Timing

10 PCI Bus

The PCI bus on the MCF547x is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Please refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	66	MHz	¹
P1	Clock Period (t_{CK})	15.15	40	ns	²
P2	Address, Data, and Command ($33 < \text{PCI} \leq 66 \text{ Mhz}$)—Input Setup (t_{IS})	3.0	—	ns	
P3	Address, Data, and Command ($0 < \text{PCI} \leq 33 \text{ Mhz}$)—Input Setup (t_{IS})	7.0	—	ns	
P4	Address, Data, and Command ($33\text{--}66 \text{ Mhz}$)—Output Valid (t_{DV})	—	6.0	ns	³
P5	Address, Data, and Command ($0\text{--}33 \text{ Mhz}$) - Output Valid (t_{DV})	—	11.0	ns	
P6	PCI signals ($0\text{--}66 \text{ Mhz}$) - Output Hold (t_{DH})	0	—	ns	⁴

Table 14. PCI Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
P7	PCI signals (0–66 Mhz) - Input Hold (t_{IH})	0	—	ns	⁵
P8	PCI REQ/GNT (33 < PCI ≤ 66Mhz) - Output valid (t_{DV})	—	6	ns	⁶
P9	PCI REQ/GNT (0 < PCI ≤ 33Mhz) - Output valid (t_{DV})	—	12	ns	
P10	PCI REQ/GNT (33 < PCI ≤ 66Mhz) - Input Setup (t_{IS})	—	5	ns	
P11	PCI REQ (0 < PCI ≤ 33Mhz) - Input Setup (t_{IS})	12	—	ns	
P12	PCI GNT (0 < PCI ≤ 33Mhz) - Input Setup (t_{IS})	10	—	ns	

- ¹ Please see the reset configuration signals description in the “Signal Descriptions” chapter within the *MCF547x Reference Manual*. Also specific guidelines may need to be followed when operating the system PLL below certain frequencies.
- ² Max cycle rate is determined by CLKIN and how the user has the system PLL configured.
- ³ All signals defined as PCI based signals. Does not include PTP (point-to-point) signals.
- ⁴ PCI 2.2 spec does not require an output hold time. Although the MCF547X may provide a slight amount of hold, it is not required or guaranteed.
- ⁵ PCI 2.2 spec requires zero input hold.
- ⁶ These signals are defined at PTP (Point-to-point) in the PCI 2.2 spec.

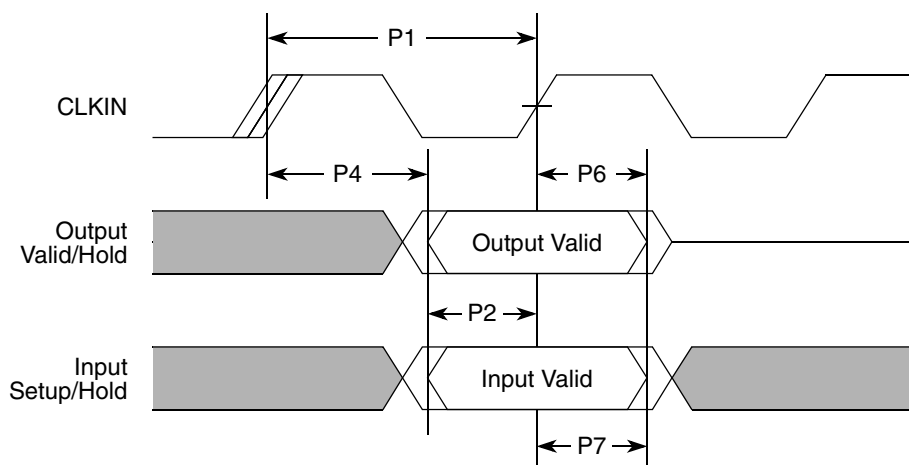


Figure 18. PCI Timing

11 Fast Ethernet AC Timing Specifications

11.1 MII/7-WIRE Interface Timing Specs

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the EMAC_10_100 I/O signals.

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices. If this interface is to be used with a specific transceiver device the timing specs may be altered to match that specific transceiver.

Table 15. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
M2	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
M3	RXCLK pulse width high	35%	65%	RXCLK period
M4	RXCLK pulse width low	35%	65%	RXCLK period

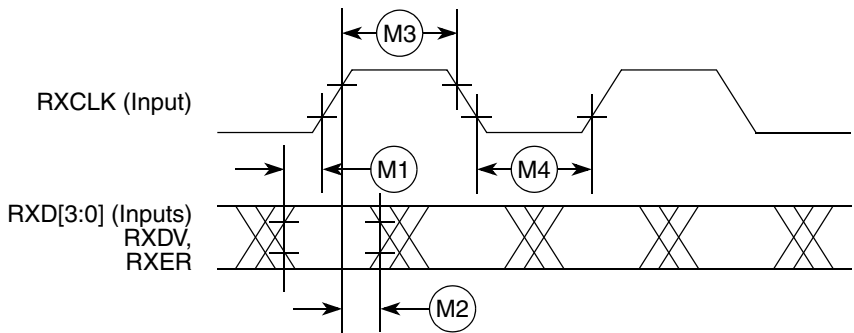


Figure 19. MII Receive Signal Timing Diagram

11.2 MII Transmit Signal Timing

Table 16. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	TXCLK to TXD[3:0], TXEN, TXER invalid	0	—	ns
M6	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns
M7	TXCLK pulse width high	35%	65%	TXCLK period
M8	TXCLK pulse width low	35%	65%	TXCLK period

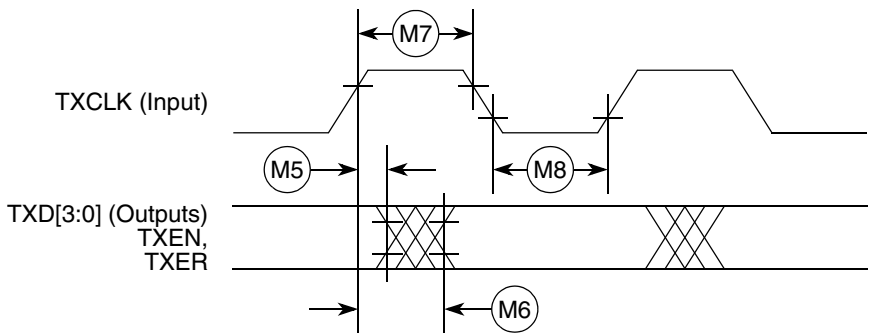


Figure 20. MII Transmit Signal Timing Diagram

12 General Timing Specifications

Table 19 lists timing specifications for the GPIO, PSC, $\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and external interrupts.

Table 19. General AC Timing Specifications

Name	Characteristic	Min	Max	Unit
G1	CLKIN high to signal output valid	—	2	PSTCLK
G2	CLKIN high to signal invalid (output hold)	0	—	ns
G3	Signal input pulse width	2	—	PSTCLK

13 I²C Input/Output Timing Specifications

Table 20 lists specifications for the I²C input timing parameters shown in Figure 23.

Table 20. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	Bus clocks
I2	Clock low period	8	—	Bus clocks
I3	SCL/SDA rise time ($V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$)	—	1	mS
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time ($V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$)	—	1	mS
I6	Clock high time	4	—	Bus clocks
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	Bus clocks
I9	Stop condition setup time	2	—	Bus clocks

Table 21 lists specifications for the I²C output timing parameters shown in Figure 23.

Table 21. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1 ¹	Start condition hold time	6	—	Bus clocks
I2 ¹	Clock low period	10	—	Bus clocks
I3 ²	SCL/SDA rise time ($V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$)	—	—	μS
I4 ¹	Data hold time	7	—	Bus clocks
I5 ³	SCL/SDA fall time ($V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$)	—	3	ns
I6 ¹	Clock high time	10	—	Bus clocks
I7 ¹	Data setup time	2	—	Bus clocks
I8 ¹	Start condition setup time (for repeated start condition only)	20	—	Bus clocks
I9 ¹	Stop condition setup time	10	—	Bus clocks

- ¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 21. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 21 are minimum values.
- ² Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
- ³ Specified at a nominal 50-pF load.

Figure 23 shows timing for the values in Table 20 and Table 21.

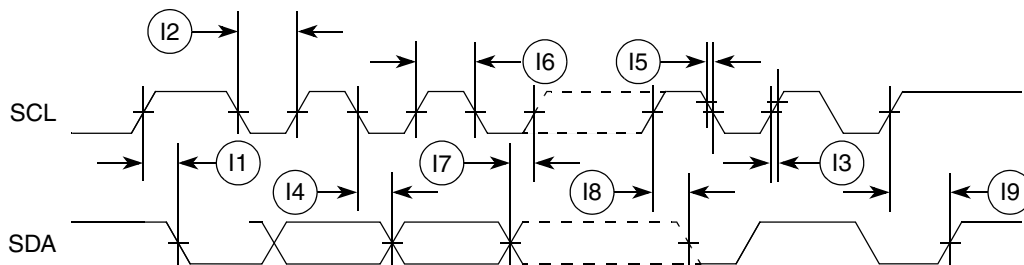


Figure 23. I²C Input/Output Timings

14 JTAG and Boundary Scan Timing

Table 22. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f _{JCYC}	DC	10	MHz
J2	TCLK Cycle Period	t _{JCYC}	2	—	t _{CK}
J3	TCLK Clock Pulse Width	t _{JCW}	15.15	—	ns
J4	TCLK Rise and Fall Times	t _{JCRF}	0.0	3.0	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t _{BSDST}	5.0	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t _{BSDHT}	24.0	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t _{BSDV}	0.0	15.0	ns
J8	TCLK Low to Boundary Scan Output High Z	t _{BSDZ}	0.0	15.0	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t _{TAPBST}	5.0	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t _{TAPBHT}	10.0	—	ns
J11	TCLK Low to TDO Data Valid	t _{TDODV}	0.0	20.0	ns
J12	TCLK Low to TDO High Z	t _{TDODZ}	0.0	15.0	ns
J13	$\overline{\text{TRST}}$ Assert Time	t _{TRSTAT}	100.0	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t _{TRSTST}	10.0	—	ns

¹ MTMOD is expected to be a static signal. Hence, it is not associated with any timing

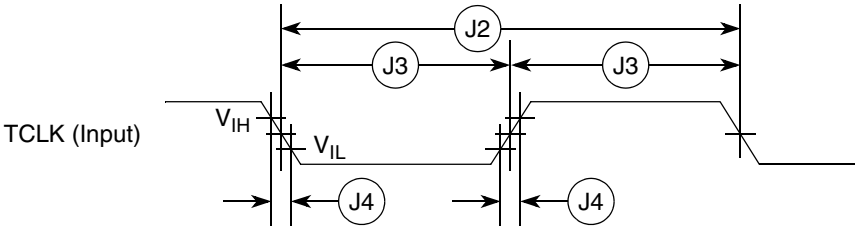


Figure 24. Test Clock Input Timing

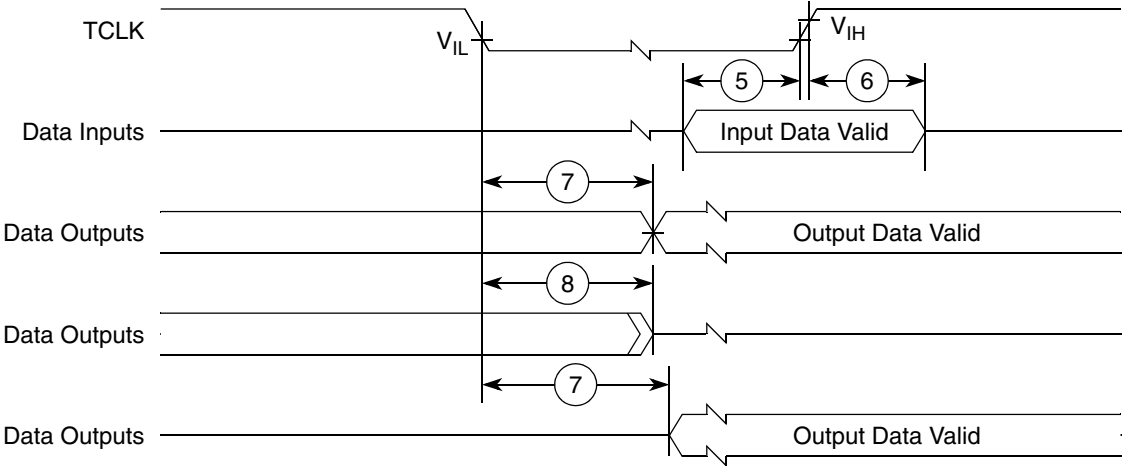


Figure 25. Boundary Scan (JTAG) Timing

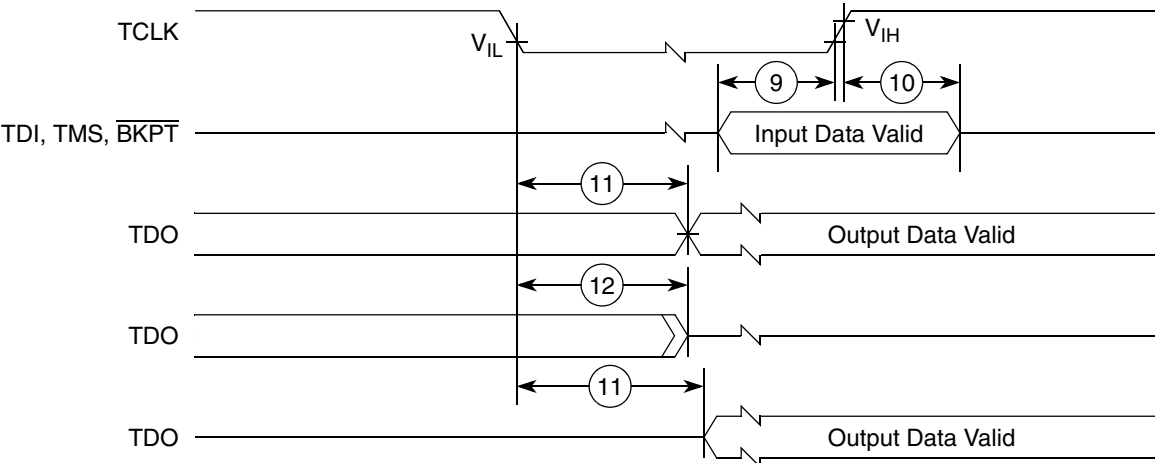


Figure 26. Test Access Port Timing

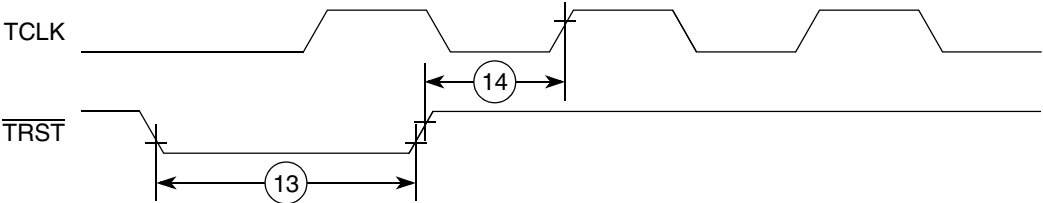
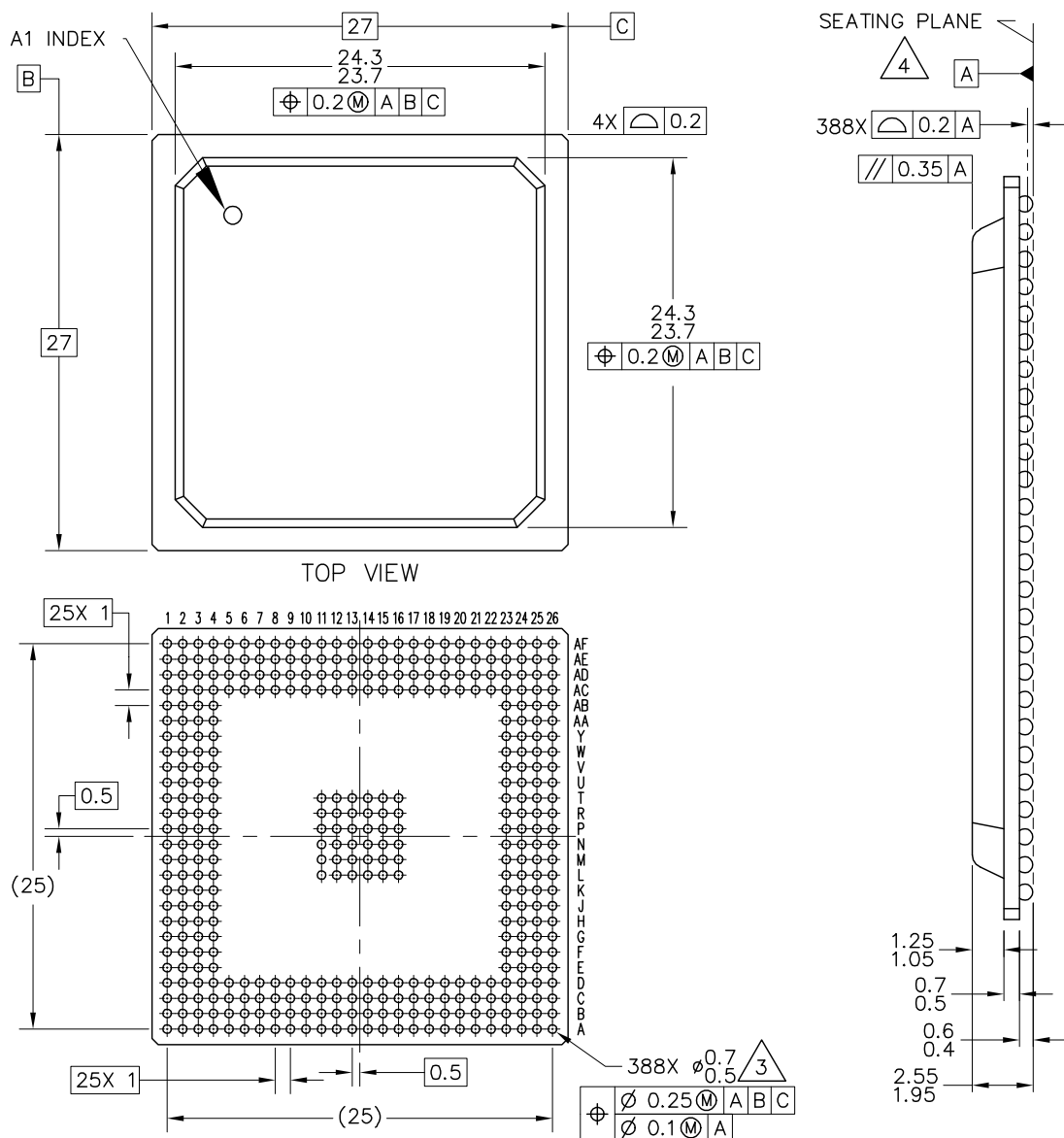



Figure 27. TRST Timing Debug AC Timing Specifications

17 Case Drawing



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TITLE: 388 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)				DOCUMENT NO: 98ARS23880W			REV: C		
				CASE NUMBER: 1164-02			25 JAN 2007		
				STANDARD: JEDEC MS-034 AAL-1					

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4.  DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PACKAGE CODES:
 5254 - 2 LAYER SUBSTRATE PACKAGE
 5367 - 4 LAYER SUBSTRATE PACKAGE

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TITLE: 388 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)		DOCUMENT NO: 98ARS23880W		REV: C	
		CASE NUMBER: 1164-02		25 JAN 2007	
		STANDARD: JEDEC MS-034 AAL-1			

Figure 31. 388-pin BGA Case Outline

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