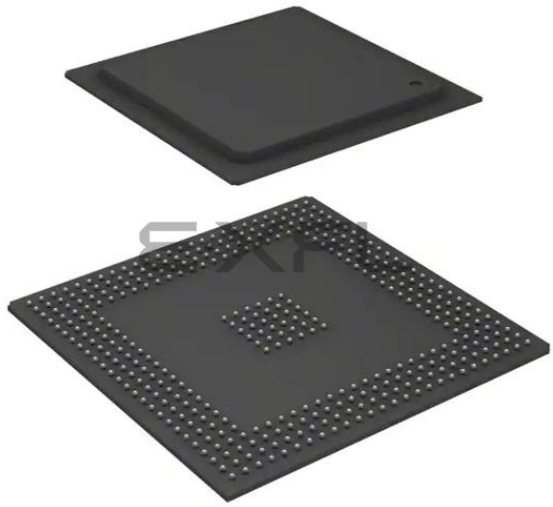


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V4E
Core Size	32-Bit Single-Core
Speed	266MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, PWM, WDT
Number of I/O	99
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5475vr266

Table of Contents

List of Figures

List of Tables

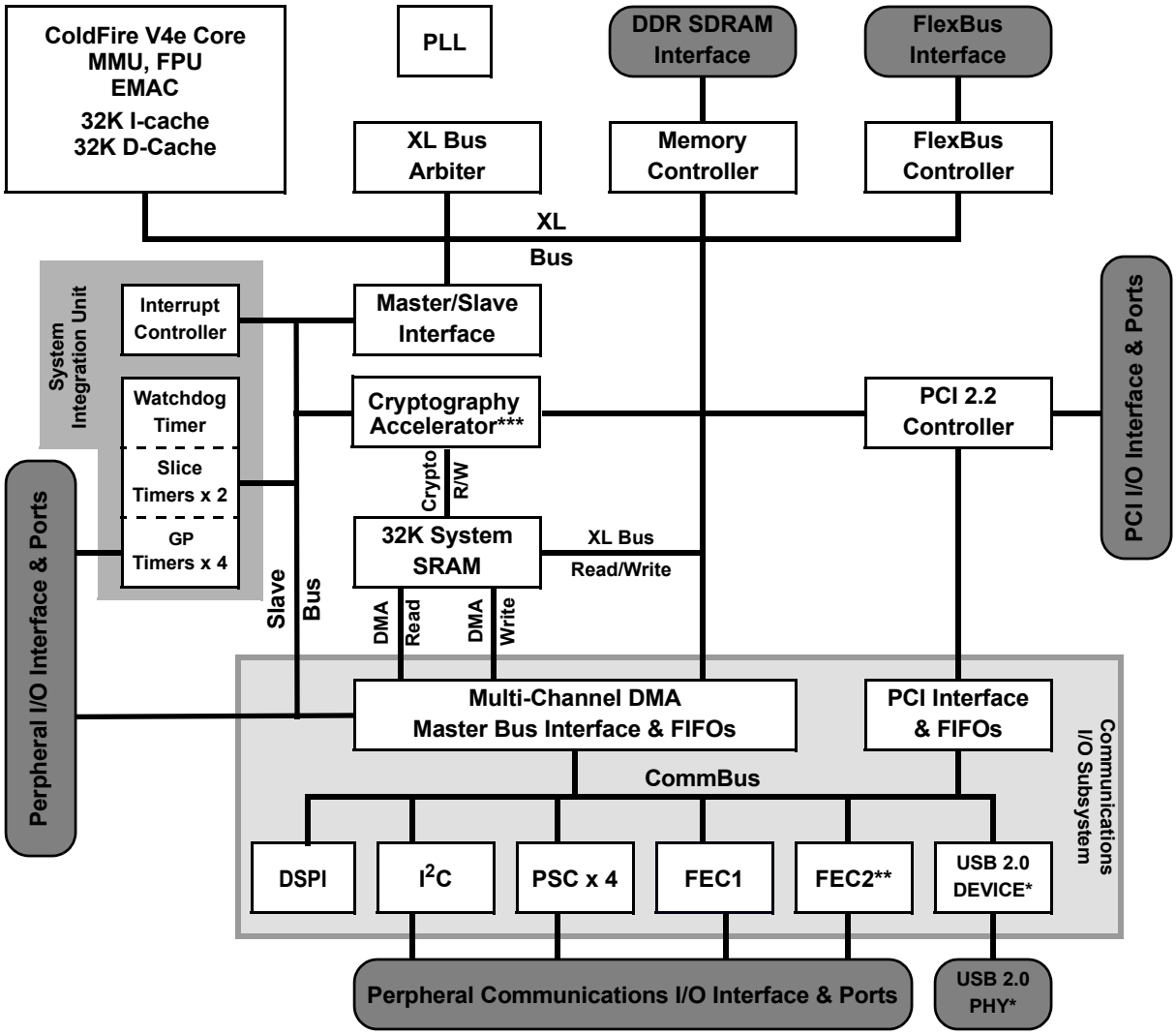
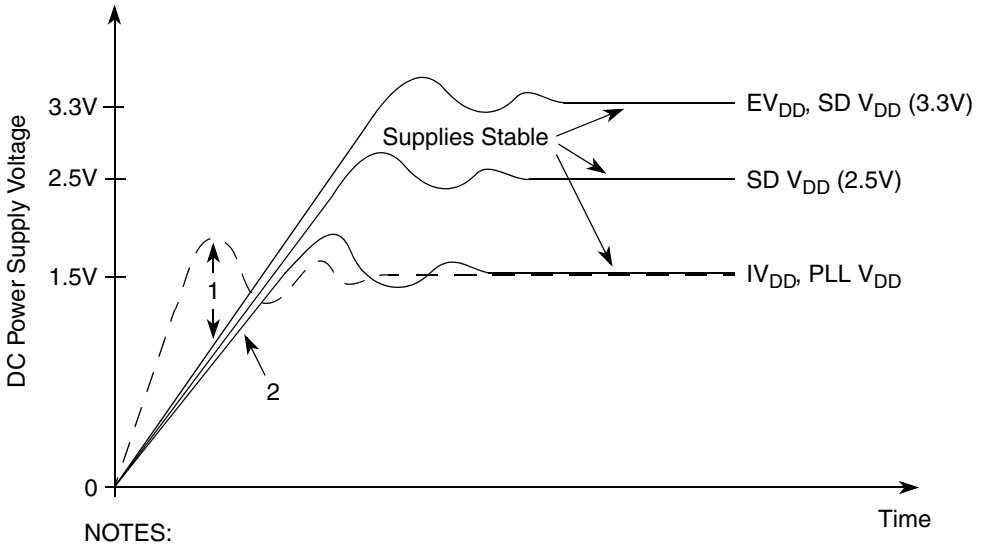


Figure 1. MCF547X Block Diagram



NOTES:
1. IVDD should not exceed EVDD or SD VDD by more than 0.4V at any time, including power-up.
2. Recommended that IVDD/PLL VDD should track EVDD/SD VDD up to 0.9V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (EVDD, SD VDD, IVDD, or PLL VDD) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

The relationship between SD V_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SD V_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

4.2.1 Power Up Sequence

If EV_{DD}/SD V_{DD} are powered up with the IV_{DD} at 0V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SD V_{DD} to be in a high impedance state. There is no limit to how long after EV_{DD}/SD V_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, SD V_{DD}, or PLL V_{DD} by more than 0.4V during power ramp up or there is high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IV_{DD}/PLL V_{DD} and EV_{DD}/SD V_{DD} should track up to 0.9V, then separate for the completion of ramps with EV_{DD}/SD V_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

4.2.2 Power Down Sequence

If IV_{DD}PLL V_{DD} are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PLL V_{DD} power down before EV_{DD} or SD V_{DD} must power down. IV_{DD} should not lag EV_{DD}, SD V_{DD}, or PLL V_{DD} going low by more than 0.4V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PLL V_{DD} to 0V
2. Drop EV_{DD}/SD V_{DD} supplies

4.3 General USB Layout Guidelines

4.3.1 USB D+ and D- High-Speed Traces

1. High speed clock and the USBD+ and USBD- differential pair should be routed first.
2. Route USBD+ and USBD- signals on the top layer of the board.
3. The trace width and spacing of the USBD+ and USBD- signals should be such that the differential impedance is 90Ω.
4. Route traces over continuous planes (power and ground)—they should not pass over any power/ground plane slots or anti-etch. When placing connectors, make sure the ground plane clear-outs around each pin have ground continuity between all pins.
5. Maintain the parallelism (skew matched) between USBD+ and USBD-. These traces should be the same overall length.
6. Do not route USBD+ and USBD- traces under oscillators or parallel to clock traces and/or data buses. Minimize the lengths of high speed signals that run parallel to the USBD+ and USBD- pair. Maintain a minimum 50mil spacing to clock signals.
7. Keep USBD+ and USBD- traces as short as possible.
8. Route USBD+, USBD-, and USBVBUS signals with a minimum amount of vias and corners. Use 45° turns.
9. Stubs should be avoided as much as possible. If they cannot be avoided, stubs should be no greater than 200mils.

4.3.2 USB VBUS Traces

Connecting the USBVBUS pin directly to the 5V VBUS signal from the USB connector can cause long-term reliability problems in the ESD network of the processor. Therefore, use of an external voltage divider for VBUS is recommended. Figure 4 and Figure 5 depict possible connections for VBUS. Point A, marked in each figure, is where a 5V version of VBUS should connect. Point B, marked in each figure, is where a 3.3V version of VBUS should connect to the USBVBUS pin on the device.

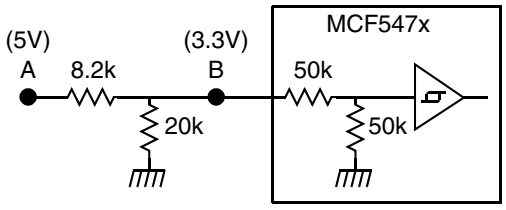


Figure 4. Preferred VBUS Connections

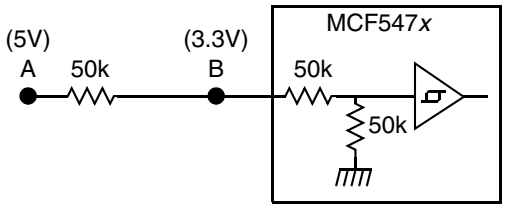


Figure 5. Alternate VBUS Connections

4.3.3 USB Receptacle Connections

It is recommended to connect the shield and the ground pin of the B USB receptacle for upstream ports to the board ground plane. The ground pin of the A USB receptacles for downstream ports should also be connected to the board ground plane, but industry practice varies widely on the connection of the shield of the A USB receptacles to other system grounds. Take precautions for control of ground loops between hosts and self-powered USB devices through the cable shield.

6 PLL Timing Specifications

The specifications in Table 7 are for the CLKIN pin.

Table 7. Clock Timing Specifications

Num	Characteristic	Min	Max	Units
C1	Cycle time	15.0	40	ns
C2	Rise time (20% of Vdd to 80% of vdd)	—	2	ns
C3	Fall time (80% of Vdd to 20% of Vdd)	—	2	ns
C4	Duty cycle (at 50% of Vdd)	40	60	%

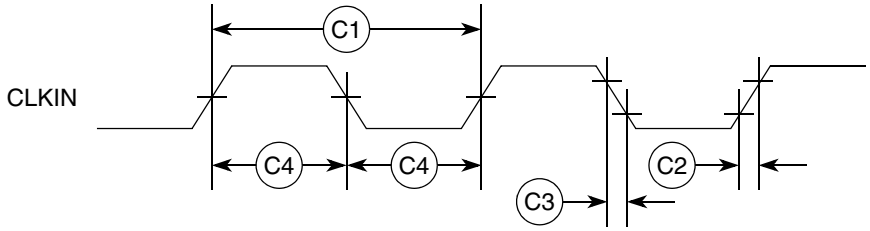


Figure 8. Input Clock Timing Diagram

Table 8 shows the supported PLL encodings.

Table 8. MCF547x Divide Ratio Encodings

AD[12:8][1]	Clock Ratio	CLKIN—PCI and FlexBus Frequency Range (MHz)	Internal XLB, SDRAM Bus, and PSTCLK Frequency Range (MHz)	Core Frequency Range (MHz)
00011	1:2	41.67–66.66	83.33–133.33	166.66–266.66
00101	1:2	25.0–44.42	50.0–88.83[2]	100.0–177.66
01111	1:4	25.0–33.3	100–133.33	200–266.66

1 All other values of AD[12:8] are reserved.

2 DDR memories typically have a minimum speed of 83 MHz. Some vendors specifiy down to 75 MHz. Check with the memory component specifications to verify.

Figure 9 correlates CLKIN, internal bus, and core clock frequencies for the 1x–4x multipliers.

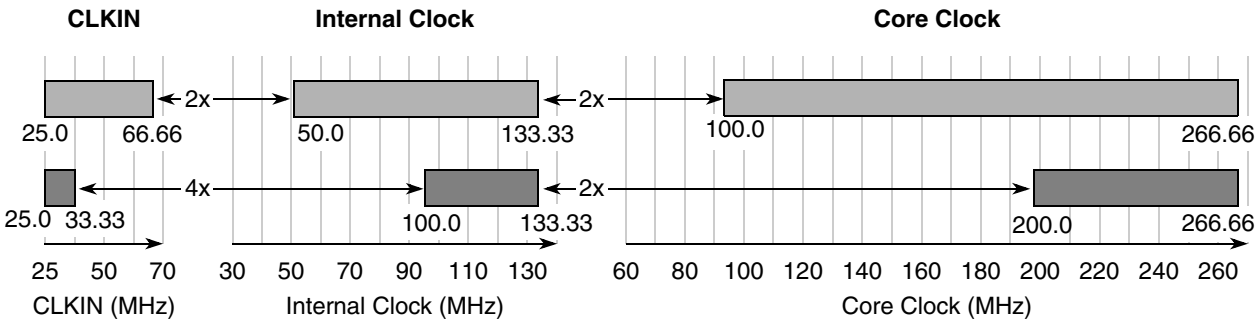


Figure 9. CLKIN, Internal Bus, and Core Clock Ratios

8.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the system clock.

Table 10. FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	66	Mhz	1
FB1	Clock Period (CLKIN)	15.15	40	ns	2
FB2	Address, Data, and Control Output Valid (AD[31:0], $\overline{\text{FBCS}}$[5:0], R/$\overline{\text{W}}$, ALE, TSIZ[1:0], $\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0], $\overline{\text{OE}}$, and $\overline{\text{TBST}}$)	—	7.0	ns	3
FB3	Address, Data, and Control Output Hold ((AD[31:0], $\overline{\text{FBCS}}$[5:0], R/$\overline{\text{W}}$, ALE, TSIZ[1:0], $\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0], $\overline{\text{OE}}$, and $\overline{\text{TBST}}$)	1	—	ns	3, 4
FB4	Data Input Setup	3.5	—	ns	
FB5	Data Input Hold	0	—	ns	
FB6	Transfer Acknowledge ($\overline{\text{TA}}$) Input Setup	4	—	ns	
FB7	Transfer Acknowledge ($\overline{\text{TA}}$) Input Hold	0	—	ns	
FB8	Address Output Valid (PCIAD[31:0])	—	7.0	ns	5
FB9	Address Output Hold (PCIAD[31:0])	0	—	ns	5

1 The frequency of operation is the same as the PCI frequency of operation. The MCF547X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI.

2 Max cycle rate is determined by CLKIN and how the user has the system PLL configured.

3 Timing for chip selects only applies to the FBCS[5:0] signals. Please see Section 9.2, “DDR SDRAM AC Timing Characteristics” for SDCS[3:0] timing.

4 The FlexBus supports programming an extension of the address hold. Please consult the MCF547X specification manual for more information.

5 These specs are used when the PCIAD[31:0] signals are configured as 32-bit, non-muxed FlexBus address signals.

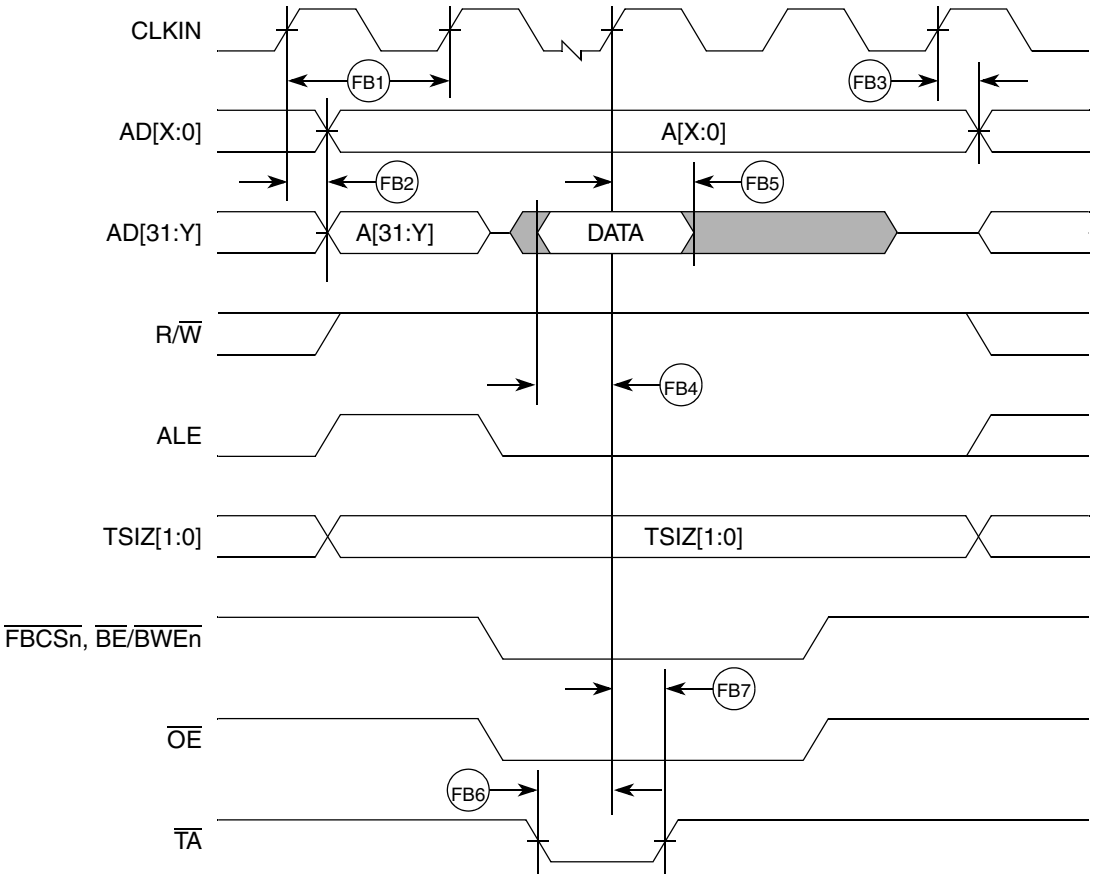


Figure 11. FlexBus Read Timing

Table 11. SDR Timing Specifications

Symbol	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	0	133	Mhz	1
SD1	Clock Period (t_{CK})	7.52	12	ns	2
SD2	Clock Skew (t_{SK})		TBD		
SD3	Pulse Width High (t_{CKH})	0.45	0.55	SDCLK	3
SD4	Pulse Width Low (t_{CKL})	0.45	0.55	SDCLK	4
SD5	Address, CKE, CAS, RAS, WE, BA, CS - Output Valid (t_{CMV})		0.5 × SDCLK + 1.0ns	ns	
SD6	Address, CKE, CAS, RAS, WE, BA, CS - Output Hold (t_{CMH})	2.0		ns	
SD7	SDRDQS Output Valid (t_{DQSOV})		Self timed	ns	5
SD8	SDDQS[3:0] input setup relative to SDCLK (t_{DQSIS})	0.25 × SDCLK	0.40 × SDCLK	ns	6
SD9	SDDQS[3:0] input hold relative to SDCLK (t_{DQSIH})	Does not apply. 0.5 SDCLK fixed width.			7
SD10	Data Input Setup relative to SDCLK (reference only) (t_{DIS})	0.25 × SDCLK		ns	8
SD11	Data Input Hold relative to SDCLK (reference only) (t_{DIH})	1.0		ns	
SD12	Data and Data Mask Output Valid (t_{DV})		0.75 × SDCLK +0.500ns	ns	
SD13	Data and Data Mask Output Hold (t_{DH})	1.5		ns	

1 The frequency of operation is 2x or 4x the CLKIN frequency of operation. The MCF547X supports a single external reference clock (CLKIN). This signal defines the frequency of operation for FlexBus and PCI, but SDRAM clock operates at the same frequency as the internal bus clock. Please see the PLL chapter of the *MCF547X Reference Manual* for more information on setting the SDRAM clock rate.

2 SDCLK is one SDRAM clock in (ns).

3 Pulse width high plus pulse width low cannot exceed min and max clock period.

4 Pulse width high plus pulse width low cannot exceed min and max clock period.

5 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SDR_DQS only pulses during a read cycle and one pulse occurs for each data beat.

6 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS only pulses during a read cycle and one pulse occurs for each data beat.

7 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.

8 Because a read cycle in SDR mode uses the DQS circuit within the MCF547X, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens results in successful SDR reads. The input setup spec is provided as guidance.

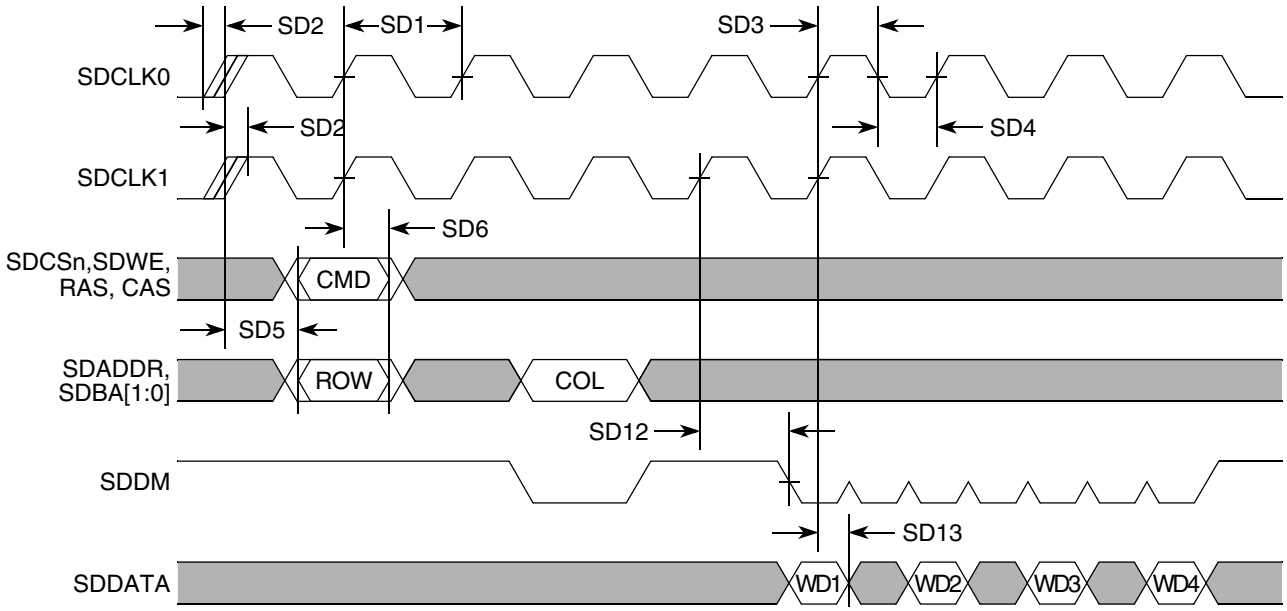


Figure 13. SDR Write Timing

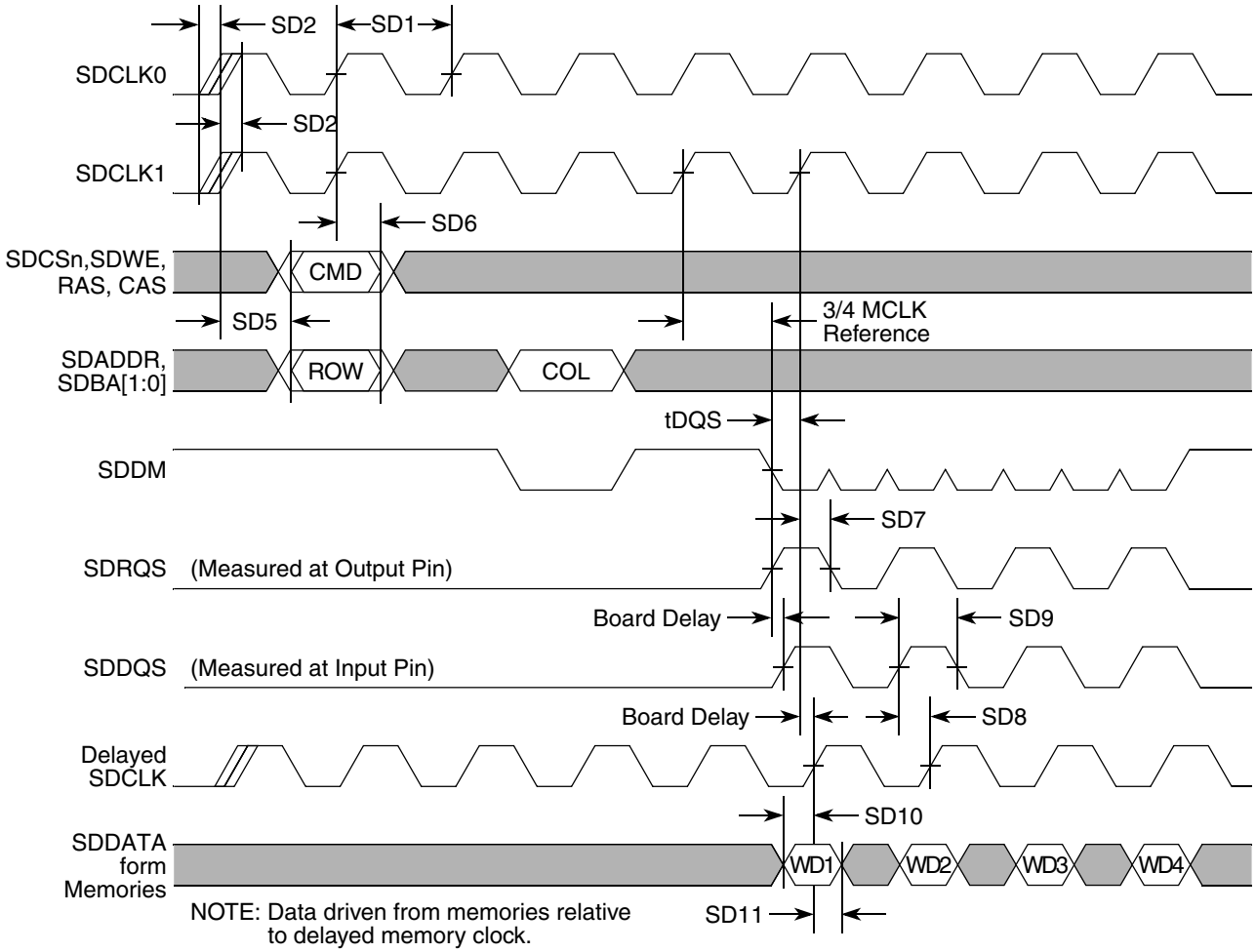


Figure 14. SDR Read Timing

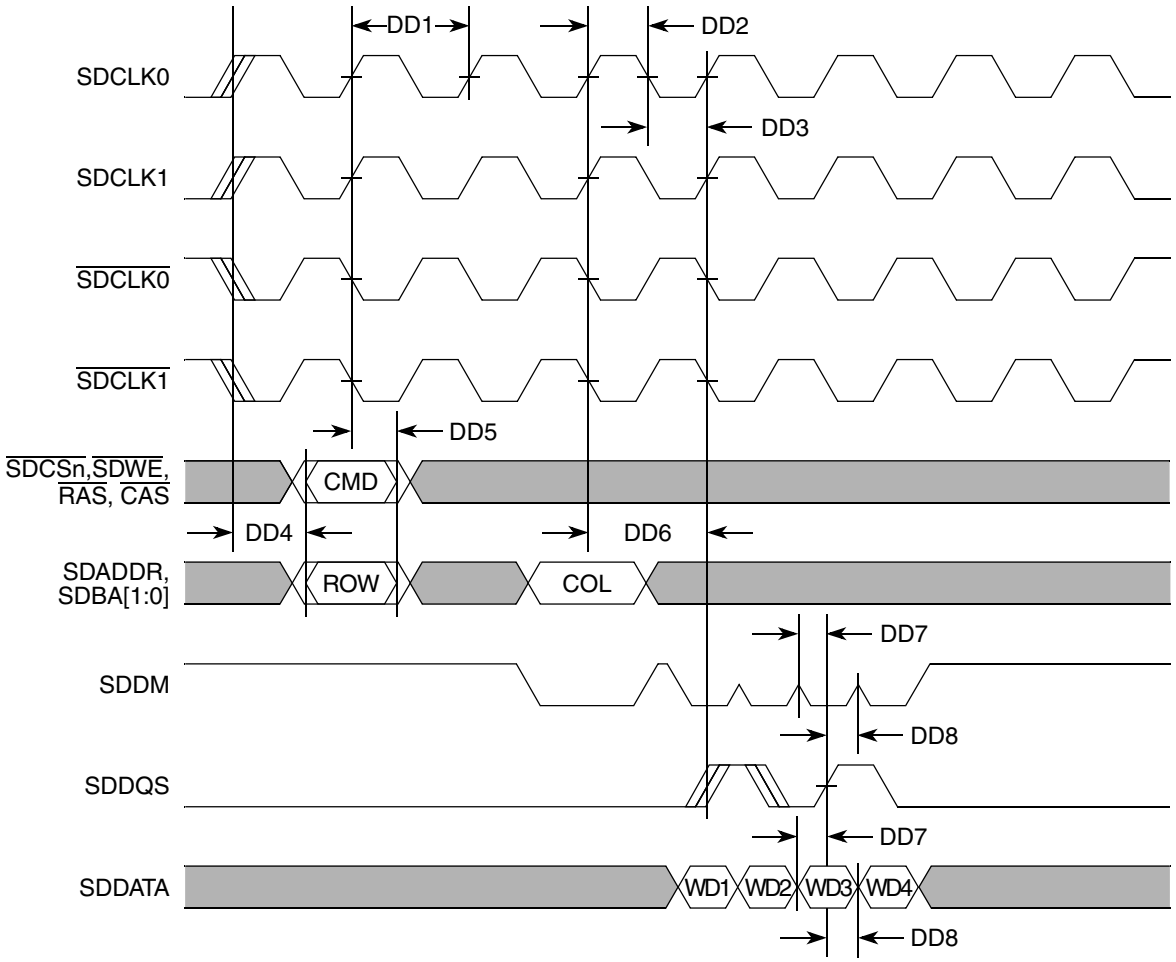


Figure 16. DDR Write Timing

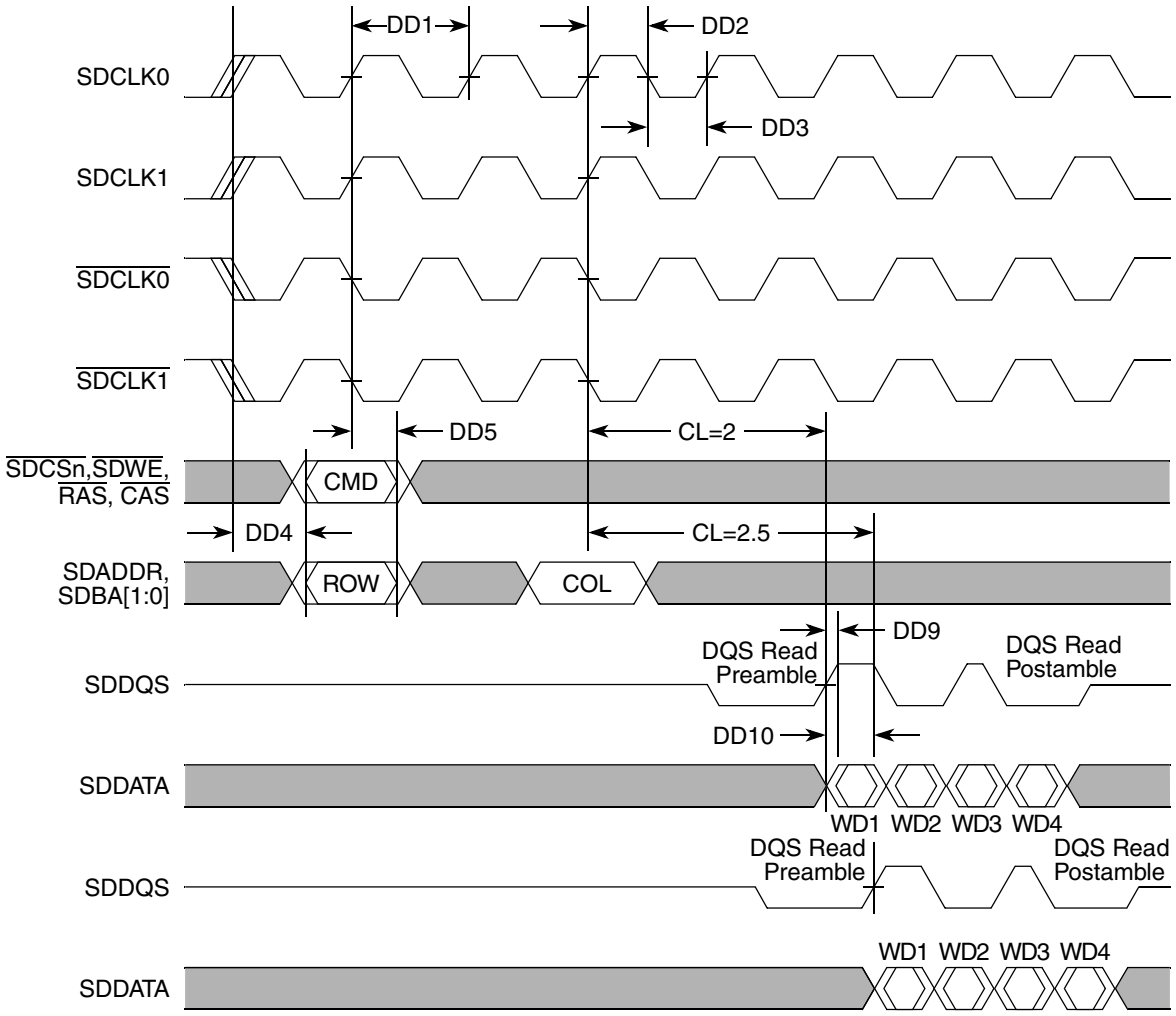


Figure 17. DDR Read Timing

10 PCI Bus

The PCI bus on the MCF547*x* is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Please refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	66	MHz	1
P1	Clock Period (t_{CK})	15.15	40	ns	2
P2	Address, Data, and Command (33< PCI ≤ 66 Mhz)—Input Setup (t_{IS})	3.0	—	ns	
P3	Address, Data, and Command (0 < PCI ≤ 33 Mhz)—Input Setup (t_{IS})	7.0	—	ns	
P4	Address, Data, and Command (33–66 Mhz)—Output Valid (t_{DV})	—	6.0	ns	3
P5	Address, Data, and Command (0–33 Mhz) - Output Valid (t_{DV})	—	11.0	ns	
P6	PCI signals (0–66 Mhz) - Output Hold (t_{DH})	0	—	ns	4

Table 14. PCI Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
P7	PCI signals (0–66 Mhz) - Input Hold (t_{IH})	0	—	ns	5
P8	PCI REQ/GNT (33 < PCI ≤ 66Mhz) - Output valid (t_{DV})	—	6	ns	6
P9	PCI REQ/GNT (0 < PCI ≤ 33Mhz) - Output valid (t_{DV})	—	12	ns	
P10	PCI REQ/GNT (33 < PCI ≤ 66Mhz) - Input Setup (t_{IS})	—	5	ns	
P11	PCI REQ (0 < PCI ≤ 33Mhz) - Input Setup (t_{IS})	12	—	ns	
P12	PCI GNT (0 < PCI ≤ 33Mhz) - Input Setup (t_{IS})	10	—	ns	

1 Please see the reset configuration signals description in the “Signal Descriptions” chapter within the *MCF547x Reference Manual*. Also specific guidelines may need to be followed when operating the system PLL below certain frequencies.

2 Max cycle rate is determined by CLKIN and how the user has the system PLL configured.

3 All signals defined as PCI bused signals. Does not include PTP (point-to-point) signals.

4 PCI 2.2 spec does not require an output hold time. Although the MCF547X may provide a slight amount of hold, it is not required or guaranteed.

5 PCI 2.2 spec requires zero input hold.

6 These signals are defined at PTP (Point-to-point) in the PCI 2.2 spec.

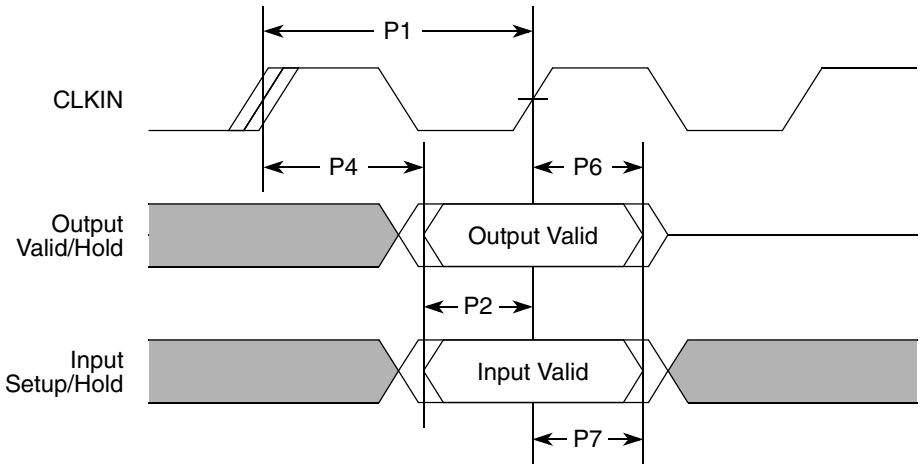


Figure 18. PCI Timing

11 Fast Ethernet AC Timing Specifications

11.1 MII/7-WIRE Interface Timing Specs

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the EMAC_10_100 I/O signals.

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices. If this interface is to be used with a specific transceiver device the timing specs may be altered to match that specific transceiver.

11.3 MII Async Inputs Signal Timing (CRS, COL)

Table 17. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

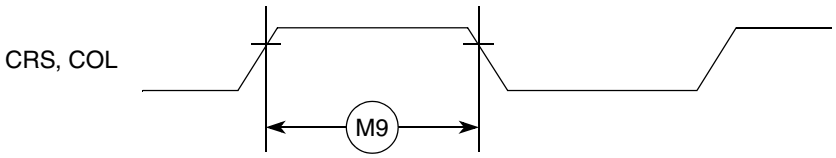


Figure 21. MII Async Inputs Timing Diagram

11.4 MII Serial Management Channel Timing (MDIO,MDC)

Table 18. MII Serial Management Channel Signal Timing

Num	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (min prop delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

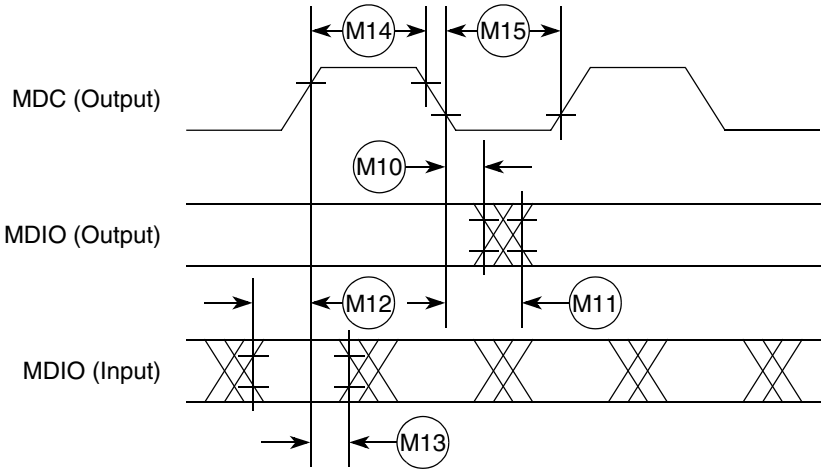


Figure 22. MII Serial Management Channel TIming Diagram

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 21. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 21 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 23 shows timing for the values in Table 20 and Table 21.

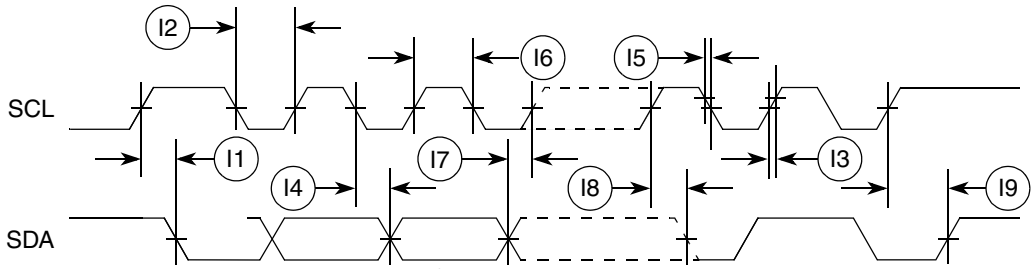


Figure 23. I^2C Input/Output Timings

14 JTAG and Boundary Scan Timing

Table 22. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	10	MHz
J2	TCLK Cycle Period	t_{JCYC}	2	—	t_{CK}
J3	TCLK Clock Pulse Width	t_{JCW}	15.15	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0.0	3.0	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	5.0	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	24.0	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0.0	15.0	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0.0	15.0	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	5.0	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10.0	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0.0	20.0	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0.0	15.0	ns
J13	$\overline{TRST}$ Assert Time	t_{TRSTAT}	100.0	—	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10.0	—	ns

1 MTMOD is expected to be a static signal. Hence, it is not associated with any timing

Table 23 lists specifications for the debug AC timing parameters shown in Figure 29.

Table 23. Debug AC Timing Specifications

Num	Characteristic	66 MHz		Units
		Min	Max	
D1	PSTDDATA to PSTCLK setup	4.5	—	ns
D2	PSTCLK to PSTDDATA hold	4.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLKs
D4 [1]	DSCLK-to-DSO hold	4	—	PSTCLKs
D5	DSCLK cycle time	5	—	PSTCLKs

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 23.

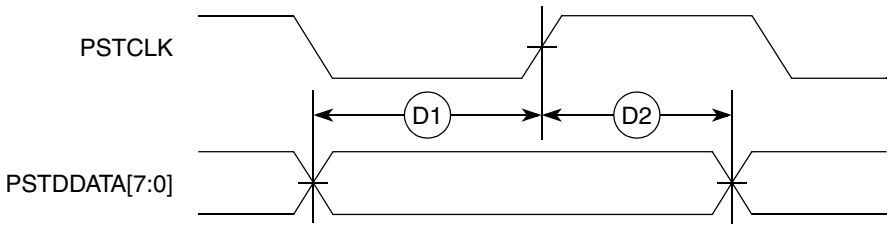


Figure 28. Real-Time Trace AC Timing

Figure 29 shows BDM serial port AC timing for the values in Table 23.

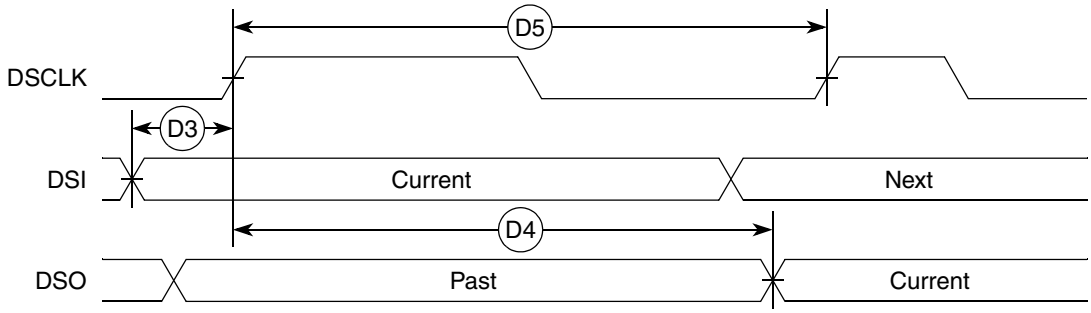
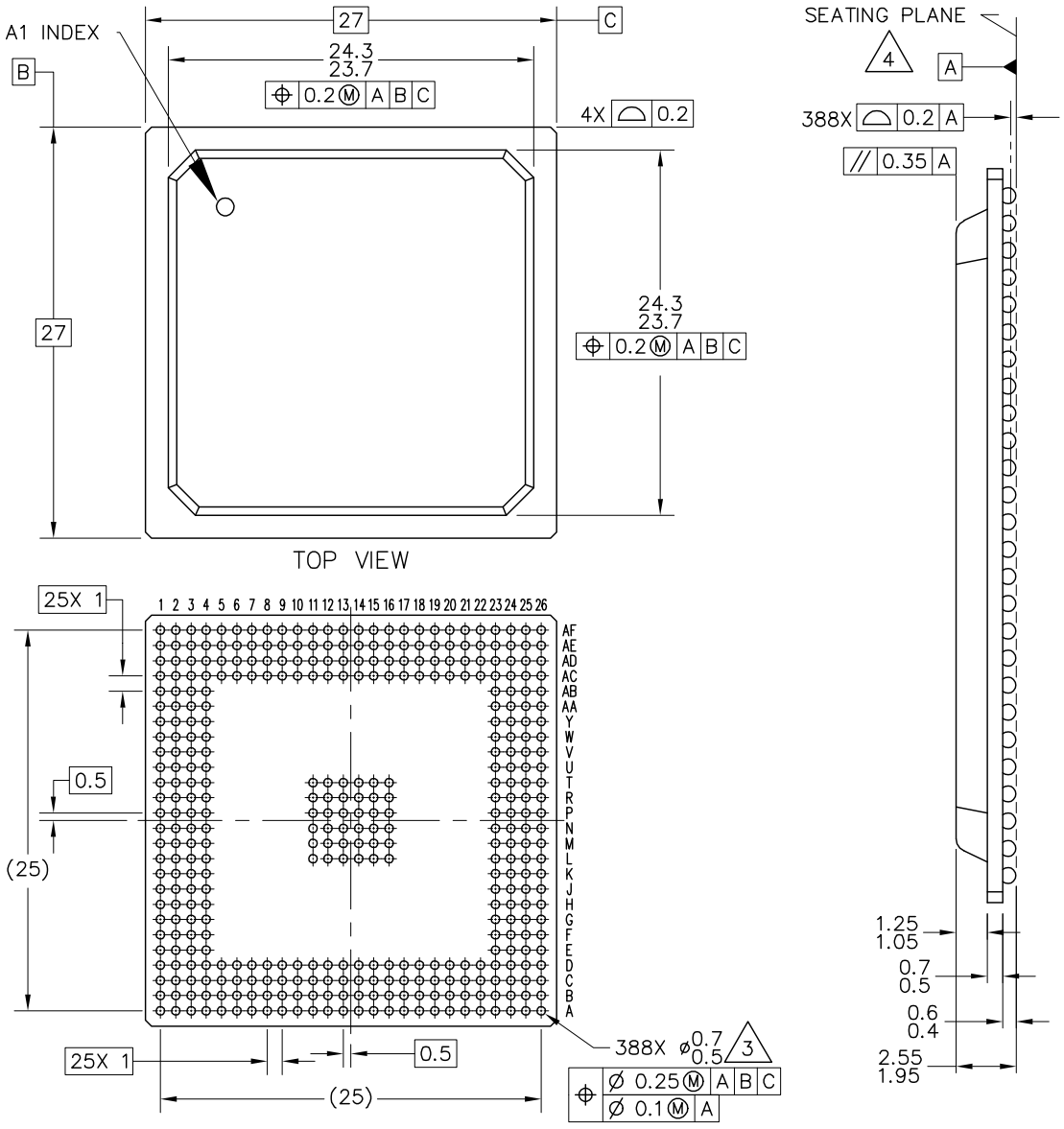


Figure 29. BDM Serial Port AC Timing

17 Case Drawing



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ARS23880W	REV: C
388 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	CASE NUMBER: 1164–02	25 JAN 2007
	STANDARD: JEDEC MS–034 AAL–1	

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PACKAGE CODES:
   5254 – 2 LAYER SUBSTRATE PACKAGE
   5367 – 4 LAYER SUBSTRATE PACKAGE

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 388 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARS23880W	REV: C
	CASE NUMBER: 1164–02	25 JAN 2007
	STANDARD: JEDEC MS–034 AAL–1	

Figure 31. 388-pin BGA Case Outline

18 Revision History

Revision Number	Date	Substantive Changes
2.2	August 29, 2005	Table 7: Changed C1 maximum spec from 33.3 ns to 40 ns.
2.3	August 30, 2005	Table 22: Changed J11 maximum from 15 ns to 20 ns.
2.4	December 14, 2005	Table 10: Changed FB1 maximum from 33.33 ns to 40 ns. Table 14: Changed FB1 maximum from 33.33 ns to 40 ns.
3	February 20, 2007	Table 4: Updated DC electrical specifications, V_{IL} and V_{IH}. Table 6: Changed FlexBus output load from 20pF to 30pF. Added Section 4.3, “General USB Layout Guidelines.”
4	December 4, 2007	Figure 2: Changed resistor value from 10W to 10Ω Figure 3: Changed note 1 in from “IVDD should not exceed EVDD, SD VDD or PLL VDD by more than 0.4V...” to “IVDD should not exceed EVDD or SD VDD by more than 0.4V...” Table 3: Updated thermal information for θ_{JMA}, θ_{JB}, and θ_{JC} Table 4: Added input leakage current spec. Table 6: Added footnote regarding pads having balanced source & sink current. Table 9: Added $\overline{\text{RSTI}}$ pulse duration spec. Added features list, pinout drawing, block diagram, and case outline.

THIS PAGE INTENTIONALLY BLANK

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MCF5475EC
Rev. 4
12/2007

freescale™
semiconductor