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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	35-UFBGA, WLCSP
Supplier Device Package	35-WLCSP (3.23x2.10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4244fni-443t

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
  - AN90071: CY8CMBRxxx CapSense Design Guide
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator

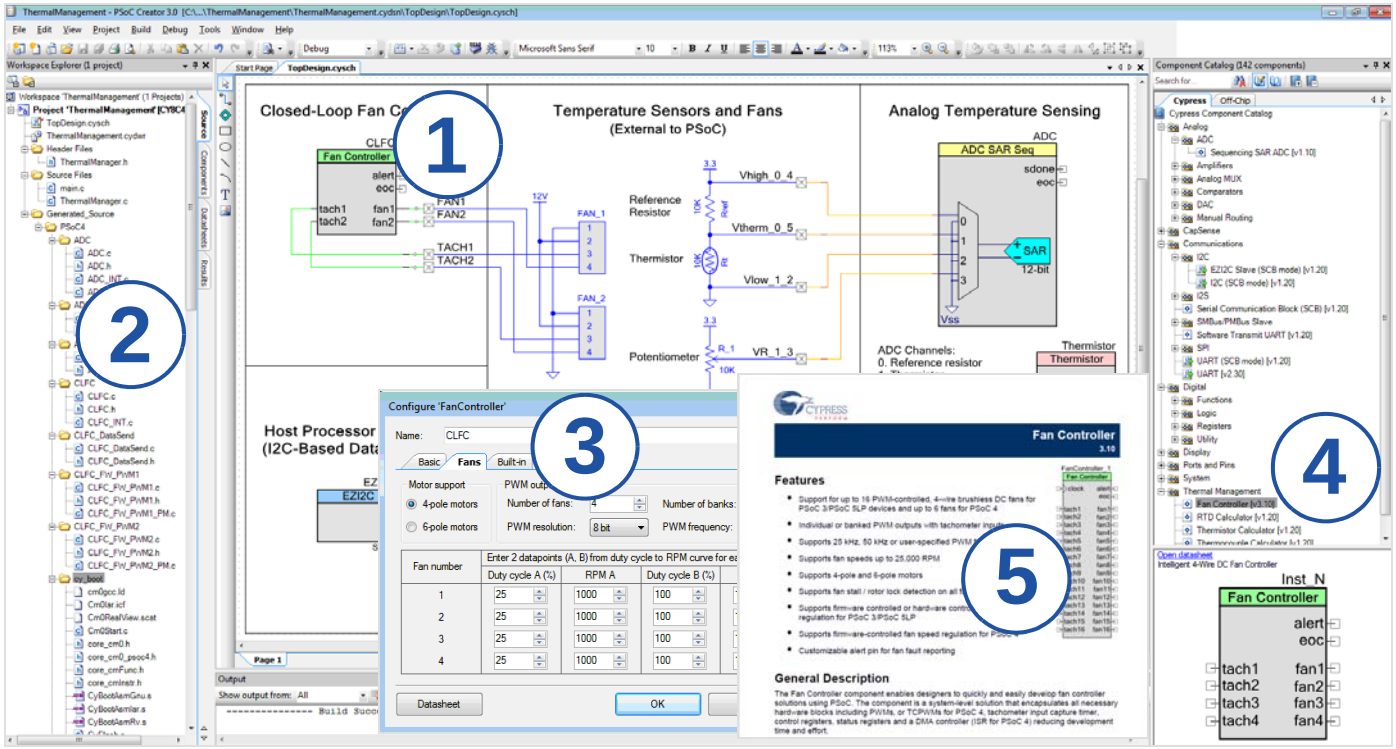
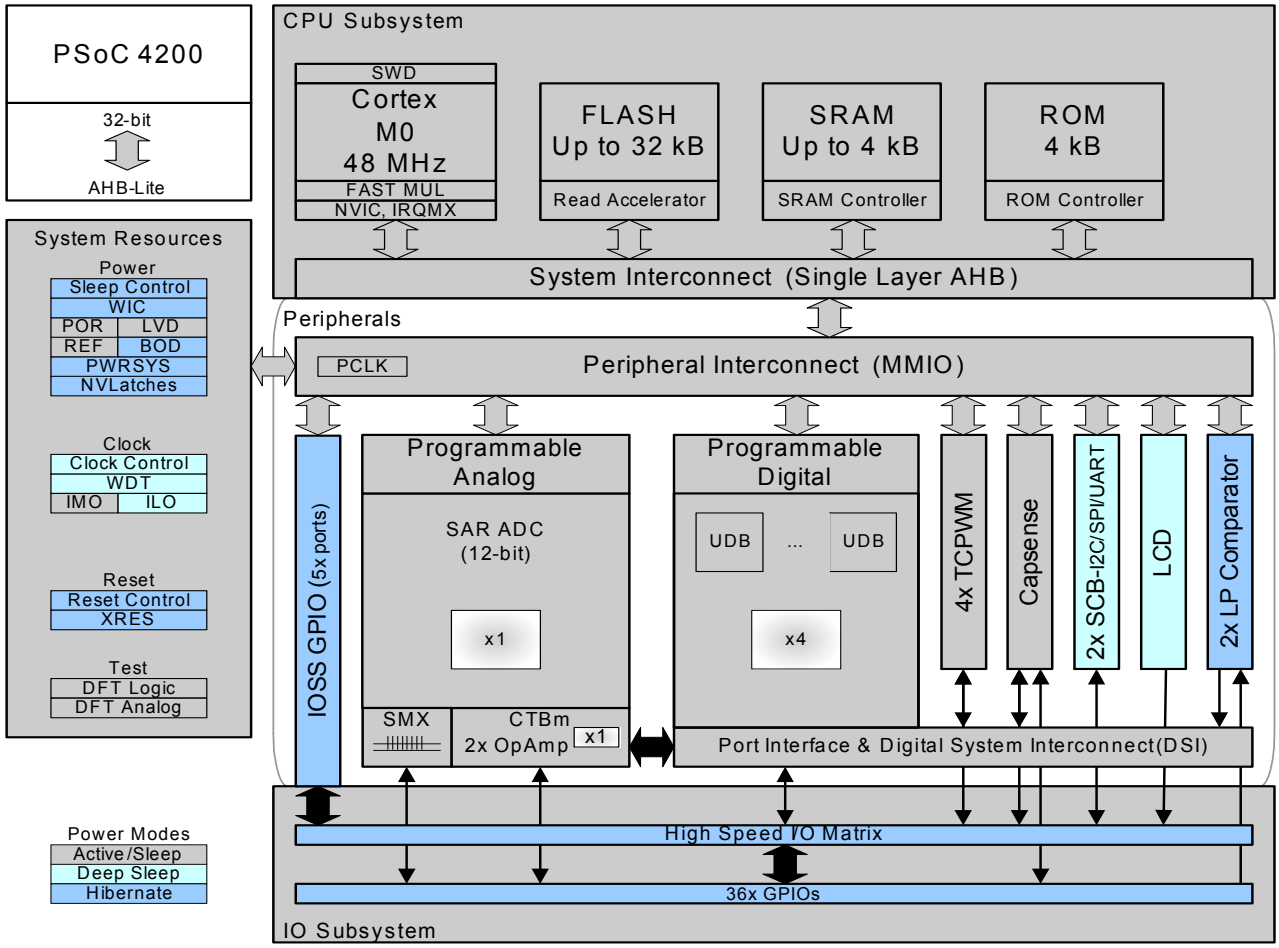


Figure 2. Block Diagram



The PSoC 4200 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4200 devices. The SWD interface is fully compatible with industry-standard third-party tools. With the ability to disable debug features, with very robust flash protection, and allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 4200 family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4200 with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4200 allows the customer to make.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 4200. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 48 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low-power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

PSoC 4200 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4200 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal to noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

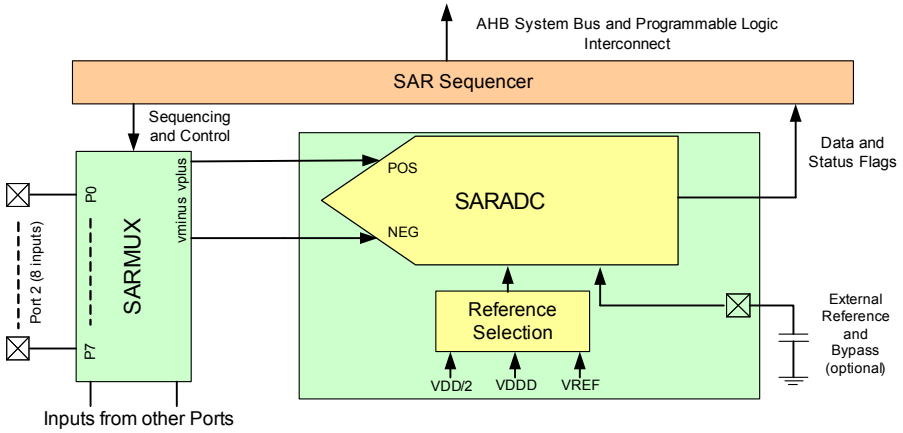
The 12-bit 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice (for the PSoC-4200 case) of three internal voltage references: V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 4. SAR ADC System Diagram



Two Opamps (CTBm Block)

PSoC 4200 has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the S/H circuit of the ADC without requiring external buffering.

Temperature Sensor

PSoC 4200 has one on-chip temperature sensor This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress supplied software that includes calibration and linearization.

Low-power Comparators

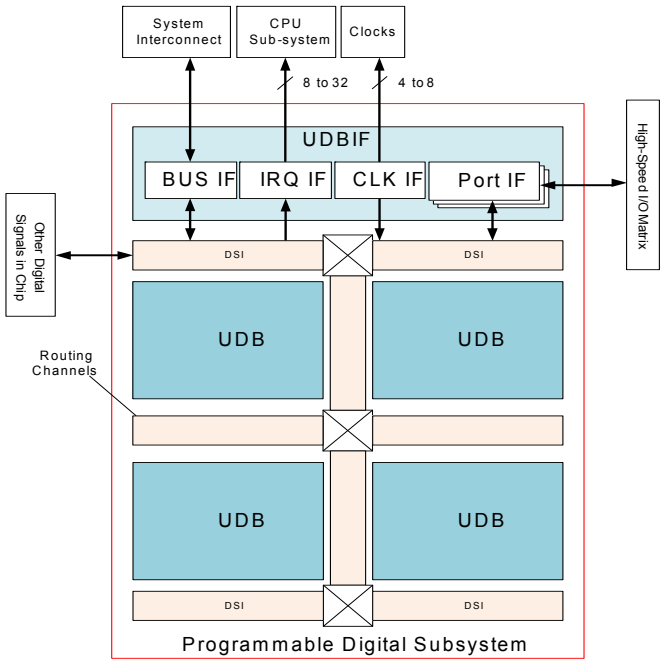
PSoC 4200 has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

PSoC 4200 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

Figure 5. UDB Array

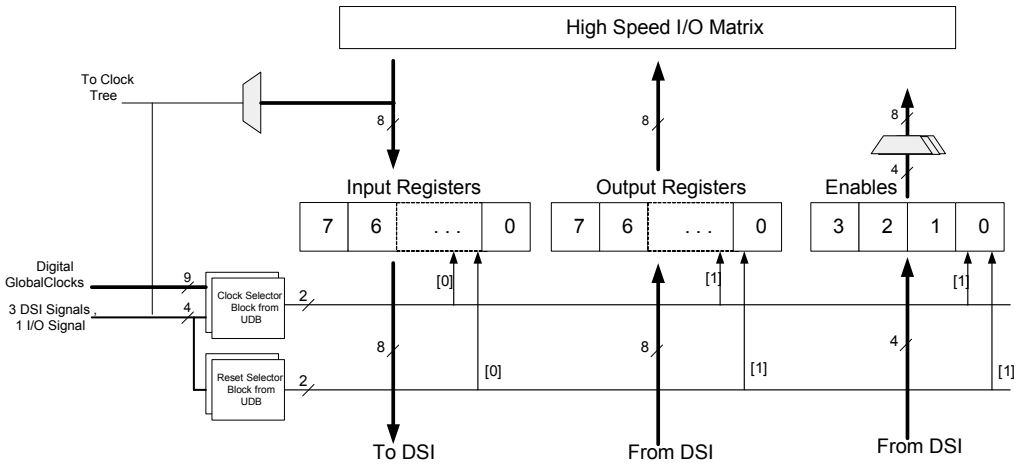


UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see Figure 6).

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to any pin on the chip through the DSI.

Figure 6. Port Interface



44-TQFP		40-QFN		28-SSOP		48-TQFP		Alternate Functions for Pins					Pin Description
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
24	P0.0	22	P0.0	19	P0.0	28	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
25	P0.1	23	P0.1	20	P0.1	29	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
26	P0.2	24	P0.2	21	P0.2	30	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
27	P0.3	25	P0.3	22	P0.3	31	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
28	P0.4	26	P0.4	–	–	32	P0.4	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
29	P0.5	27	P0.5	–	–	33	P0.5	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
30	P0.6	28	P0.6	23	P0.6	34	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
31	P0.7	29	P0.7	24	P0.7	35	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
32	XRES	30	XRES	25	XRES	36	XRES	–	–	–	–	–	Chip reset, active low
33	VCCD	31	VCCD	26	VCCD	37	VCCD	–	–	–	–	–	Regulated supply, connect to 1µF cap or 1.8V
–	–	–	–	–	–	38	VSSD	–	–	–	–	–	Digital Ground
34	VDDD	32	VDDD	27	VDD	39	VDDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5V
35	VDDA	33	VDDA	27	VDD	40	VDDA	–	–	–	–	–	Analog Supply, 1.8 - 5.5V, equal to VDDD
36	VSSA	34	VSSA	28	VSS	41	VSSA	–	–	–	–	–	Analog Ground
37	P1.0	35	P1.0	1	P1.0	42	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
38	P1.1	36	P1.1	2	P1.1	43	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
39	P1.2	37	P1.2	3	P1.2	44	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
40	P1.3	38	P1.3	–	–	45	P1.3	ctb.oa1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
41	P1.4	39	P1.4	–	–	46	P1.4	ctb.oa1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
42	P1.5	–	–	–	–	47	P1.5	ctb.oa1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
43	P1.6	–	–	–	–	48	P1.6	ctb.oa0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
44	P1.7/VREF	40	P1.7/VREF	4	P1.7/VREF	1	P1.7/VREF	ctb.oa1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Notes:

1. tcpwm_p and tcpwm_n refer to tcpwm non-inverted and inverted outputs respectively.
2. P3.2 and P3.3 are SWD pins after boot (reset).

35-Ball CSP		Alternate Functions for Pins					Pin Description
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
D7	P1.3	ctb.oa1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
D4	P1.4	ctb.oa1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
D5	P1.5	ctb.oa1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
D6	P1.6	ctb.oa0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
E7	P1.7/VREF	ctb.oa1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Descriptions of the Pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V ±5%).

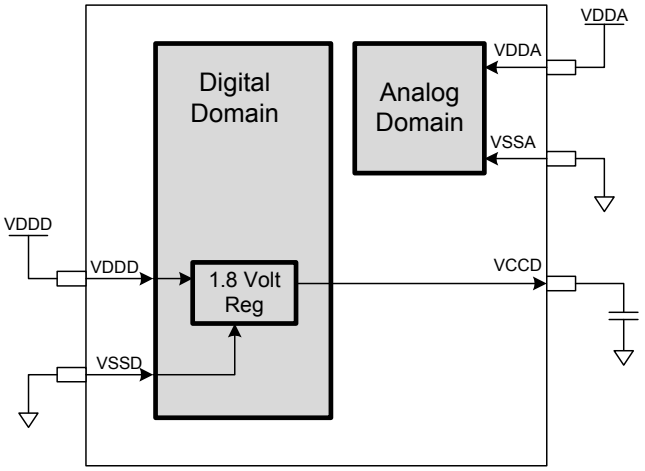
Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following packages are supported: 48-pin TQFP, 44-pin TQFP, 40-pin QFN, and 28-pin SSOP.

Power

The following power system diagrams show the minimum set of power supply pins as implemented for the PSoC 4200. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DDA} input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

Figure 12. PSoC 4 Power Supply



The PSoC 4200 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, PSoC 4200 is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4200 supplies the internal logic and the V_{CCD} output of PSoC 4200 must be bypassed to ground via an external capacitor (in the range of 1 µF to 1.6 µF; X5R ceramic or better).

V_{DDA} and V_{DDD} must be shorted together; the grounds, V_{SSA} and V_{SS} must also be shorted together. Bypass capacitors must be used from V_{DDD} to ground, typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 13. 48-TQFP Package Example

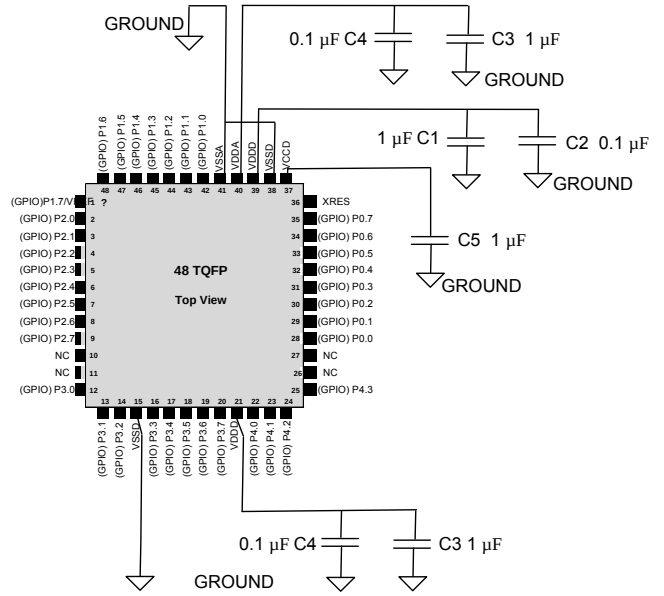
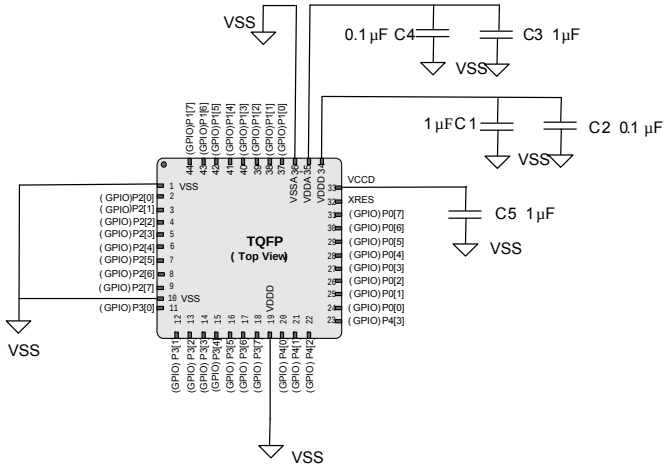


Figure 14. 44-TQFP Package Example



Power Supply	Bypass Capacitors
V_{DDD}–V_{SS}	0.1-µF ceramic at each pin (C2, C6) plus bulk capacitor 1 µF to 10 µF (C1). Total capacitance may be greater than 10 µF.
V_{DDA}–V_{SSA}	0.1-µF ceramic at pin (C4). Additional 1 µF to 10 µF (C3) bulk capacitor. Total capacitance may be greater than 10 µF.
V_{CCD}–V_{SS}	1-µF ceramic capacitor at the VCCD pin (C5)
V_{REF}–V_{SSA} (optional)	The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor. Total capacitance may be greater than 10 µF.

Development Support

The PSoC 4200 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4200 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 2. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID31	IDD26	I^2C wakeup and WDT on.	–	1.3	–	µA	T = 25 °C
SID32	IDD27	I^2C wakeup and WDT on.	–	–	45	µA	T = 85 °C
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V							
SID34	IDD29	I^2C wakeup and WDT on	–	1.5	15	µA	Typ. at 25 °C. Max at 85 °C.
Deep Sleep Mode, V_{DD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	IDD32	I^2C wakeup and WDT on.	–	1.7	–	µA	T = 25 °C
SID38	IDD33	I^2C wakeup and WDT on	–	–	60	µA	T = 85 °C
Deep Sleep Mode, +105 °C							
SID33Q	IDD28Q	I^2C wakeup and WDT on. Regulator Off.	–	–	135	µA	V_{DD} = 1.71 to 1.89
SID34Q	IDD29Q	I^2C wakeup and WDT on.	–	–	180	µA	V_{DD} = 1.8 to 3.6
SID35Q	IDD30Q	I^2C wakeup and WDT on.	–	–	140	µA	V_{DD} = 3.6 to 5.5
Hibernate Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID40	IDD35	GPIO and Reset active	–	150	-	nA	T = 25 °C
SID41	IDD36	GPIO and Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, V_{DD} = 3.6 V to 5.5 V							
SID43	IDD38	GPIO and Reset active	–	150	–	nA	T = 25 °C
Hibernate Mode, V_{DD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID46	IDD41	GPIO and Reset active	–	150	–	nA	T = 25 °C
SID47	IDD42	GPIO and Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, +105 °C							
SID42Q	IDD37Q	Regulator Off	–	–	19.4	µA	V_{DD} = 1.71 to 1.89
SID43Q	IDD38Q		–	–	17	µA	V_{DD} = 1.8 to 3.6
SID44Q	IDD39Q		–	–	16	µA	V_{DD} = 3.6 to 5.5
Stop Mode							
SID304	IDD43A	Stop Mode current; V_{DD} = 3.3 V	–	20	80	nA	Typ. at 25 °C. Max at 85 °C.
Stop Mode, +105 °C							
SID304Q	IDD43AQ	Stop Mode current; V_{DD} = 3.6 V	–	–	5645	nA	
XRES current							
SID307	IDD_XR	Supply current while XRES asserted	–	2	5	mA	

Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID50	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24 MHz IMO. Guaranteed by characterization
SID51	$T_{HIBERNATE}$	Wakeup from Hibernate and Stop modes	–	–	2	ms	Guaranteed by characterization
SID52	$T_{RESETWIDTH}$	External reset pulse width	1	–	–	µs	Guaranteed by characterization

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	µA	
SID270	I_{DD_MED}	Power = medium	–	550	950	µA	
SID271	I_{DD_LOW}	Power = low	–	150	350	µA	
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	VDDA – 0.2	V	
SID282	V_{CM}	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	VDDA – 0.2	V	
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–		
SID283	V_{OUT_1}	Power = high, Iload=10 mA	0.5	–	VDDA – 0.5	V	
SID284	V_{OUT_2}	Power = high, Iload=1 mA	0.2	–	VDDA – 0.2	V	
SID285	V_{OUT_3}	Power = medium, Iload=1 mA	0.2	–	VDDA – 0.2	V	
SID286	V_{OUT_4}	Power = low, Iload=0.1mA	0.2	–	VDDA – 0.2	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode. TA ≤ 85 °C
SID290Q	VOS_DR_TR	Offset voltage drift, trimmed	15	±3	15	µV/°C	High mode. TA ≤ 105 °C
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC	70	80	–	dB	V_{DDD} = 3.6 V
SID292	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V_{DDD} = 3.6 V
	Noise		–	–	–	–	
SID293	V_{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	µVrms	
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	V_{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	

Table 8. Opamp Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq$ 2.7 V	6	–	–	V/µs	
SID299	T_op_wake	From disable to enable, no external RC dominating	–	300	–	µs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	Guaranteed by design
	Comp_mode	Comparator mode; 50 mV drive, Trise = Tfall (approx.)	–	–	–		
SID300	T_{PD1}	Response time; power = high	–	150	–	ns	
SID301	T_{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T_{PD3}	Response time; power = low	–	2000	–	ns	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	

Comparatorr

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	$V_{OFFSET2}$	Input offset voltage, Common Mode voltage range from 0 to V_{DD}-1	–	–	±4	mV	
SID85A	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	–	±12	–	mV	
SID86	V_{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to V_{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2.
SID247	V_{ICM2}	Input common mode voltage in low power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	0	–	V_{DDD}	V	
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq$ 2.7 V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	V_{DDD} < 2.7 V. Guaranteed by characterization
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	Guaranteed by characterization
SID248	I_{CMP2}	Block current, low power mode	–	–	100	µA	Guaranteed by characterization
SID259	I_{CMP3}	Block current, ultra low power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	–	6	28	µA	Guaranteed by characterization

CSD

Table 14. CSD Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID.CSD#16	IDAC1IDD	IDAC1 (8 bits) block current	–	–	1125	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7 bits) block current	–	–	1125	µA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID308A	Vcompidac	Voltage compliance range of IDAC for S0	0.8	–	VDD-0.8	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise, 0.1-pF sensitivity	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1-pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8 bits) in High range	–	612	–	uA	
SID314A	IDAC1_CRT2	Output current of Idac1 (8 bits) in Low range	–	306	–	uA	
SID315	IDAC2_CRT1	Output current of Idac2 (7 bits) in High range	–	304.8	–	uA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7 bits) in Low range	–	152.4	–	uA	
SID320	IDACOFFSET	All zeroes input	–	–	±1	LSB	
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH	Mismatch between IDACs	–	–	7	LSB	
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

System Resources

Power-on-Reset (POR) with Brown Out

Table 28. Imprecise Power On Reset (IPOR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	$V_{IPORHYST}$	Hysteresis	15	–	200	mV	Guaranteed by characterization

Table 29. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.64	–	–	V	Full functionality between 1.71 V and BOD trip voltage is guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization
BID55	Svdd	Maximum power supply ramp rate	–	–	67	kV/sec	

Voltage Monitors

Table 30. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID195	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	–	–	100	µA	Guaranteed by characterization

Table 31. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	Guaranteed by characterization

Table 39. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID256*	T_{WS48}*	Number of wait states at 48 MHz	1	–	–		CPU execution from Flash. Guaranteed by characterization
SID257	T_{WS24}*	Number of wait states at 24 MHz	0	–	–		CPU execution from Flash. Guaranteed by characterization
SID260	V_{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of Vbg (1.024 V). Guaranteed by characterization
SID262	$T_{CLKSWITCH}$	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	. Guaranteed by design
* Tws48 and Tws24 are guaranteed by Design							

Table 40. UDB Port Adaptor Specifications

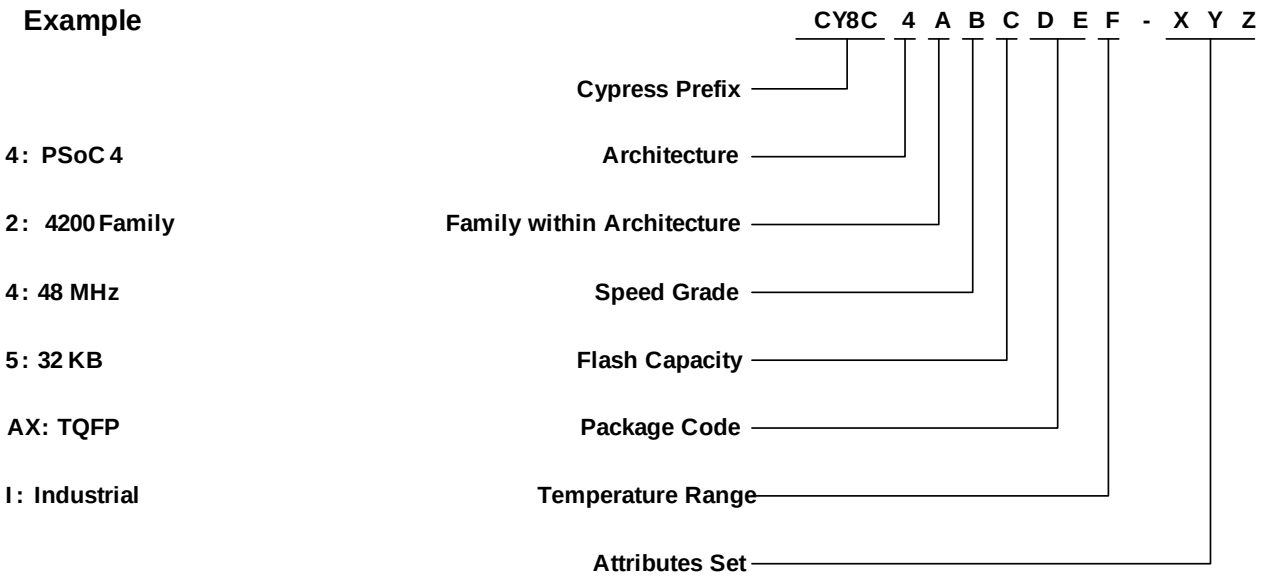
(Based on LPC Component Specs, Guaranteed by Characterization -10-pF load, 3-V V_{DDIO} and V_{DDD})

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID263	T_{LCLKDO}	LCLK to output delay	–	–	18	ns	
SID264	$T_{DINLCLK}$	Input setup time to LCLCK rising edge	–	–	7	ns	
SID265	$T_{DINLCLKHLD}$	Input hold time from LCLK rising edge	5	–	–	ns	
SID266	$T_{LCLKHIZ}$	LCLK to output tristated	–	–	28	ns	
SID267	T_{FLCLK}	LCLK frequency	–	–	33	MHz	
SID268	$T_{LCLKDUTY}$	LCLK duty cycle (percentage high)	40	–	60	%	

Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.



The Field Values are listed in the following table.

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	1	4100 Family
		2	4200 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
DE	Package Code	AX, AZ	TQFP
		LQ	QFN
		PV	SSOP
		FN	WLCSP
F	Temperature Range	I	Industrial
		Q	Extended Industrial
XYZ	Attributes Code	000-999	Code of feature set in specific family

Packaging

Table 42. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25.00	105	°C
T_J	Operating junction temperature		–40	–	125	°C
T_{JA}	Package θ_{JA} (28-pin SSOP)		–	66.58	–	°C/Watt
T_{JA}	Package θ_{JA} (35-ball WLCSP)		–	28.00	–	°C/Watt
T_{JA}	Package θ_{JA} (40-pin QFN)		–	15.34	–	°C/Watt
T_{JA}	Package θ_{JA} (44-pin TQFP)		–	57.16	–	°C/Watt
T_{JA}	Package θ_{JA} (48-pin TQFP)		–	67.30	–	°C/Watt
T_{JC}	Package θ_{JC} (28-pin SSOP)		–	26.28	–	°C/Watt
T_{JC}	Package θ_{JC} (35-ball WLCSP)		–	00.40	–	°C/Watt
T_{JC}	Package θ_{JC} (40-pin QFN)		–	2.50	–	°C/Watt
T_{JC}	Package θ_{JC} (44-pin TQFP)		–	17.47	–	°C/Watt
T_{JC}	Package θ_{JC} (48-pin TQFP)		–	27.60	–	°C/Watt

Table 43. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
28-pin SSOP	260 °C	30 seconds
35-ball WLCSP	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin TQFP	260 °C	30 seconds

Table 44. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
28-pin SSOP	MSL 3
35-ball WLCSP	MSL 3
40-pin QFN	MSL 3
44-pin TQFP	MSL 3
48-pin TQFP	MSL 3

PSoC 4 CAB Libraries with Schematics Symbols and PCB Footprints are on the Cypress web site at http://www.cypress.com/cad-resources/psoc-4-cad-libraries?source=search&cat=technical_documents.

Figure 17. 28-pin (210-mil) SSOP Package Outline

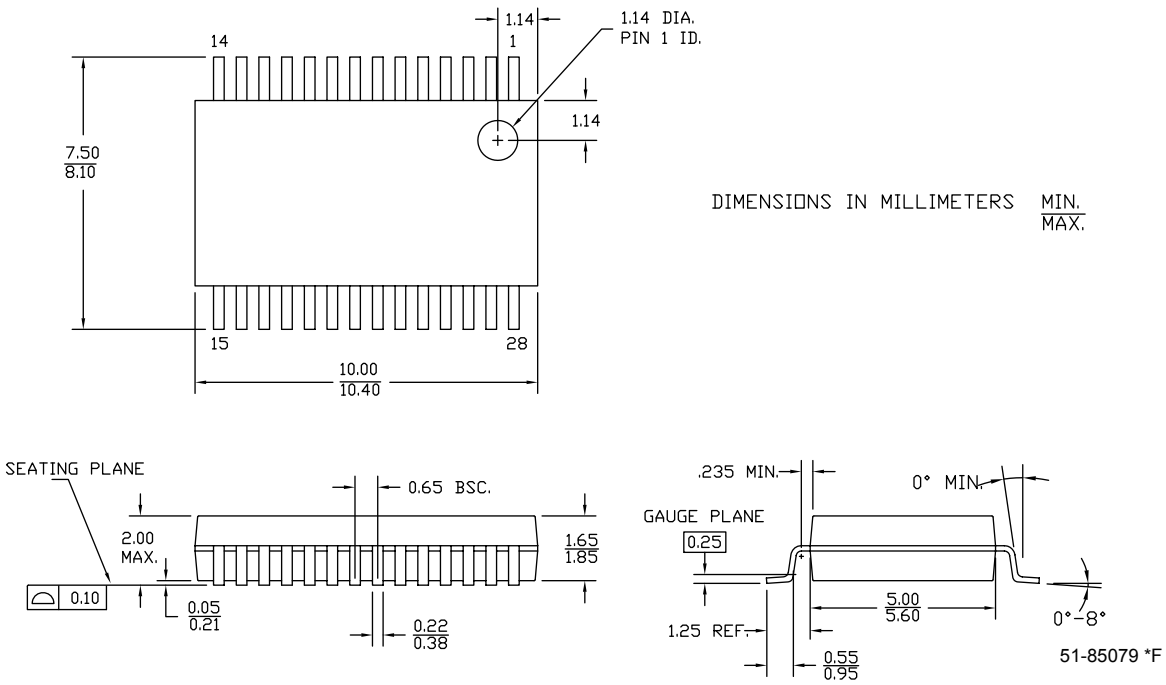
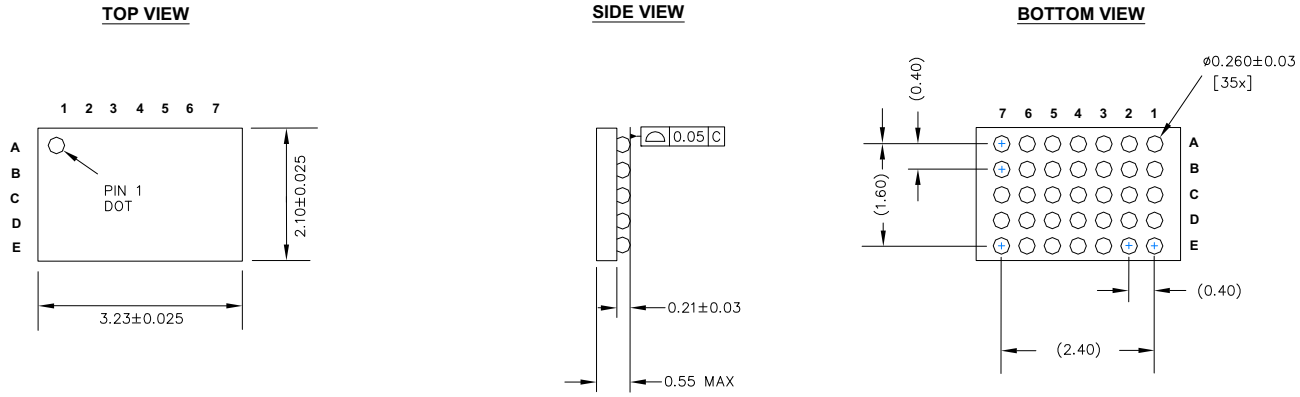


Figure 18. 35-ball WLCSP Package Outline



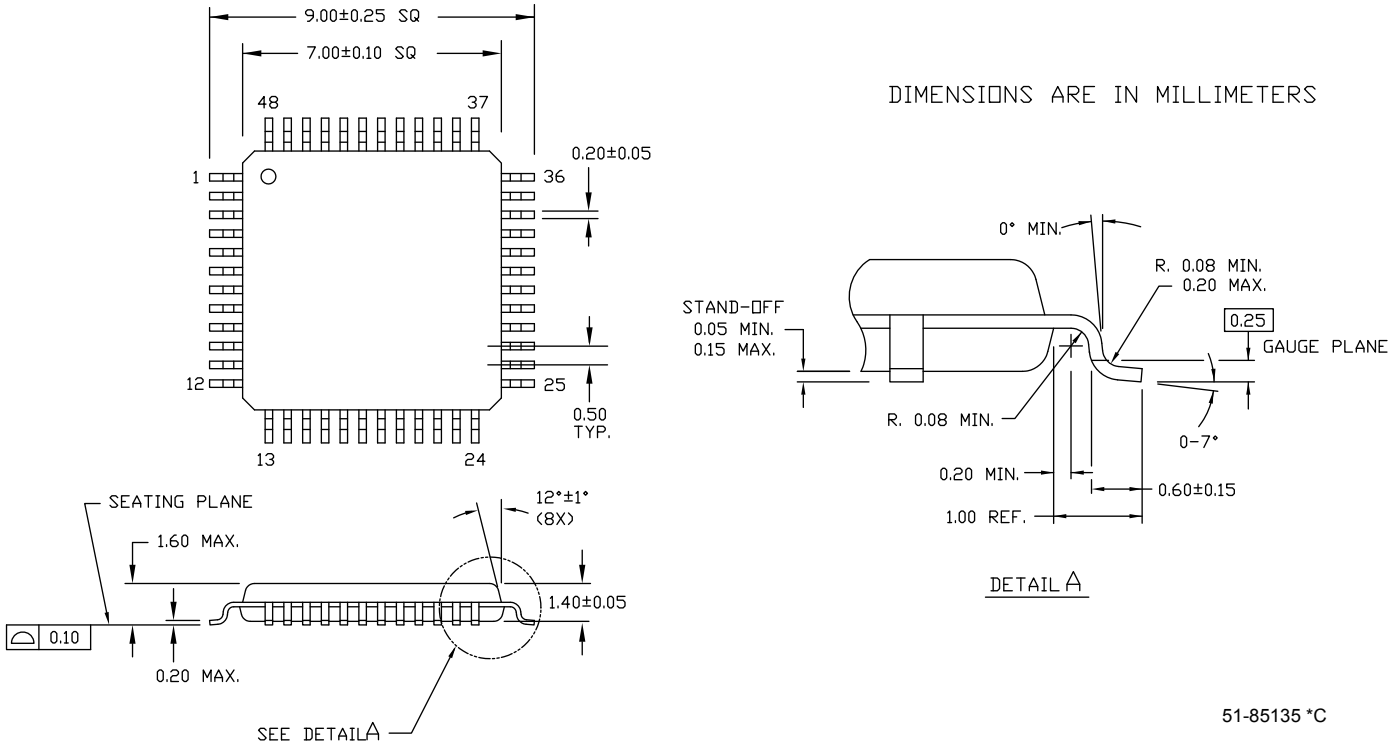
NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18

2. ALL DIMENSIONS ARE IN MILLIMETERS

001-93741 **

Figure 21. 48-Pin TQFP Package Outline



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