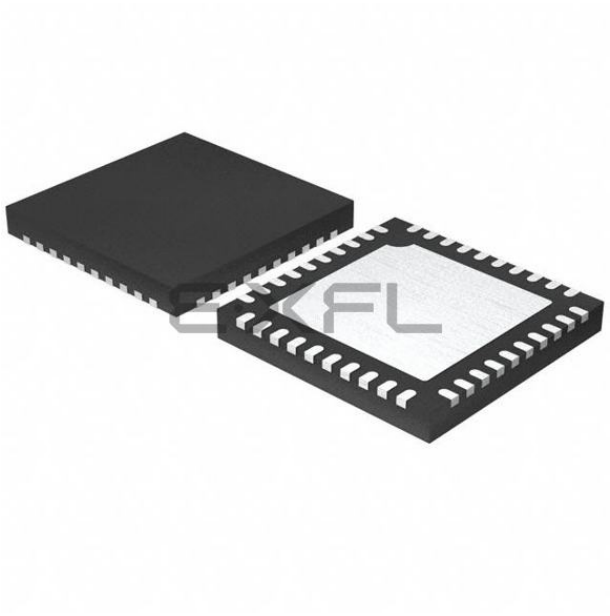

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4244lqi-443

Contents

Two Opamps (CTBm Block)

PSoC 4200 has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the S/H circuit of the ADC without requiring external buffering.

Temperature Sensor

PSoC 4200 has one on-chip temperature sensor This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress supplied software that includes calibration and linearization.

Low-power Comparators

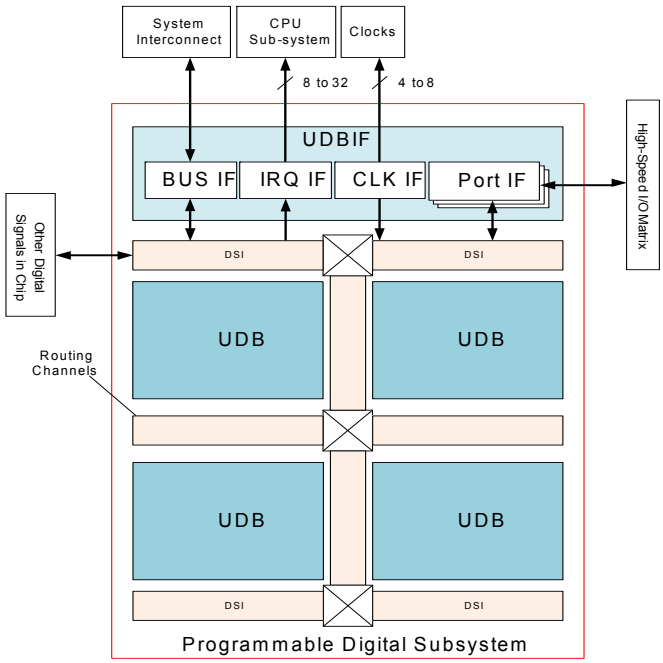
PSoC 4200 has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

PSoC 4200 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

Figure 5. UDB Array

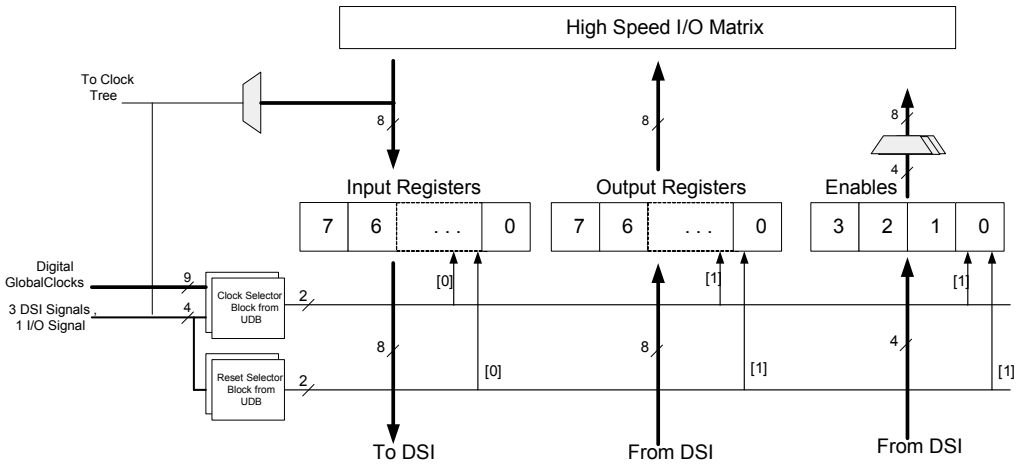


UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see Figure 6).

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to any pin on the chip through the DSI.

Figure 6. Port Interface



Fixed Function Digital

Timer/Counter/PWM Block (TCPWM)

The TCPWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

Serial Communication Blocks (SCB)

PSoC 4200 has two SCBs, which can each implement an I^2C, UART, or SPI interface.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes. The I^2C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. The required Rise and Fall times for different I^2C speeds are guaranteed by using appropriate pull-up resistor values depending on VDD, Bus Capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, refer to the UM10204 I2C bus specification and user manual (the latest revision is available at www.nxp.com).

PSoC 4200 is not completely compliant with the I^2C spec in the following respects:

- GPIO cells are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-Mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast mode and Fast-Mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I^2C master, it interposes an IDLE state between NACK and Repeated Start; the I^2C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in I^2C slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its I^2C address must be even.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

GPIO

PSoC 4200 has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4200 since it has 4.5 ports).

Special Function Peripherals

LCD Segment Drive

PSoC 4200 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in PSoC 4200 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

WLCSP Package Bootloader

The WLCSP package is supplied with an I^2C Bootloader installed in flash. The bootloader is compatible with PSoC Creator bootloadable project files and has the following default settings:

- I^2C SCL and SDA connected to port pins P4.0 and P4.1 respectively (external pull-up resistors required)
- I^2C Slave mode, address 8, data rate = 100 kbps
- Single application
- Wait two seconds for bootload command
- Other bootloader options are as set by the PSoC Creator Bootloader Component default
- Occupies the bottom 4.5 KB of flash

For more information on this bootloader, see the following Cypress application note:

AN73854 - Introduction to Bootloaders

Note that a PSoC Creator bootloadable project must be associated with *.hex* and *.elf* files for a bootloader project that is configured for the target device. Bootloader *.hex* and *.elf* files can be found at http://www.cypress.com/?rID=78632. The factory-installed bootloader can be overwritten using JTAG or SWD programming.

Pinouts

The following is the pin-list for the PSoC 4200 (44-TQFP, 40-QFN, 28-SSOP, and 48-TQFP). Port 2 comprises of the high-speed Analog inputs for the SAR Mux. P1.7 is the optional external input and bypass for the SAR reference. Ports 3 and 4 contain the Digital Communication channels. All pins support CSD CapSense and Analog Mux Bus connections.

44-TQFP		40-QFN		28-SSOP		48-TQFP		Alternate Functions for Pins					Pin Description
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
1	VSS	–	–	–	–	–	–	–	–	–	–	–	Ground
2	P2.0	1	P2.0	–	–	2	P2.0	sarmux.0	–	–	–	–	Port 2 Pin 0: gpio, lcd, csd, sarmux
3	P2.1	2	P2.1	–	–	3	P2.1	sarmux.1	–	–	–	–	Port 2 Pin 1: gpio, lcd, csd, sarmux
4	P2.2	3	P2.2	5	P2.2	4	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
5	P2.3	4	P2.3	6	P2.3	5	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
6	P2.4	5	P2.4	7	P2.4	6	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
7	P2.5	6	P2.5	8	P2.5	7	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
8	P2.6	7	P2.6	9	P2.6	8	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
9	P2.7	8	P2.7	10	P2.7	9	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
10	VSS	9	VSS	–	–	–	–	–	–	–	–	–	Ground
–	–	–	–	–	–	10	NC	–	–	–	–	–	No Connect
–	–	–	–	–	–	11	NC	–	–	–	–	–	No Connect
11	P3.0	10	P3.0	11	P3.0	12	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
12	P3.1	11	P3.1	12	P3.1	13	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
13	P3.2	12	P3.2	13	P3.2	14	P3.2	–	tcpwm1_p[0]	–	swd_io[0]	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
–	–	–	–	–	–	15	VSSD	–	–	–	–	–	Ground
14	P3.3	13	P3.3	14	P3.3	16	P3.3	–	tcpwm1_n[0]	–	swd_clk[0]	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
15	P3.4	14	P3.4	–	–	17	P3.4	–	tcpwm2_p[0]	–	–	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
16	P3.5	15	P3.5	–	–	18	P3.5	–	tcpwm2_n[0]	–	–	scb1_spi_ssel_2	Port 3 Pin 5: gpio, lcd, csd, pwm, scb1
17	P3.6	16	P3.6	–	–	19	P3.6	–	tcpwm3_p[0]	–	swd_io[1]	scb1_spi_ssel_3	Port 3 Pin 6: gpio, lcd, csd, pwm, scb1, swd
18	P3.7	17	P3.7	–	–	20	P3.7	–	tcpwm3_n[0]	–	swd_clk[1]	–	Port 3 Pin 7: gpio, lcd, csd, pwm, swd
19	VDDD	–	–	–	–	21	VDDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5V
20	P4.0	18	P4.0	15	P4.0	22	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
21	P4.1	19	P4.1	16	P4.1	23	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
22	P4.2	20	P4.2	17	P4.2	24	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
23	P4.3	21	P4.3	18	P4.3	25	P4.3	csd_c_sh_tank	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
–	–	–	–	–	–	26	NC	–	–	–	–	–	No Connect
–	–	–	–	–	–	27	NC	–	–	–	–	–	No Connect

44-TQFP		40-QFN		28-SSOP		48-TQFP		Alternate Functions for Pins					Pin Description
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
24	P0.0	22	P0.0	19	P0.0	28	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
25	P0.1	23	P0.1	20	P0.1	29	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
26	P0.2	24	P0.2	21	P0.2	30	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
27	P0.3	25	P0.3	22	P0.3	31	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
28	P0.4	26	P0.4	–	–	32	P0.4	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
29	P0.5	27	P0.5	–	–	33	P0.5	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
30	P0.6	28	P0.6	23	P0.6	34	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
31	P0.7	29	P0.7	24	P0.7	35	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
32	XRES	30	XRES	25	XRES	36	XRES	–	–	–	–	–	Chip reset, active low
33	VCCD	31	VCCD	26	VCCD	37	VCCD	–	–	–	–	–	Regulated supply, connect to 1µF cap or 1.8V
–	–	–	–	–	–	38	VSSD	–	–	–	–	–	Digital Ground
34	VDDD	32	VDDD	27	VDD	39	VDDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5V
35	VDDA	33	VDDA	27	VDD	40	VDDA	–	–	–	–	–	Analog Supply, 1.8 - 5.5V, equal to VDDD
36	VSSA	34	VSSA	28	VSS	41	VSSA	–	–	–	–	–	Analog Ground
37	P1.0	35	P1.0	1	P1.0	42	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
38	P1.1	36	P1.1	2	P1.1	43	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
39	P1.2	37	P1.2	3	P1.2	44	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
40	P1.3	38	P1.3	–	–	45	P1.3	ctb.oa1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
41	P1.4	39	P1.4	–	–	46	P1.4	ctb.oa1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
42	P1.5	–	–	–	–	47	P1.5	ctb.oa1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
43	P1.6	–	–	–	–	48	P1.6	ctb.oa0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
44	P1.7/VREF	40	P1.7/VREF	4	P1.7/VREF	1	P1.7/VREF	ctb.oa1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Notes:

1. tcpwm_p and tcpwm_n refer to tcpwm non-inverted and inverted outputs respectively.
2. P3.2 and P3.3 are SWD pins after boot (reset).

Figure 7. 48-Pin TQFP Pinout

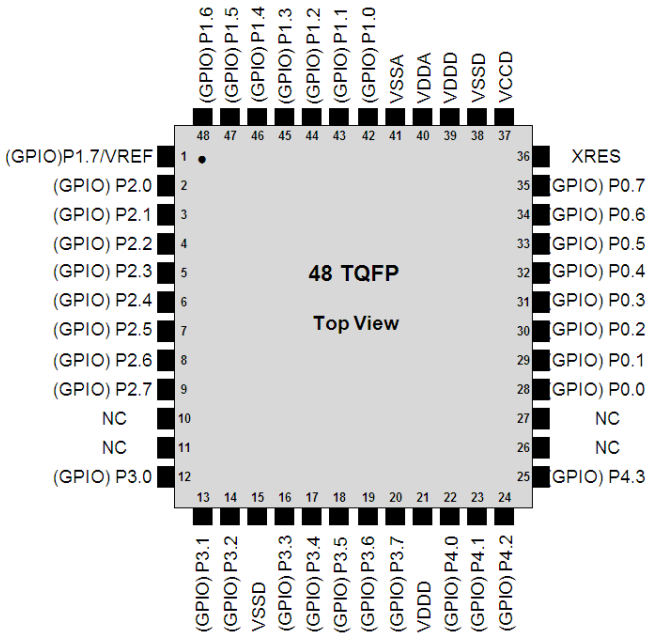


Figure 8. 44-pin TQFP Part Pinout

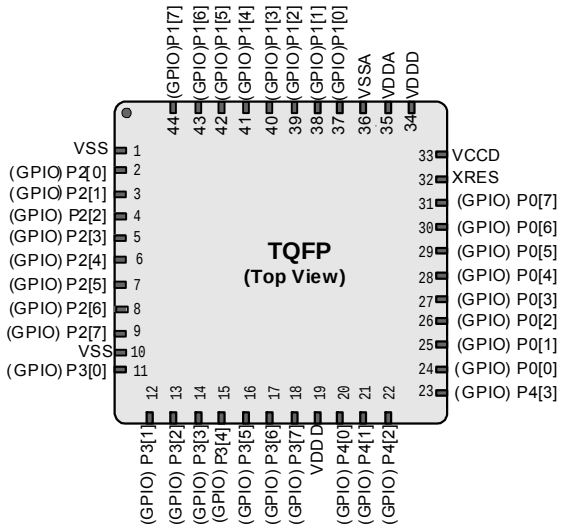


Figure 9. 40-Pin QFN Pinout

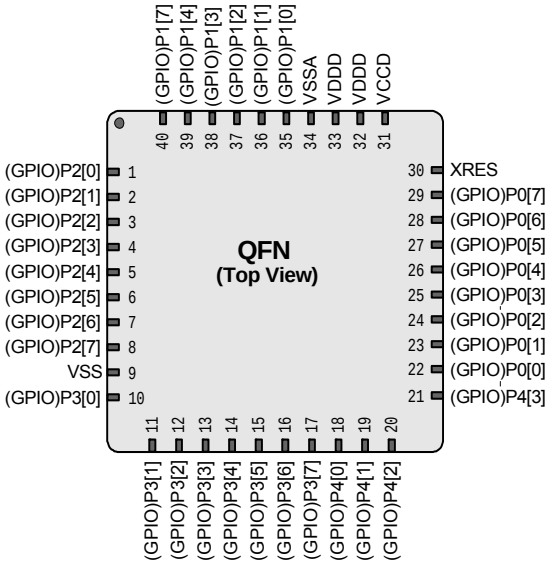


Figure 10. 35-Ball WLCSP

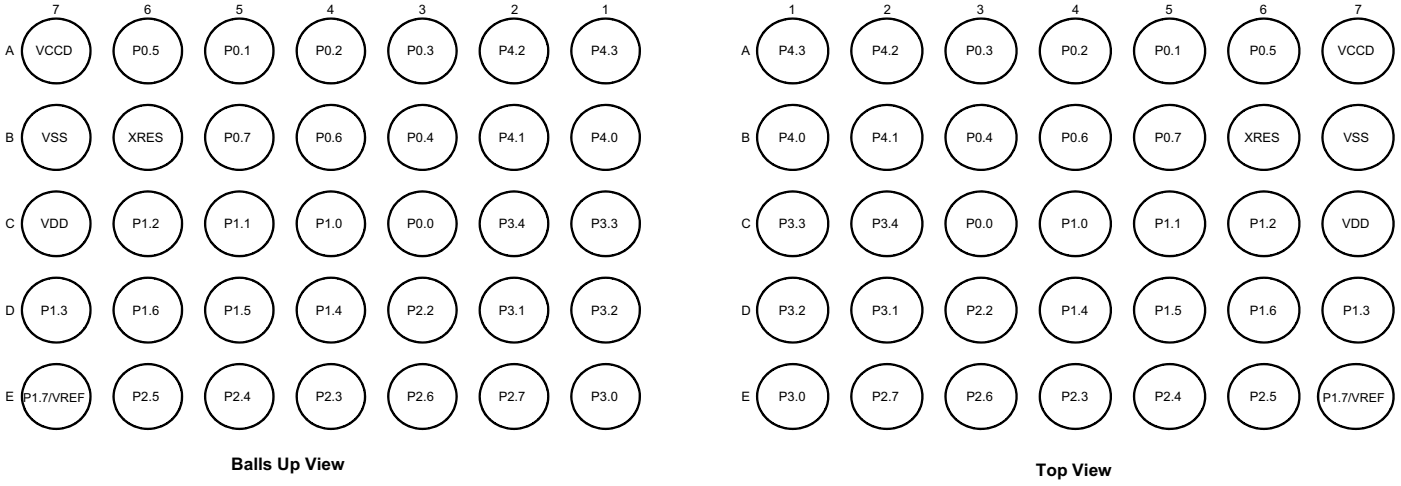
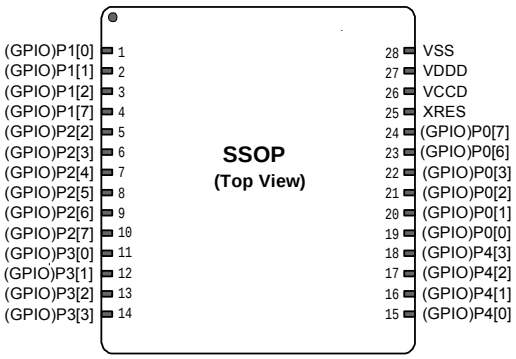


Figure 11. 28-Pin SSOP Pinout



Development Support

The PSoC 4200 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4200 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SSD}	–0.5	–	6	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	–0.5	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–200	–	200	mA	

Device Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 105 °C and TJ ≤ 125 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power Supply Input Voltage (V_{DDA} = V_{DDD} = V_{DD})	1.8	–	5.5	V	With regulator enabled
SID255	V_{DDD}	Power Supply Input Voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	
SID55	CEFC	External Regulator voltage bypass	1	1.3	1.6	µF	X5R ceramic or better
SID56	CEXC	Power supply decoupling capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V. Typical Values measured at V_{DD} = 3.3 V							
SID9	IDD4	Execute from Flash; CPU at 6 MHz	–	–	2.8	mA	
SID10	IDD5	Execute from Flash; CPU at 6 MHz	–	2.2	–	mA	T = 25 °C
SID12	IDD7	Execute from Flash; CPU at 12 MHz,	–	–	4.2	mA	
SID13	IDD8	Execute from Flash; CPU at 12 MHz	–	3.7	–	mA	T = 25 °C
SID16	IDD11	Execute from Flash; CPU at 24 MHz	–	6.7	–	mA	T = 25 °C
SID17	IDD12	Execute from Flash; CPU at 24 MHz	–	–	7.2	mA	
SID19	IDD14	Execute from Flash; CPU at 48 MHz	–	12.8	–	mA	T = 25 °C
SID20	IDD15	Execute from Flash; CPU at 48 MHz	–	–	13.8	mA	
Sleep Mode, V_{DD} = 1.7 V to 5.5 V							
SID25	IDD20	I^2C wakeup, WDT, and Comparators on. 6 MHz.	–	1.3	1.8	mA	V_{DD} = 1.71 to 5.5 V.
SID25A	IDD20A	I^2C wakeup, WDT, and Comparators on. 12 MHz	–	1.7	2.2	mA	V_{DD} = 1.71 to 5.5 V.

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[2]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID241	V_{IH}[2]	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	
SID243	V_{IH}[2]	LVTTL input, $V_{DDD} \geq$ 2.7 V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq$ 2.7 V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 8 mA at 3-V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3-V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	
SID66	C_{IN}	Input capacitance	–	–	7	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq$ 2.7 V. Guaranteed by characterization
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DD}/Vss	–	–	100	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Table 8. Opamp Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq$ 2.7 V	6	–	–	V/µs	
SID299	T_op_wake	From disable to enable, no external RC dominating	–	300	–	µs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	Guaranteed by design
	Comp_mode	Comparator mode; 50 mV drive, Trise = Tfall (approx.)	–	–	–		
SID300	T_{PD1}	Response time; power = high	–	150	–	ns	
SID301	T_{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T_{PD3}	Response time; power = low	–	2000	–	ns	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	

Comparatorr

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	$V_{OFFSET2}$	Input offset voltage, Common Mode voltage range from 0 to V_{DD}-1	–	–	±4	mV	
SID85A	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	–	±12	–	mV	
SID86	V_{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to V_{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2.
SID247	V_{ICM2}	Input common mode voltage in low power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	0	–	V_{DDD}	V	
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq$ 2.7 V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	V_{DDD} < 2.7 V. Guaranteed by characterization
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	Guaranteed by characterization
SID248	I_{CMP2}	Block current, low power mode	–	–	100	µA	Guaranteed by characterization
SID259	I_{CMP3}	Block current, ultra low power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	–	6	28	µA	Guaranteed by characterization

Table 12. SAR ADC DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID111	A_INL	Integral non linearity	–1.7	–	+2	LSB	V_{DD} = 1.71 to 5.5, 1 Msps, Vref = 1 to 5.5.
SID111A	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V_{DDD} = 1.71 to 3.6, 1 Msps, Vref = 1.71 to V_{DDD}.
SID111B	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V_{DDD} = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5.
SID112	A_DNL	Differential non linearity	–1	–	+2.2	LSB	V_{DDD} = 1.71 to 5.5, 1 Msps, Vref = 1 to 5.5.
SID112A	A_DNL	Differential non linearity	–1	–	+2	LSB	V_{DDD} = 1.71 to 3.6, 1 Msps, Vref = 1.71 to V_{DDD}.
SID112B	A_DNL	Differential non linearity	–1	–	+2.2	LSB	V_{DDD} = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5.

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	1	Msps	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	Ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	Ksps	
SID109	A_SNDR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz.

LCD Direct Drive

Table 18. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	
SID157	I_{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO. 25 °C	–	0.6	–	mA	32 × 4 segments. 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO. 25 °C	–	0.5	–	mA	32 × 4 segments. 50 Hz

Table 19. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	

Table 20. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	
SID161	I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

Table 21. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID162	F_{UART}	Bit rate	–	–	1	Mbps

SPI Specifications

Table 22. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID163	I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA
SID164	I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA
SID165	I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA

Table 23. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz

SWD Interface

Table 32. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	
SID220	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	
SID221	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	
SID222	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	

Table 34. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if T_A > 85 °C and IMO frequency < 24 MHz
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12	µs	
SID227	$T_{JITRMSIMO1}$	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	$T_{JITRMSIMO2}$	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Ordering Information

The PSoC 4200 part numbers and features are listed in the following table.

Table 41. PSoC 4200 Family Ordering Information

Family	MPN	Features												Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CapSense	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	GPIO	28-SSOP	35-WLCSP	40-QFN	44-TQFP	48-TQFP
4200	CY8C4244PVI-432	48	16	4	2	1	-	-	1 Msps	2	4	2	24	√				
	CY8C4244PVI-442	48	16	4	2	1	√	√	1 Msps	2	4	2	24	√				
	CY8C4244PVQ-432	48	16	4	2	1	-	-	1 Msps	2	4	2	24	√				
	CY8C4244PVQ-442	48	16	4	2	1	√	√	1 Msps	2	4	2	24	√				
	CY8C4244FNI-443	48	16	4	2	2	√	√	1 Msps	2	4	2	31		√			
	CY8C4244LQI-443	48	16	4	2	2	√	√	1 Msps	2	4	2	34			√		
	CY8C4244AXI-443	48	16	4	2	2	√	√	1 Msps	2	4	2	36				√	
	CY8C4244LQQ-443	48	16	4	2	2	√	√	1 Msps	2	4	2	34			√		
	CY8C4244AXQ-443	48	16	4	2	2	√	√	1 Msps	2	4	2	36				√	
	CY8C4244AZI-443	48	16	4	2	2	√	√	1 Msps	2	4	2	36					√
	CY8C4245AXI-473	48	32	4	4	2	-	-	1 Msps	2	4	2	36				√	
	CY8C4245AXQ-473	48	32	4	4	2	-	-	1 Msps	2	4	2	36				√	
	CY8C4245AZI-473	48	32	4	4	2	-	-	1 Msps	2	4	2	36					√
	CY8C4245PVI-482	48	32	4	4	1	√	√	1 Msps	2	4	2	24	√				
	CY8C4245PVQ-482	48	32	4	4	1	√	√	1 Msps	2	4	2	24	√				
	CY8C4245FNI-483(T)	48	32	4	4	2	√	√	1 Msps	2	4	2	31		√			
	CY8C4245LQI-483	48	32	4	4	2	√	√	1 Msps	2	4	2	34			√		
	CY8C4245AXI-483	48	32	4	4	2	√	√	1 Msps	2	4	2	36				√	
	CY8C4245LQQ-483	48	32	4	4	2	√	√	1 Msps	2	4	2	34			√		
	CY8C4245AXQ-483	48	32	4	4	2	√	√	1 Msps	2	4	2	36				√	
	CY8C4245AZI-483	48	32	4	4	2	√	√	1 Msps	2	4	2	36					√

Figure 17. 28-pin (210-mil) SSOP Package Outline

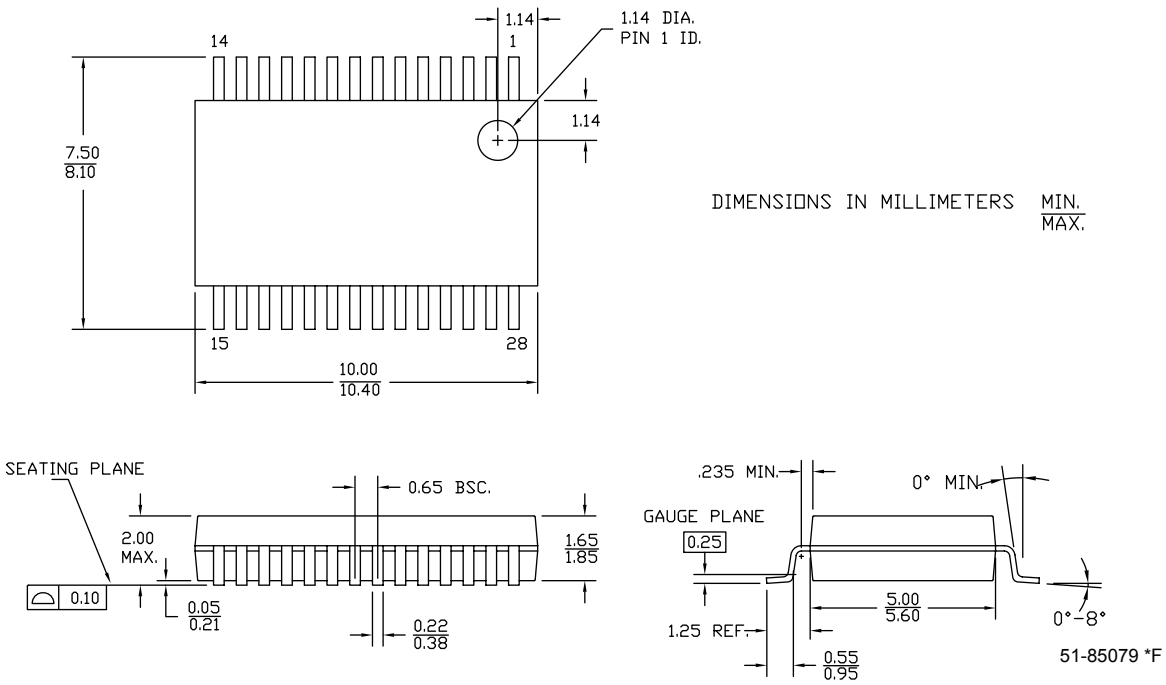
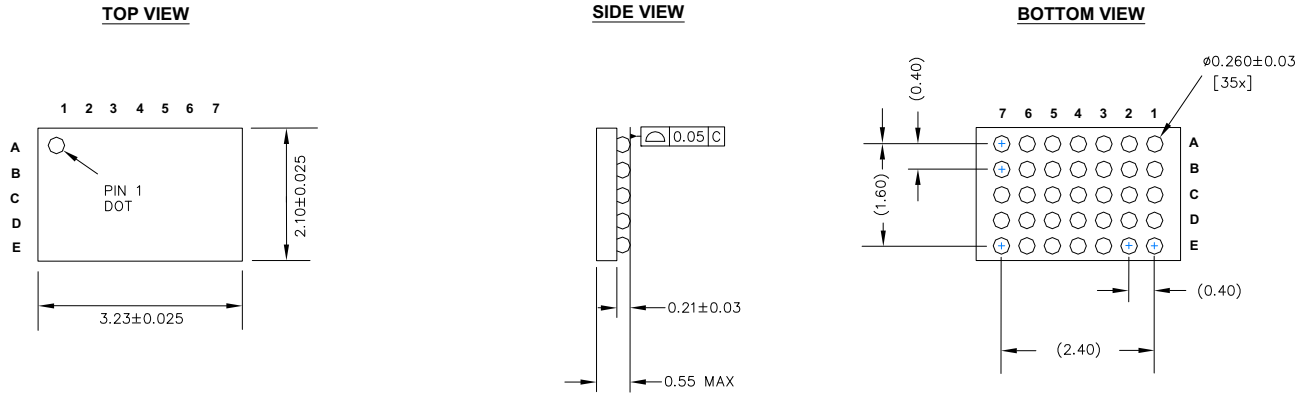


Figure 18. 35-ball WLCSP Package Outline



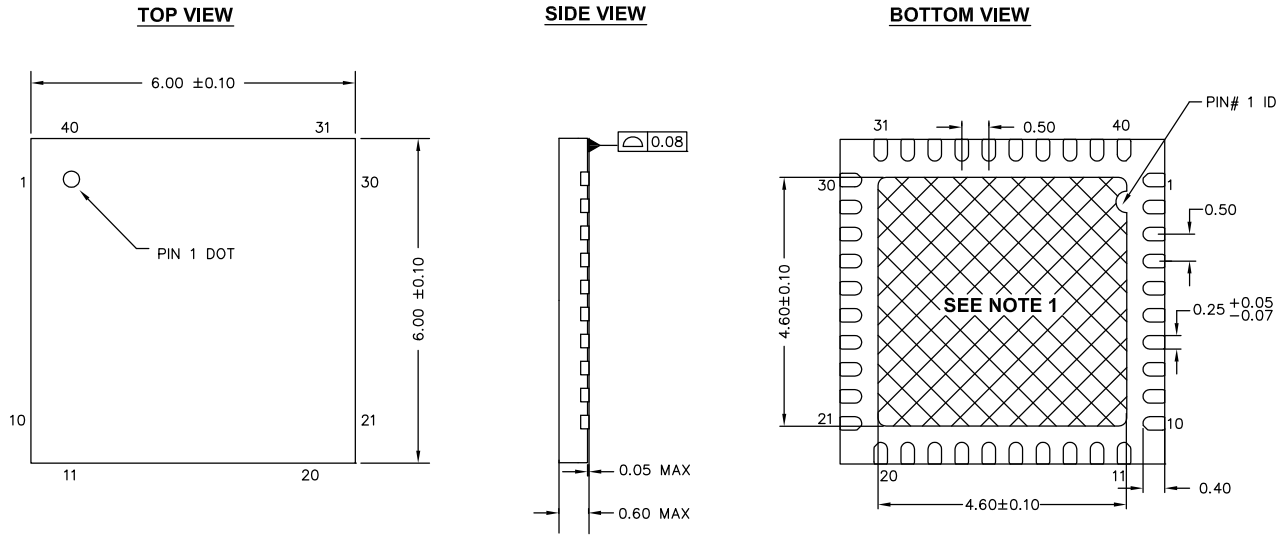
NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18

2. ALL DIMENSIONS ARE IN MILLIMETERS

001-93741 **

Figure 19. 40-pin QFN Package Outline



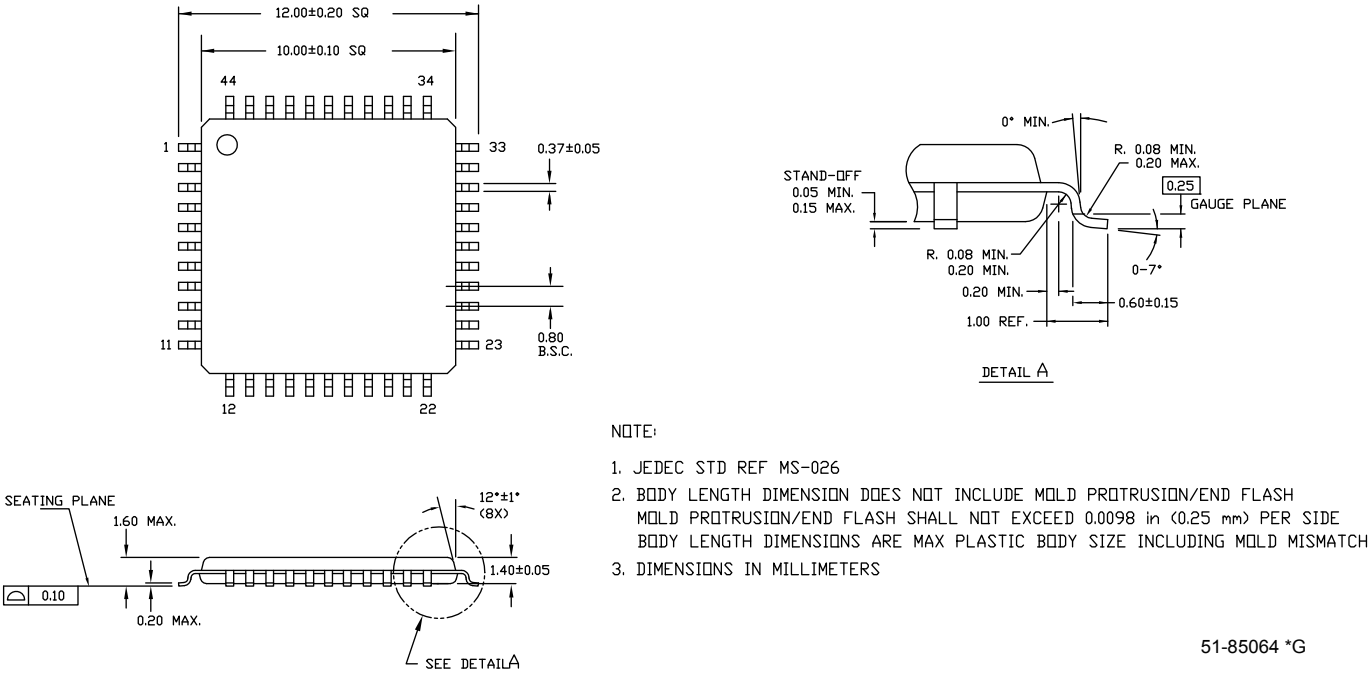
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 20. 44-pin TQFP Package Outline



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

Acronyms

Table 45. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 45. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD