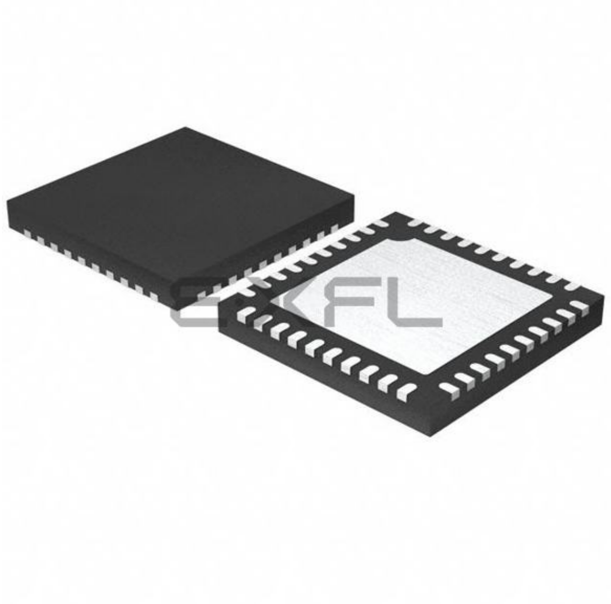


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4245lqi-483

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
  - AN90071: CY8CMBRxxx CapSense Design Guide
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

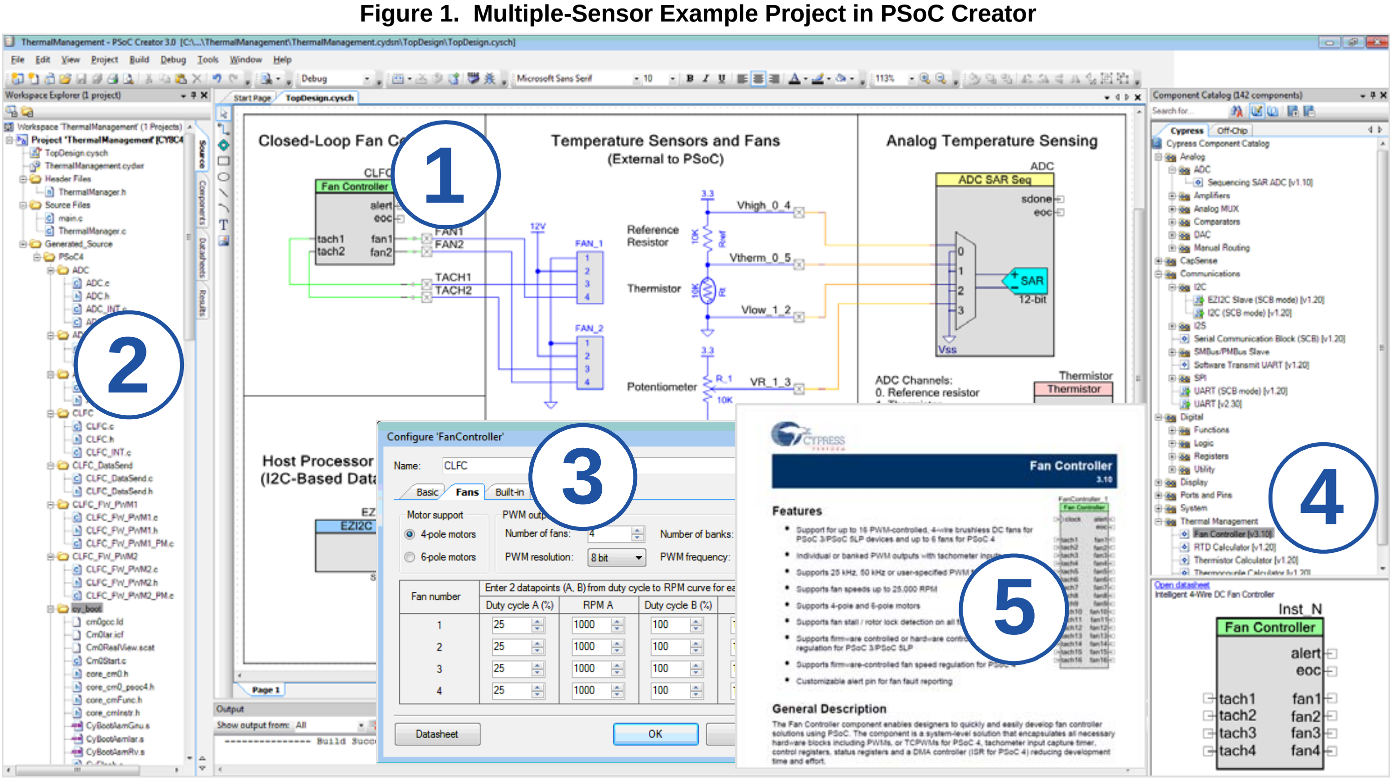
The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in PSoC 4200 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4200 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4200 Flash supports the following flash protection modes at the memory subsystem level:

- **Open: No Protection.** Factory default mode in which the product is shipped.
- **Protected: User may change from Open to Protected.** This mode disables Debug interface accesses. The mode can be set back to Open but only after completely erasing the Flash.
- **Kill: User may change from Open to Kill.** This mode disables all Debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrevocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

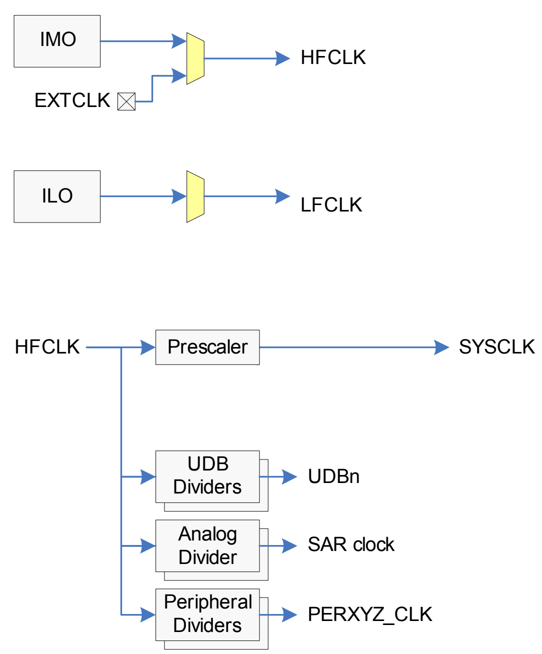
The power system is described in detail in the section Power on page 16. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4200 operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4200 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4200 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO) and a provision for an external clock.

Figure 3. PSoC 4200 MCU Clocking Architecture



The HFCLK signal can be divided down (see PSoC 4200 MCU Clocking Architecture) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4200, each with 16-bit divide capability; this allows eight to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator. When UDB-generated pulse interrupts are used, SYSCLK must equal HFCLK.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 4200. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 48 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low-power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

PSoC 4200 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4200 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal to noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

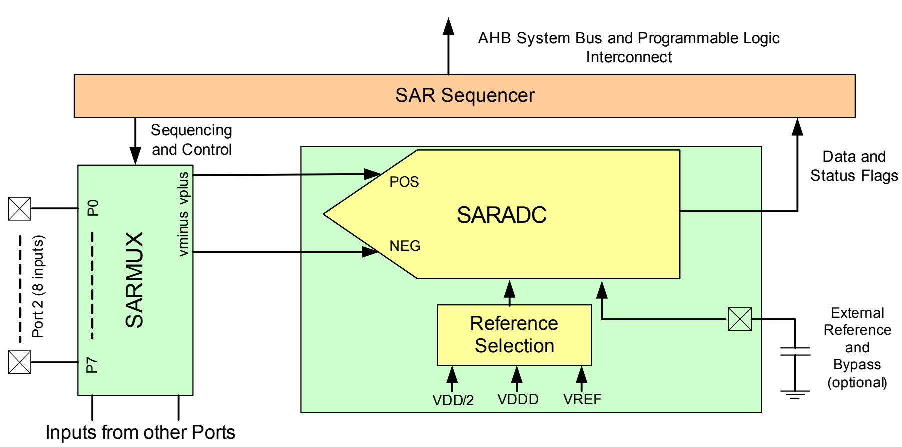
The 12-bit 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice (for the PSoC-4200 case) of three internal voltage references: V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 4. SAR ADC System Diagram



44-TQFP		40-QFN		28-SSOP		48-TQFP		Alternate Functions for Pins					Pin Description
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
24	P0.0	22	P0.0	19	P0.0	28	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
25	P0.1	23	P0.1	20	P0.1	29	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
26	P0.2	24	P0.2	21	P0.2	30	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
27	P0.3	25	P0.3	22	P0.3	31	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
28	P0.4	26	P0.4	–	–	32	P0.4	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
29	P0.5	27	P0.5	–	–	33	P0.5	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
30	P0.6	28	P0.6	23	P0.6	34	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
31	P0.7	29	P0.7	24	P0.7	35	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
32	XRES	30	XRES	25	XRES	36	XRES	–	–	–	–	–	Chip reset, active low
33	VCCD	31	VCCD	26	VCCD	37	VCCD	–	–	–	–	–	Regulated supply, connect to 1µF cap or 1.8V
–	–	–	–	–	–	38	VSSD	–	–	–	–	–	Digital Ground
34	VDDD	32	VDDD	27	VDD	39	VDDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5V
35	VDDA	33	VDDA	27	VDD	40	VDDA	–	–	–	–	–	Analog Supply, 1.8 - 5.5V, equal to VDDD
36	VSSA	34	VSSA	28	VSS	41	VSSA	–	–	–	–	–	Analog Ground
37	P1.0	35	P1.0	1	P1.0	42	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
38	P1.1	36	P1.1	2	P1.1	43	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
39	P1.2	37	P1.2	3	P1.2	44	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
40	P1.3	38	P1.3	–	–	45	P1.3	ctb.oa1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
41	P1.4	39	P1.4	–	–	46	P1.4	ctb.oa1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
42	P1.5	–	–	–	–	47	P1.5	ctb.oa1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
43	P1.6	–	–	–	–	48	P1.6	ctb.oa0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
44	P1.7/VREF	40	P1.7/VREF	4	P1.7/VREF	1	P1.7/VREF	ctb.oa1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Notes:

1. tcpwm_p and tcpwm_n refer to tcpwm non-inverted and inverted outputs respectively.
2. P3.2 and P3.3 are SWD pins after boot (reset).

The following is the pin-list for the PSoC 4200 (35-WLCSP).

35-Ball CSP		Alternate Functions for Pins					Pin Description
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
D3	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
E4	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
E5	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
E6	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
E3	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
E2	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
E1	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
D2	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
D1	P3.2	–	tcpwm1_p[0]	–	swd_io[0]	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
B7	VSS	–	–	–	–	–	Ground
C1	P3.3	–	tcpwm1_n[0]	–	swd_clk[0]	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
C2	P3.4	–	tcpwm2_p[0]	-	–	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
B1	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
B2	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
A2	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
A1	P4.3	csd_c_sh_tank	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
C3	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
A5	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
A4	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
A3	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
B3	P0.4	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
A6	P0.5	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
B4	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
B5	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
B6	XRES	–	–	–	–	–	Chip reset, active low
A7	VCCD	–	–	–	–	–	Regulated supply, connect to 1µF cap or 1.8V
C7	VDD	–	–	–	–	–	Supply, 1.8 - 5.5V
C4	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
C5	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
C6	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm

Development Support

The PSoC 4200 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4200 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SSD}	–0.5	–	6	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	–0.5	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–200	–	200	mA	

Device Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 105 °C and TJ ≤ 125 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power Supply Input Voltage ($V_{DDA} = V_{DDD} = V_{DD}$)	1.8	–	5.5	V	With regulator enabled
SID255	V_{DDD}	Power Supply Input Voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	
SID55	CEFC	External Regulator voltage bypass	1	1.3	1.6	µF	X5R ceramic or better
SID56	CEXC	Power supply decoupling capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V. Typical Values measured at V_{DD} = 3.3 V							
SID9	IDD4	Execute from Flash; CPU at 6 MHz	–	–	2.8	mA	
SID10	IDD5	Execute from Flash; CPU at 6 MHz	–	2.2	–	mA	T = 25 °C
SID12	IDD7	Execute from Flash; CPU at 12 MHz,	–	–	4.2	mA	
SID13	IDD8	Execute from Flash; CPU at 12 MHz	–	3.7	–	mA	T = 25 °C
SID16	IDD11	Execute from Flash; CPU at 24 MHz	–	6.7	–	mA	T = 25 °C
SID17	IDD12	Execute from Flash; CPU at 24 MHz	–	–	7.2	mA	
SID19	IDD14	Execute from Flash; CPU at 48 MHz	–	12.8	–	mA	T = 25 °C
SID20	IDD15	Execute from Flash; CPU at 48 MHz	–	–	13.8	mA	
Sleep Mode, V_{DD} = 1.7 V to 5.5 V							
SID25	IDD20	I^2C wakeup, WDT, and Comparators on. 6 MHz.	–	1.3	1.8	mA	V_{DD} = 1.71 to 5.5 V.
SID25A	IDD20A	I^2C wakeup, WDT, and Comparators on. 12 MHz	–	1.7	2.2	mA	V_{DD} = 1.71 to 5.5 V.

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[2]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID241	V_{IH}[2]	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	
SID243	V_{IH}[2]	LVTTL input, $V_{DDD} \geq 2.7$ V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq 2.7$ V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 8 mA at 3-V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3-V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	
SID66	C_{IN}	Input capacitance	–	–	7	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V. Guaranteed by characterization
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DD}/Vss	–	–	100	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Table 8. Opamp Specifications
(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq$ 2.7 V	6	–	–	V/µs	
SID299	T_op_wake	From disable to enable, no external RC dominating	–	300	–	µs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	Guaranteed by design
	Comp_mode	Comparator mode; 50 mV drive, Trise = Tfall (approx.)	–	–	–		
SID300	T_{PD1}	Response time; power = high	–	150	–	ns	
SID301	T_{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T_{PD3}	Response time; power = low	–	2000	–	ns	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	

Comparatorr

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	$V_{OFFSET2}$	Input offset voltage, Common Mode voltage range from 0 to V_{DD}-1	–	–	±4	mV	
SID85A	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	–	±12	–	mV	
SID86	V_{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to V_{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2.
SID247	V_{ICM2}	Input common mode voltage in low power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	0	–	V_{DDD}	V	
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq$ 2.7 V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	V_{DDD} < 2.7 V. Guaranteed by characterization
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	Guaranteed by characterization
SID248	I_{CMP2}	Block current, low power mode	–	–	100	µA	Guaranteed by characterization
SID259	I_{CMP3}	Block current, ultra low power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C)	–	6	28	µA	Guaranteed by characterization

CSD

Table 14. CSD Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID.CSD#16	IDAC1IDD	IDAC1 (8 bits) block current	–	–	1125	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7 bits) block current	–	–	1125	µA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID308A	Vcompidac	Voltage compliance range of IDAC for S0	0.8	–	VDD-0.8	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise, 0.1-pF sensitivity	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1-pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8 bits) in High range	–	612	–	uA	
SID314A	IDAC1_CRT2	Output current of Idac1 (8 bits) in Low range	–	306	–	uA	
SID315	IDAC2_CRT1	Output current of Idac2 (7 bits) in High range	–	304.8	–	uA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7 bits) in Low range	–	152.4	–	uA	
SID320	IDACOFFSET	All zeroes input	–	–	±1	LSB	
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH	Mismatch between IDACs	–	–	7	LSB	
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Timer/Counter/PWM

Table 15. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I^2C

Table 16. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	

Table 17. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	

LCD Direct Drive

Table 18. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	
SID157	I_{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO. 25 °C	–	0.6	–	mA	32 × 4 segments. 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO. 25 °C	–	0.5	–	mA	32 × 4 segments. 50 Hz

Table 19. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	

Table 20. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	
SID161	I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

Table 21. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID162	F_{UART}	Bit rate	–	–	1	Mbps

SPI Specifications

Table 22. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID163	I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA
SID164	I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA
SID165	I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA

Table 23. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz

Table 24. Fixed SPI Master Mode AC Specifications
(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID167	T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns
SID168	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns
SID169	T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns

Table 25. Fixed SPI Slave Mode AC Specifications
(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × Tscbclk	ns
SID171A	T_{DSO_ext}	MISO valid after Sclock driving edge in Ext. Clock mode	–	–	48	ns
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns

Memory

Table 26. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 27. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[3]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[3]	Row erase time	–	–	13	ms	
SID176	$T_{ROWPROGRAM}$[3]	Row program time after erase	–	–	7	ms	
SID178	$T_{BULKERASE}$[3]	Bulk erase time (32 KB)	–	–	35	ms	
SID180	$T_{DEVPROG}$[3]	Total device program time	–	–	7	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET}	Flash retention. $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. $T_A \le 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F_{RETQ}	Flash retention. $T_A \le 105$ °C, 10 K P/E cycles, ≤ three years at $T_A \ge$ 85 °C	10	–	20	years	Guaranteed by characterization

Note
3. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Power-on-Reset (POR) with Brown Out

Table 28. Imprecise Power On Reset (IPOR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	$V_{IPORHYST}$	Hysteresis	15	–	200	mV	Guaranteed by characterization

Table 29. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.64	–	–	V	Full functionality between 1.71 V and BOD trip voltage is guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization
BID55	Svdd	Maximum power supply ramp rate	–	–	67	kV/sec	

Voltage Monitors

Table 30. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID195	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	–	–	100	µA	Guaranteed by characterization

Table 31. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	Guaranteed by characterization

SWD Interface

Table 32. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	$3.3\ V \le V_{DD} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	$1.71\ V \le V_{DD} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	
SID220	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	
SID221	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	
SID222	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	

Table 34. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if T_A > 85 °C and IMO frequency < 24 MHz
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12	µs	
SID227	$T_{JITRMSIMO1}$	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	$T_{JITRMSIMO2}$	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 36. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T_A > 85 °C

Table 37. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	Guaranteed by characterization

Table 38. UDB AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Datapath performance							
SID249	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	
SID250	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	
SID251	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	
PLD Performance in UDB							
SID252	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	
Clock to Output Performance							
SID253	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typ.	–	15	–	ns	
SID254	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case.	–	25	–	ns	

Table 39. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID256*	T_{WS48}*	Number of wait states at 48 MHz	1	–	–		CPU execution from Flash. Guaranteed by characterization
SID257	T_{WS24}*	Number of wait states at 24 MHz	0	–	–		CPU execution from Flash. Guaranteed by characterization
SID260	V_{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of Vbg (1.024 V). Guaranteed by characterization
SID262	$T_{CLKSWITCH}$	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	. Guaranteed by design
* Tws48 and Tws24 are guaranteed by Design							

Table 40. UDB Port Adaptor Specifications

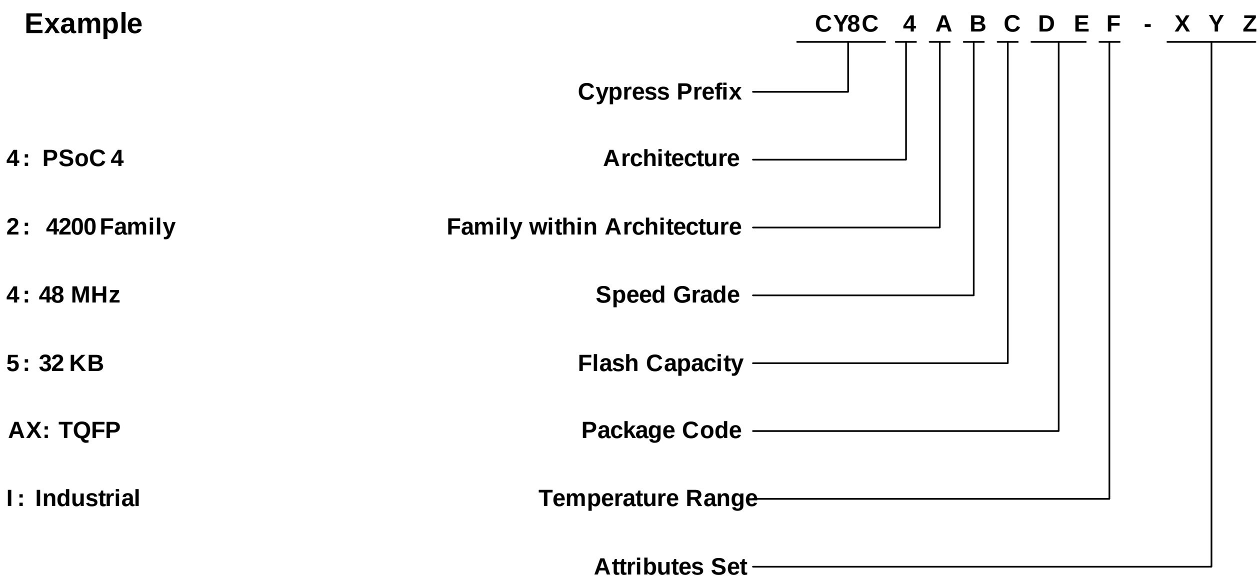
(Based on LPC Component Specs, Guaranteed by Characterization -10-pF load, 3-V V_{DDIO} and V_{DDD})

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID263	T_{LCLKDO}	LCLK to output delay	–	–	18	ns	
SID264	$T_{DINLCLK}$	Input setup time to LCLCK rising edge	–	–	7	ns	
SID265	$T_{DINLCLKHLD}$	Input hold time from LCLK rising edge	5	–	–	ns	
SID266	$T_{LCLKHIZ}$	LCLK to output tristated	–	–	28	ns	
SID267	T_{FLCLK}	LCLK frequency	–	–	33	MHz	
SID268	$T_{LCLKDUTY}$	LCLK duty cycle (percentage high)	40	–	60	%	

Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.



The Field Values are listed in the following table.

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	1	4100 Family
		2	4200 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
DE	Package Code	AX, AZ	TQFP
		LQ	QFN
		PV	SSOP
		FN	WLCSP
F	Temperature Range	I	Industrial
		Q	Extended Industrial
XYZ	Attributes Code	000-999	Code of feature set in specific family

Acronyms

Table 45. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD