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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4245lqq-483

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in PSoC 4200 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4200 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4200 Flash supports the following flash protection modes at the memory subsystem level:

- **Open: No Protection.** Factory default mode in which the product is shipped.
- **Protected: User may change from Open to Protected.** This mode disables Debug interface accesses. The mode can be set back to Open but only after completely erasing the Flash.
- **Kill: User may change from Open to Kill.** This mode disables all Debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrevocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

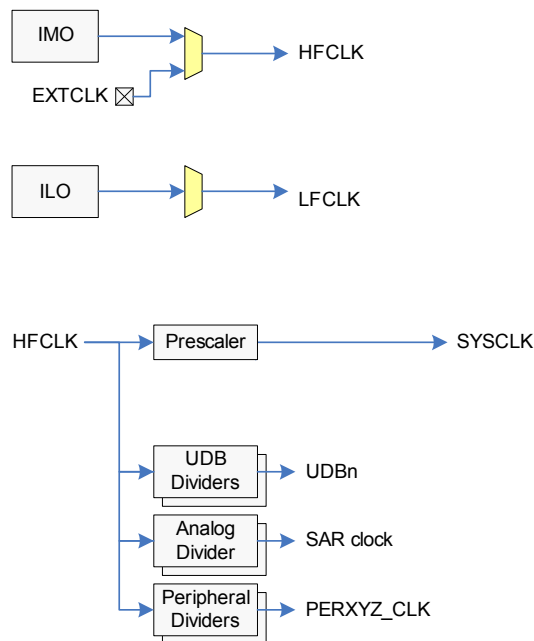
The power system is described in detail in the section [Power on page 16](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4200 operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4200 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4200 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO) and a provision for an external clock.

Figure 3. PSoC 4200 MCU Clocking Architecture



The HFCLK signal can be divided down (see [PSoC 4200 MCU Clocking Architecture](#)) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4200, each with 16-bit divide capability; this allows eight to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator. When UDB-generated pulse interrupts are used, SYSCLK must equal HFCLK.

Fixed Function Digital

Timer/Counter/PWM Block (TCPWM)

The TCPWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a pre-terminated state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

Serial Communication Blocks (SCB)

PSoC 4200 has two SCBs, which can each implement an I²C, UART, or SPI interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I²C peripheral is compatible with the I²C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes. The I²C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. The required Rise and Fall times for different I²C speeds are guaranteed by using appropriate pull-up resistor values depending on VDD, Bus Capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, refer to the UM10204 I²C bus specification and user manual (the latest revision is available at www.nxp.com).

PSoC 4200 is not completely compliant with the I²C spec in the following respects:

- GPIO cells are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.
- Fast-Mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast mode and Fast-Mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I²C master, it interposes an IDLE state between NACK and Repeated Start; the I²C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.

- When the SCB is in I²C slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its I²C address must be even.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

GPIO

PSoC 4200 has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4200 since it has 4.5 ports).

Special Function Peripherals

LCD Segment Drive

PSoC 4200 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in PSoC 4200 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used. (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

WLCSP Package Bootloader

The WLCSP package is supplied with an I²C Bootloader installed in flash. The bootloader is compatible with PSoC Creator bootloadable project files and has the following default settings:

- I²C SCL and SDA connected to port pins P4.0 and P4.1 respectively (external pull-up resistors required)
- I²C Slave mode, address 8, data rate = 100 kbps
- Single application
- Wait two seconds for bootstrap command
- Other bootloader options are as set by the PSoC Creator Bootloader Component default
- Occupies the bottom 4.5 KB of flash

For more information on this bootloader, see the following Cypress application note:

[AN73854](#) - Introduction to Bootloaders

Note that a PSoC Creator bootloadable project must be associated with *.hex* and *.elf* files for a bootloader project that is configured for the target device. Bootloader *.hex* and *.elf* files can be found at <http://www.cypress.com/?rID=78632>. The factory-installed bootloader can be overwritten using JTAG or SWD programming.

Pinouts

The following is the pin-list for the PSoC 4200 (44-TQFP, 40-QFN, 28-SSOP, and 48-TQFP). Port 2 comprises of the high-speed Analog inputs for the SAR Mux. P1.7 is the optional external input and bypass for the SAR reference. Ports 3 and 4 contain the Digital Communication channels. All pins support CSD CapSense and Analog Mux Bus connections.

44-TQFP		40-QFN		28-SSOP		48-TQFP		Alternate Functions for Pins					Pin Description
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
1	VSS	–	–	–	–	–	–	–	–	–	–	–	Ground
2	P2.0	1	P2.0	–	–	2	P2.0	sarmux.0	–	–	–	–	Port 2 Pin 0: gpio, lcd, csd, sarmux
3	P2.1	2	P2.1	–	–	3	P2.1	sarmux.1	–	–	–	–	Port 2 Pin 1: gpio, lcd, csd, sarmux
4	P2.2	3	P2.2	5	P2.2	4	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
5	P2.3	4	P2.3	6	P2.3	5	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
6	P2.4	5	P2.4	7	P2.4	6	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
7	P2.5	6	P2.5	8	P2.5	7	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
8	P2.6	7	P2.6	9	P2.6	8	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
9	P2.7	8	P2.7	10	P2.7	9	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
10	VSS	9	VSS	–	–	–	–	–	–	–	–	–	Ground
–	–	–	–	–	–	10	NC	–	–	–	–	–	No Connect
–	–	–	–	–	–	11	NC	–	–	–	–	–	No Connect
11	P3.0	10	P3.0	11	P3.0	12	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
12	P3.1	11	P3.1	12	P3.1	13	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
13	P3.2	12	P3.2	13	P3.2	14	P3.2	–	tcpwm1_p[0]	–	swd_io[0]	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
–	–	–	–	–	–	15	VSSD	–	–	–	–	–	Ground
14	P3.3	13	P3.3	14	P3.3	16	P3.3	–	tcpwm1_n[0]	–	swd_clk[0]	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
15	P3.4	14	P3.4	–	–	17	P3.4	–	tcpwm2_p[0]	–	–	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
16	P3.5	15	P3.5	–	–	18	P3.5	–	tcpwm2_n[0]	–	–	scb1_spi_ssel_2	Port 3 Pin 5: gpio, lcd, csd, pwm, scb1
17	P3.6	16	P3.6	–	–	19	P3.6	–	tcpwm3_p[0]	–	swd_io[1]	scb1_spi_ssel_3	Port 3 Pin 6: gpio, lcd, csd, pwm, scb1, swd
18	P3.7	17	P3.7	–	–	20	P3.7	–	tcpwm3_n[0]	–	swd_clk[1]	–	Port 3 Pin 7: gpio, lcd, csd, pwm, swd
19	VDDD	–	–	–	–	21	VDDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5V
20	P4.0	18	P4.0	15	P4.0	22	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
21	P4.1	19	P4.1	16	P4.1	23	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
22	P4.2	20	P4.2	17	P4.2	24	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
23	P4.3	21	P4.3	18	P4.3	25	P4.3	csd_c_sh_tank	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
–	–	–	–	–	–	26	NC	–	–	–	–	–	No Connect
–	–	–	–	–	–	27	NC	–	–	–	–	–	No Connect

44-TQFP		40-QFN		28-SSOP		48-TQFP		Alternate Functions for Pins					Pin Description
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
24	P0.0	22	P0.0	19	P0.0	28	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
25	P0.1	23	P0.1	20	P0.1	29	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
26	P0.2	24	P0.2	21	P0.2	30	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
27	P0.3	25	P0.3	22	P0.3	31	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
28	P0.4	26	P0.4	–	–	32	P0.4	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
29	P0.5	27	P0.5	–	–	33	P0.5	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
30	P0.6	28	P0.6	23	P0.6	34	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
31	P0.7	29	P0.7	24	P0.7	35	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
32	XRES	30	XRES	25	XRES	36	XRES	–	–	–	–	–	Chip reset, active low
33	VCCD	31	VCCD	26	VCCD	37	VCCD	–	–	–	–	–	Regulated supply, connect to 1µF cap or 1.8V
–	–	–	–	–	–	38	VSSD	–	–	–	–	–	Digital Ground
34	VDDD	32	VDDD	27	VDD	39	VDDD	–	–	–	–	–	Digital Supply, 1.8 - 5.5V
35	VDDA	33	VDDA	27	VDD	40	VDDA	–	–	–	–	–	Analog Supply, 1.8 - 5.5V, equal to VDDD
36	VSSA	34	VSSA	28	VSS	41	VSSA	–	–	–	–	–	Analog Ground
37	P1.0	35	P1.0	1	P1.0	42	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
38	P1.1	36	P1.1	2	P1.1	43	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
39	P1.2	37	P1.2	3	P1.2	44	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
40	P1.3	38	P1.3	–	–	45	P1.3	ctb.oa1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
41	P1.4	39	P1.4	–	–	46	P1.4	ctb.oa1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
42	P1.5	–	–	–	–	47	P1.5	ctb.oa1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
43	P1.6	–	–	–	–	48	P1.6	ctb.oa0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
44	P1.7/VREF	40	P1.7/VREF	4	P1.7/VREF	1	P1.7/VREF	ctb.oa1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Notes:

1. tcpwm_p and tcpwm_n refer to tcpwm non-inverted and inverted outputs respectively.
2. P3.2 and P3.3 are SWD pins after boot (reset).

35-Ball CSP		Alternate Functions for Pins					Pin Description
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
D7	P1.3	ctb.0a1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
D4	P1.4	ctb.0a1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
D5	P1.5	ctb.0a1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
D6	P1.6	ctb.0a0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
E7	P1.7/VR EF	ctb.0a1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Descriptions of the Pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V $\pm 5\%$).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following packages are supported: 48-pin TQFP, 44-pin TQFP, 40-pin QFN, and 28-pin SSOP.

Figure 7. 48-Pin TQFP Pinout

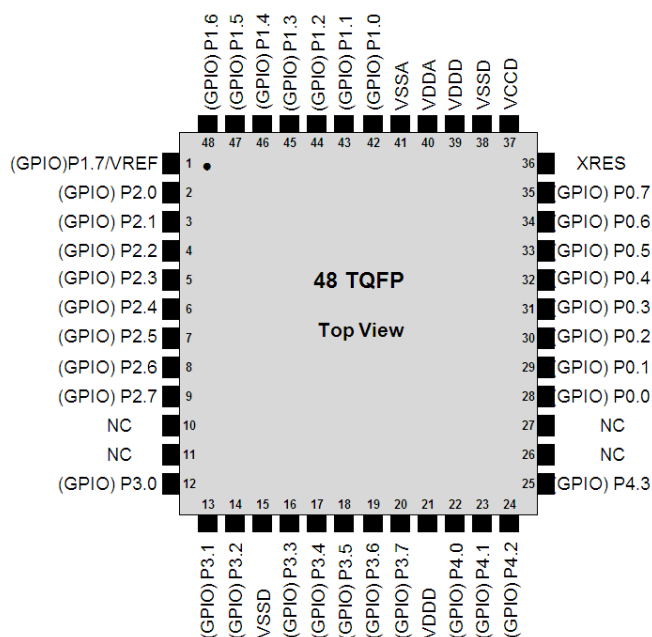


Figure 8. 44-pin TQFP Part Pinout

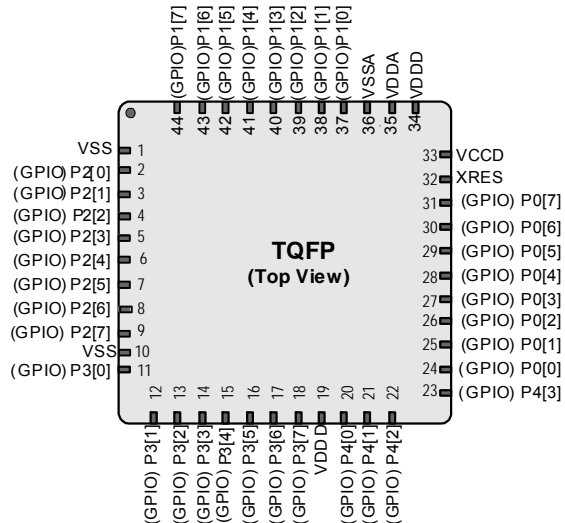


Figure 9. 40-Pin QFN Pinout

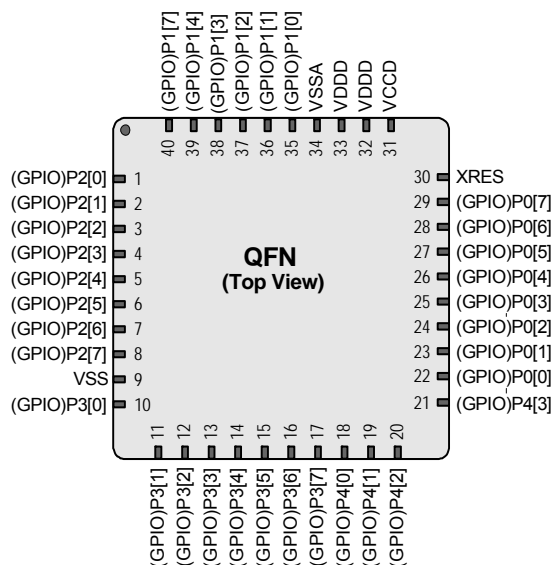


Figure 10. 35-Ball WLCSP

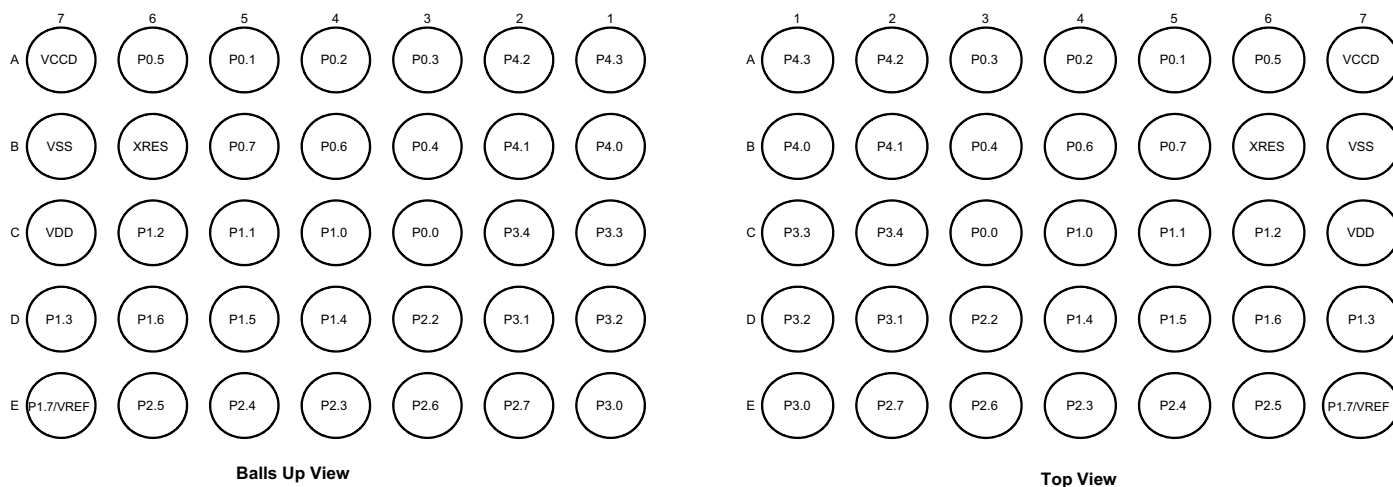
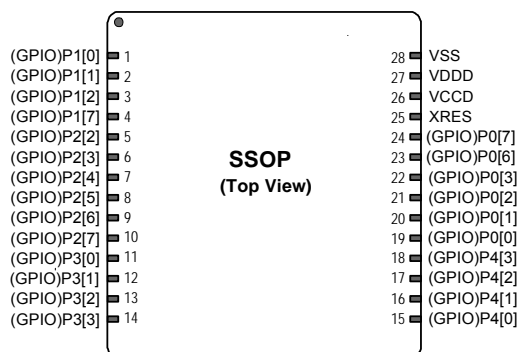


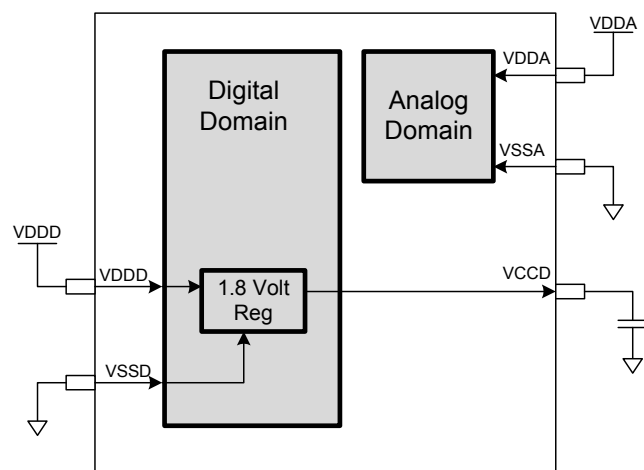
Figure 11. 28-Pin SSOP Pinout



Power

The following power system diagrams show the minimum set of power supply pins as implemented for the PSoC 4200. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DDA} input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

Figure 12. PSoC 4 Power Supply



The PSoC 4200 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, PSoC 4200 is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4200 supplies the internal logic and the V_{CCD} output of PSoC 4200 must be bypassed to ground via an external capacitor (in the range of 1 μF to 1.6 μF ; X5R ceramic or better).

V_{DDA} and V_{DDD} must be shorted together; the grounds, V_{SSA} and V_{SS} must also be shorted together. Bypass capacitors must be used from V_{DDD} to ground, typical practice for systems in this frequency range is to use a capacitor in the 1- μF range in parallel with a smaller capacitor (0.1 μF for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 13. 48-TQFP Package Example

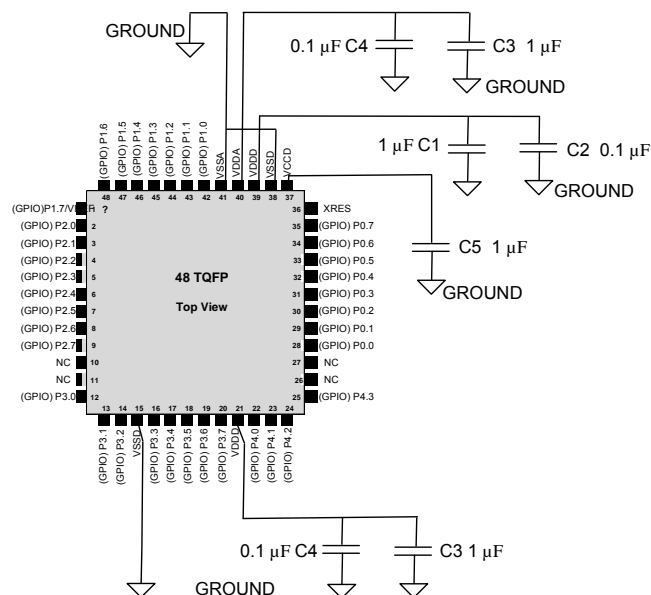
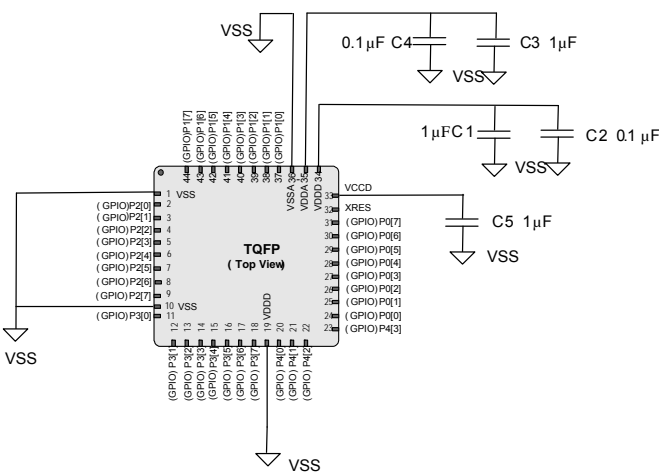


Figure 14. 44-TQFP Package Example



Power Supply	Bypass Capacitors
$V_{DDD}-V_{SS}$	0.1- μF ceramic at each pin (C2, C6) plus bulk capacitor 1 μF to 10 μF (C1). Total capacitance may be greater than 10 μF .
$V_{DDA}-V_{SSA}$	0.1- μF ceramic at pin (C4). Additional 1 μF to 10 μF (C3) bulk capacitor. Total capacitance may be greater than 10 μF .
$V_{CCD}-V_{SS}$	1- μF ceramic capacitor at the VCCD pin (C5)
$V_{REF}-V_{SSA}$ (optional)	The internal bandgap may be bypassed with a 1- μF to 10- μF capacitor. Total capacitance may be greater than 10 μF .

Table 2. DC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Deep Sleep Mode, $V_{DD} = 1.8\text{ V to }3.6\text{ V}$ (Regulator on)							
SID31	IDD26	I ² C wakeup and WDT on.	–	1.3	–	μA	T = 25 °C
SID32	IDD27	I ² C wakeup and WDT on.	–	–	45	μA	T = 85 °C
Deep Sleep Mode, $V_{DD} = 3.6\text{ V to }5.5\text{ V}$							
SID34	IDD29	I ² C wakeup and WDT on	–	1.5	15	μA	Typ. at 25 °C. Max at 85 °C.
Deep Sleep Mode, $V_{DD} = 1.71\text{ V to }1.89\text{ V}$ (Regulator bypassed)							
SID37	IDD32	I ² C wakeup and WDT on.	–	1.7	–	μA	T = 25 °C
SID38	IDD33	I ² C wakeup and WDT on	–	–	60	μA	T = 85 °C
Deep Sleep Mode, +105 °C							
SID33Q	IDD28Q	I ² C wakeup and WDT on. Regulator Off.	–	–	135	μA	$V_{DD} = 1.71\text{ to }1.89$
SID34Q	IDD29Q	I ² C wakeup and WDT on.	–	–	180	μA	$V_{DD} = 1.8\text{ to }3.6$
SID35Q	IDD30Q	I ² C wakeup and WDT on.	–	–	140	μA	$V_{DD} = 3.6\text{ to }5.5$
Hibernate Mode, $V_{DD} = 1.8\text{ V to }3.6\text{ V}$ (Regulator on)							
SID40	IDD35	GPIO and Reset active	–	150	–	nA	T = 25 °C
SID41	IDD36	GPIO and Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, $V_{DD} = 3.6\text{ V to }5.5\text{ V}$							
SID43	IDD38	GPIO and Reset active	–	150	–	nA	T = 25 °C
Hibernate Mode, $V_{DD} = 1.71\text{ V to }1.89\text{ V}$ (Regulator bypassed)							
SID46	IDD41	GPIO and Reset active	–	150	–	nA	T = 25 °C
SID47	IDD42	GPIO and Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, +105 °C							
SID42Q	IDD37Q	Regulator Off	–	–	19.4	μA	$V_{DD} = 1.71\text{ to }1.89$
SID43Q	IDD38Q		–	–	17	μA	$V_{DD} = 1.8\text{ to }3.6$
SID44Q	IDD39Q		–	–	16	μA	$V_{DD} = 3.6\text{ to }5.5$
Stop Mode							
SID304	IDD43A	Stop Mode current; $V_{DD} = 3.3\text{ V}$	–	20	80	nA	Typ. at 25 °C. Max at 85 °C.
Stop Mode, +105 °C							
SID304Q	IDD43AQ	Stop Mode current; $V_{DD} = 3.6\text{ V}$	–	–	5645	nA	
XRES current							
SID307	IDD_XR	Supply current while XRES asserted	–	2	5	mA	

Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F _{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49	T _{SLEEP}	Wakeup from sleep mode	–	0	–	μs	Guaranteed by characterization
SID50	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	–	25	μs	24 MHz IMO. Guaranteed by characterization
SID51	T _{HIBERNATE}	Wakeup from Hibernate and Stop modes	–	–	2	ms	Guaranteed by characterization
SID52	T _{RESETWIDTH}	External reset pulse width	1	–	–	μs	Guaranteed by characterization

Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	μA	
SID270	I_{DD_MED}	Power = medium	–	550	950	μA	
SID271	I_{DD_LOW}	Power = low	–	150	350	μA	
	GBW	Load = 20 pF, 0.1 mA. $V_{DDA} = 2.7$ V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT_MAX_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT_MAX_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT_MAX_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	$V_{DDA} = 1.71$ V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT_MAX_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT_MAX_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT_MAX_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	$V_{DDA} - 0.2$	V	
SID282	V_{CM}	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	$V_{DDA} - 0.2$	V	
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–	–	
SID283	V_{OUT_1}	Power = high, Iload=10 mA	0.5	–	$V_{DDA} - 0.5$	V	
SID284	V_{OUT_2}	Power = high, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID285	V_{OUT_3}	Power = medium, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID286	V_{OUT_4}	Power = low, Iload=0.1mA	0.2	–	$V_{DDA} - 0.2$	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–10	±3	10	μV/°C	High mode. $T_A \leq 85$ °C
SID290Q	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	15	±3	15	μV/°C	High mode. $T_A \leq 105$ °C
SID290A	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	±10	–	μV/°C	Medium mode
SID290B	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	±10	–	μV/°C	Low mode
SID291	CMRR	DC	70	80	–	dB	$V_{DDD} = 3.6$ V
SID292	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	$V_{DDD} = 3.6$ V
	Noise		–	–	–	–	
SID293	V_{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	μVrms	
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	V_{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	

Table 12. SAR ADC DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID111	A_INL	Integral non linearity	−1.7	−	+2	LSB	$V_{DD} = 1.71$ to 5.5 , 1 Msps, $V_{ref} = 1$ to 5.5 .
SID111A	A_INL	Integral non linearity	−1.5	−	+1.7	LSB	$V_{DDD} = 1.71$ to 3.6 , 1 Msps, $V_{ref} = 1.71$ to V_{DDD} .
SID111B	A_INL	Integral non linearity	−1.5	−	+1.7	LSB	$V_{DDD} = 1.71$ to 5.5 , 500 Ksps, $V_{ref} = 1$ to 5.5 .
SID112	A_DNL	Differential non linearity	−1	−	+2.2	LSB	$V_{DDD} = 1.71$ to 5.5 , 1 Msps, $V_{ref} = 1$ to 5.5 .
SID112A	A_DNL	Differential non linearity	−1	−	+2	LSB	$V_{DDD} = 1.71$ to 3.6 , 1 Msps, $V_{ref} = 1.71$ to V_{DDD} .
SID112B	A_DNL	Differential non linearity	−1	−	+2.2	LSB	$V_{DDD} = 1.71$ to 5.5 , 500 Ksps, $V_{ref} = 1$ to 5.5 .

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108	A_SAMP_1	Sample rate with external reference bypass cap	−	−	1	Msps	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	−	−	500	Ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	−	−	100	Ksps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	−	−	dB	$F_{IN} = 10$ kHz
SID113	A_THD	Total harmonic distortion	−	−	−65	dB	$F_{IN} = 10$ kHz.

CSD
Table 14. CSD Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID.CSD#16	IDAC1IDD	IDAC1 (8 bits) block current	–	–	1125	μA	
SID.CSD#17	IDAC2IDD	IDAC2 (7 bits) block current	–	–	1125	μA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID308A	Vcompidac	Voltage compliance range of IDAC for S0	0.8	–	VDD-0.8	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise, 0.1-pF sensitivity	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1-pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8 bits) in High range	–	612	–	uA	
SID314A	IDAC1_CRT2	Output current of Idac1 (8 bits) in Low range	–	306	–	uA	
SID315	IDAC2_CRT1	Output current of Idac2 (7 bits) in High range	–	304.8	–	uA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7 bits) in Low range	–	152.4	–	uA	
SID320	IDACOFFSET	All zeroes input	–	–	±1	LSB	
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH	Mismatch between IDACs	–	–	7	LSB	
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	μs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	μs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Timer/Counter/PWM

Table 15. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I²C

Table 16. Fixed I²C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135	μA	
SID151	I _{I2C3}	Block current consumption at 1 Mbps	–	–	310	μA	
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	–	–	1.4	μA	

Table 17. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1	Mbps	

SWD Interface

Table 32. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID214	F_SWCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	$T = 1/f_{\text{SWDCLK}}$	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	$T = 1/f_{\text{SWDCLK}}$	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	$T = 1/f_{\text{SWDCLK}}$	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	$T = 1/f_{\text{SWDCLK}}$	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_IMO1	IMO operating current at 48 MHz	–	–	1000	μA	
SID219	I_IMO2	IMO operating current at 24 MHz	–	–	325	μA	
SID220	I_IMO3	IMO operating current at 12 MHz	–	–	225	μA	
SID221	I_IMO4	IMO operating current at 6 MHz	–	–	180	μA	
SID222	I_IMO5	IMO operating current at 3 MHz	–	–	150	μA	

Table 34. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F_IMOTOL1	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if $T_A > 85^\circ\text{C}$ and IMO frequency < 24 MHz
SID226	T_STARTIMO	IMO startup time	–	–	12	μs	
SID227	T_JITRMSIMO1	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	T_JITRMSIMO2	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	T_JITRMSIMO3	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_ILO1	ILO operating current at 32 kHz	–	0.3	1.05	μA	Guaranteed by Characterization
SID233	I_ILOLEAK	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 36. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T _{STARTILO1}	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	T _{ILODUTY}	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	F _{ILOTRIM1}	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T _A > 85 °C

Table 37. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V _{DD/2}	45	–	55	%	Guaranteed by characterization

Table 38. UDB AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Datapath performance							
SID249	F _{MAX-TIMER}	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	
SID250	F _{MAX-ADDER}	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	
SID251	F _{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	
PLD Performance in UDB							
SID252	F _{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	
Clock to Output Performance							
SID253	T _{CLK_OUT_UDB1}	Prop. delay for clock in to data out at 25 °C, Typ.	–	15	–	ns	
SID254	T _{CLK_OUT_UDB2}	Prop. delay for clock in to data out, Worst case.	–	25	–	ns	

Acronyms

Table 45. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 45. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 45. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 45. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 46. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC® 4: PSoC 4200 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-87197				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*B	4108562	WKA	08/29/2013	Added clarifying note about the XRES pin in the Reset section. Updated UDB Array diagram. Added a link reference to the PSoC 4 TRM. Updated the footnote in Absolute Maximum Ratings . Updated Sleep Mode IDD specs in DC Specifications . Updated Comparator DC Specifications Updated SAR ADC AC Specifications Updated LCD Direct Drive DC Specifications Updated the number of GPIOs in Ordering Information .
*C	4568937	MKEA/ WKA	11/19/2014	Added More Information and PSoC Creator sections. Added 48-pin TQFP pin and package details. Added SID308A spec details. Updated Ordering Information .
*D	4617283	WKA	01/08/2015	Corrected typo in the ordering information table. Updated 28-pin SSOP package diagram.
*E	4643655	WKA	04/29/2015	Added 35 WLCSP pinout and package detail information. Updated CSD specifications.
*F	5287114	WKA	06/09/2016	Added reference to AN90071 in the More Information section. Updated Flash section with details of flash protection modes. Added notes in the Pinouts section. Updated 40-pin QFN and 28-pin SSOP pin diagrams. Added PSoC 4 Power Supply diagram. Updated the Bypass Capacitors column in the Power Supply table. Updated values for SID32, SID34, SID38, SID269, SID270, SID271. Added SID299A. Updated Comparator Specifications. Updated TCPWM Specifications. Updated values for SID149, SID160, SID171. Updated Conditions for SID190. Added BID55. Removed Conditions for SID237. Added reference to PSoC 4 CAB Libraries with Schematics Symbols and PCB Footprints in the Packaging section.
*G	5327384	WKA	06/28/2016	Removed capacitor connection for Pin 15 in Figure 13.
*H	5702140	GNKK	04/19/2017	Updated the Cypress logo and copyright information.