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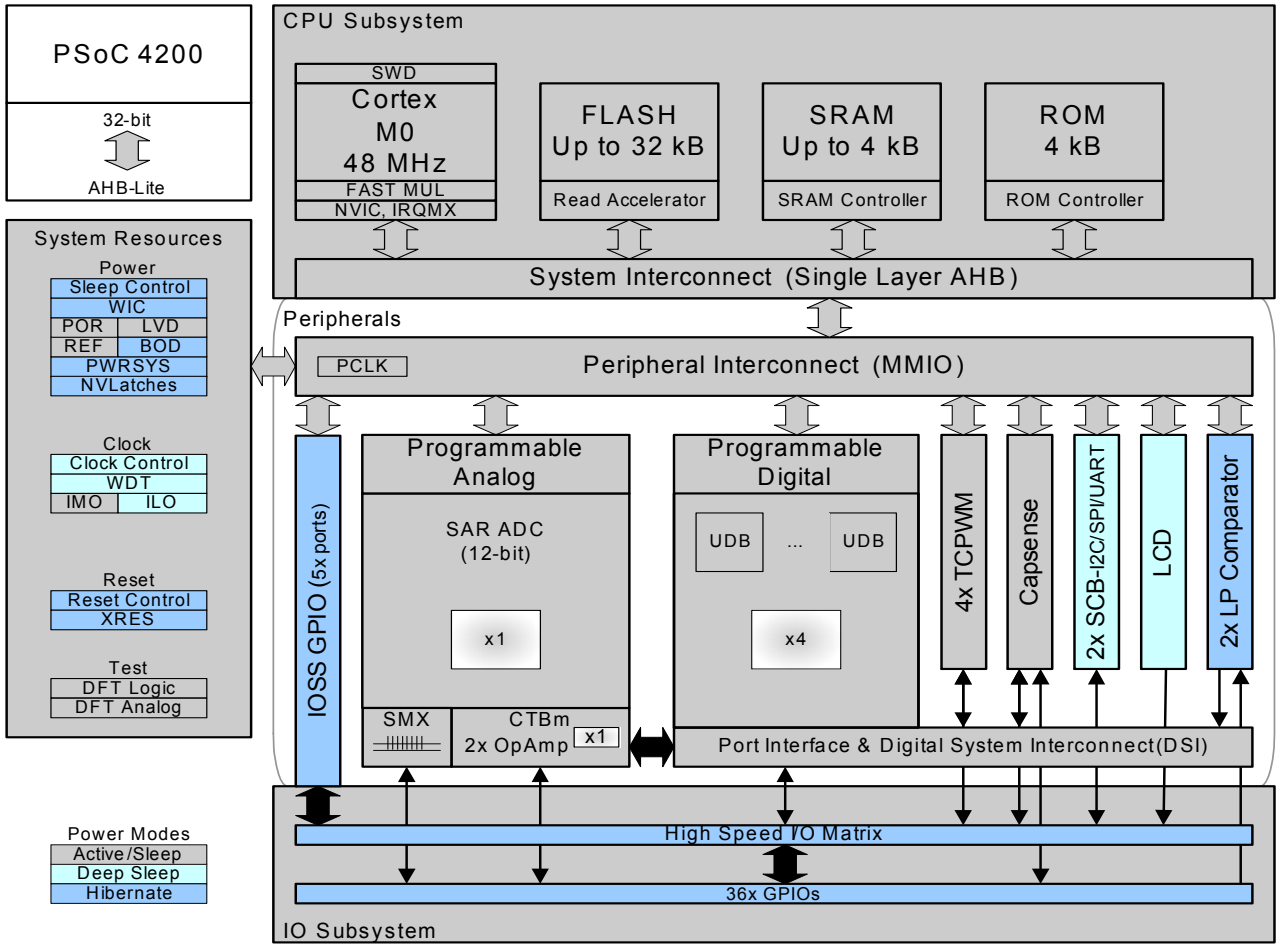
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 8x12b SAR; D/A 2xIDAC |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4245pvi-482 |

**Figure 2. Block Diagram**




The PSoC 4200 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4200 devices. The SWD interface is fully compatible with industry-standard third-party tools. With the ability to disable debug features, with very robust flash protection, and allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 4200 family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4200 with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4200 allows the customer to make.

## Fixed Function Digital

*Timer/Counter/PWM Block (TCPWM)*

The TCPWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

*Serial Communication Blocks (SCB)*

PSoC 4200 has two SCBs, which can each implement an $I^2C$, UART, or SPI interface.

**$I^2C$ Mode**: The hardware $I^2C$ block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The $I^2C$ peripheral is compatible with the $I^2C$ Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP $I^2C$-bus specification and user manual (UM10204). The $I^2C$ bus I/O is implemented with GPIO in open-drain modes. The $I^2C$ bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. The required Rise and Fall times for different $I^2C$ speeds are guaranteed by using appropriate pull-up resistor values depending on VDD, Bus Capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, refer to the UM10204 I2C bus specification and user manual (the latest revision is available at www.nxp.com).

PSoC 4200 is not completely compliant with the $I^2C$ spec in the following respects:

- GPIO cells are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the $I^2C$ system.
- Fast-Mode Plus has an $I_{OL}$ specification of 20 mA at a $V_{OL}$ of 0.4 V. The GPIO cells can sink a maximum of 8-mA $I_{OL}$ with a $V_{OL}$ maximum of 0.6 V.
- Fast mode and Fast-Mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an $I^2C$ master, it interposes an IDLE state between NACK and Repeated Start; the $I^2C$ spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in $I^2C$ slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its $I^2C$ address must be even.

**UART Mode**: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

**SPI Mode**: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

## GPIO

PSoC 4200 has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4200 since it has 4.5 ports).

The following is the pin-list for the PSoC 4200 (35-WLCSP).

| 35-Ball CSP | | Alternate Functions for Pins | | | | | Pin Description |
|---|---|---|---|---|---|---|---|
| Pin | Name | Analog | Alt 1 | Alt 2 | Alt 3 | Alt 4 | |
| D3 | P2.2 | sarmux.2 | – | – | – | – | Port 2 Pin 2: gpio, lcd, csd, sarmux |
| E4 | P2.3 | sarmux.3 | – | – | – | – | Port 2 Pin 3: gpio, lcd, csd, sarmux |
| E5 | P2.4 | sarmux.4 | tcpwm0_p[1] | – | – | – | Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm |
| E6 | P2.5 | sarmux.5 | tcpwm0_n[1] | – | – | – | Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm |
| E3 | P2.6 | sarmux.6 | tcpwm1_p[1] | – | – | – | Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm |
| E2 | P2.7 | sarmux.7 | tcpwm1_n[1] | – | – | – | Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm |
| E1 | P3.0 | – | tcpwm0_p[0] | scb1_uart_rx[0] | scb1_i2c_scl[0] | scb1_spi_mosi[0] | Port 3 Pin 0: gpio, lcd, csd, pwm, scb1 |
| D2 | P3.1 | – | tcpwm0_n[0] | scb1_uart_tx[0] | scb1_i2c_sda[0] | scb1_spi_miso[0] | Port 3 Pin 1: gpio, lcd, csd, pwm, scb1 |
| D1 | P3.2 | – | tcpwm1_p[0] | – | swd_io[0] | scb1_spi_clk[0] | Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd |
| B7 | VSS | – | – | – | – | – | Ground |
| C1 | P3.3 | – | tcpwm1_n[0] | – | swd_clk[0] | scb1_spi_ssel_0[0] | Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd |
| C2 | P3.4 | – | tcpwm2_p[0] | - | – | scb1_spi_ssel_1 | Port 3 Pin 4: gpio, lcd, csd, pwm, scb1 |
| B1 | P4.0 | – | – | scb0_uart_rx | scb0_i2c_scl | scb0_spi_mosi | Port 4 Pin 0: gpio, lcd, csd, scb0 |
| B2 | P4.1 | – | – | scb0_uart_tx | scb0_i2c_sda | scb0_spi_miso | Port 4 Pin 1: gpio, lcd, csd, scb0 |
| A2 | P4.2 | csd_c_mod | – | – | – | scb0_spi_clk | Port 4 Pin 2: gpio, lcd, csd, scb0 |
| A1 | P4.3 | csd_c_sh_tank | – | – | – | scb0_spi_ssel_0 | Port 4 Pin 3: gpio, lcd, csd, scb0 |
| C3 | P0.0 | comp1_inp | – | – | – | scb0_spi_ssel_1 | Port 0 Pin 0: gpio, lcd, csd, scb0, comp |
| A5 | P0.1 | comp1_inn | – | – | – | scb0_spi_ssel_2 | Port 0 Pin 1: gpio, lcd, csd, scb0, comp |
| A4 | P0.2 | comp2_inp | – | – | – | scb0_spi_ssel_3 | Port 0 Pin 2: gpio, lcd, csd, scb0, comp |
| A3 | P0.3 | comp2_inn | – | – | – | – | Port 0 Pin 3: gpio, lcd, csd, comp |
| B3 | P0.4 | – | – | scb1_uart_rx[1] | scb1_i2c_scl[1] | scb1_spi_mosi[1] | Port 0 Pin 4: gpio, lcd, csd, scb1 |
| A6 | P0.5 | – | – | scb1_uart_tx[1] | scb1_i2c_sda[1] | scb1_spi_miso[1] | Port 0 Pin 5: gpio, lcd, csd, scb1 |
| B4 | P0.6 | – | ext_clk | – | – | scb1_spi_clk[1] | Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk |
| B5 | P0.7 | – | – | – | wakeup | scb1_spi_ssel_0[1] | Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup |
| B6 | XRES | – | – | – | – | – | Chip reset, active low |
| A7 | VCCD | – | – | – | – | – | Regulated supply, connect to 1µF cap or 1.8V |
| C7 | VDD | – | – | – | – | – | Supply, 1.8 - 5.5V |
| C4 | P1.0 | ctb.oa0.inp | tcpwm2_p[1] | – | – | – | Port 1 Pin 0: gpio, lcd, csd, ctb, pwm |
| C5 | P1.1 | ctb.oa0.inm | tcpwm2_n[1] | – | – | – | Port 1 Pin 1: gpio, lcd, csd, ctb, pwm |
| C6 | P1.2 | ctb.oa0.out | tcpwm3_p[1] | – | – | – | Port 1 Pin 2: gpio, lcd, csd, ctb, pwm |

| 35-Ball CSP | | Alternate Functions for Pins | | | | | Pin Description |
|---|---|---|---|---|---|---|---|
| Pin | Name | Analog | Alt 1 | Alt 2 | Alt 3 | Alt 4 | |
| D7 | P1.3 | ctb.oa1.out | tcpwm3_n[1] | – | – | – | Port 1 Pin 3: gpio, lcd, csd, ctb, pwm |
| D4 | P1.4 | ctb.oa1.inm | – | – | – | – | Port 1 Pin 4: gpio, lcd, csd, ctb |
| D5 | P1.5 | ctb.oa1.inp | – | – | – | – | Port 1 Pin 5: gpio, lcd, csd, ctb |
| D6 | P1.6 | ctb.oa0.inp_alt | – | – | – | – | Port 1 Pin 6: gpio, lcd, csd |
| E7 | P1.7/VREF | ctb.oa1.inp_alt ext_vref | – | – | – | – | Port 1 Pin 7: gpio, lcd, csd, ext_ref |

**Descriptions of the Pin functions are as follows:**

**VDDD**: Power supply for both analog and digital sections (where there is no $V_{DDA}$ pin).

**VDDA**: Analog $V_{DD}$ pin where package pins allow; shorted to $V_{DDD}$ otherwise.

**VSSA:** Analog ground pin where package pins allow; shorted to VSS otherwise

**VSS**: Ground pin.

**VCCD**: Regulated Digital supply (1.8 V ±5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following packages are supported: 48-pin TQFP, 44-pin TQFP, 40-pin QFN, and 28-pin SSOP.

**Figure 7. 48-Pin TQFP Pinout**

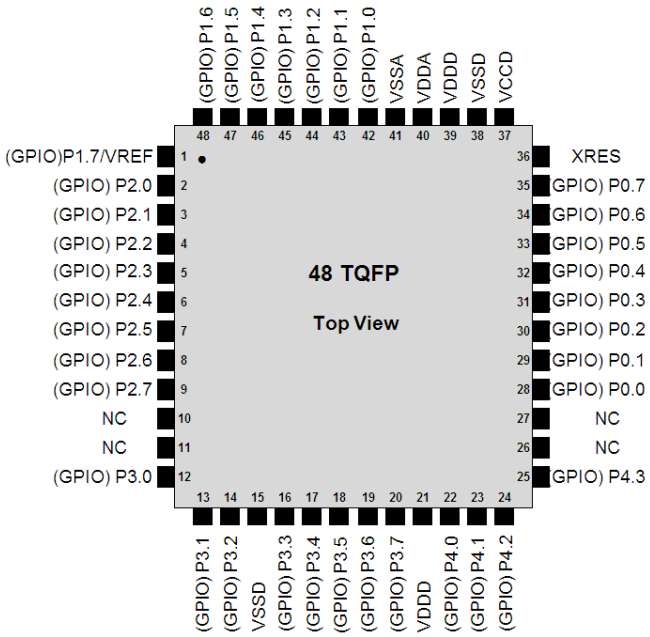



**Figure 8. 44-pin TQFP Part Pinout**

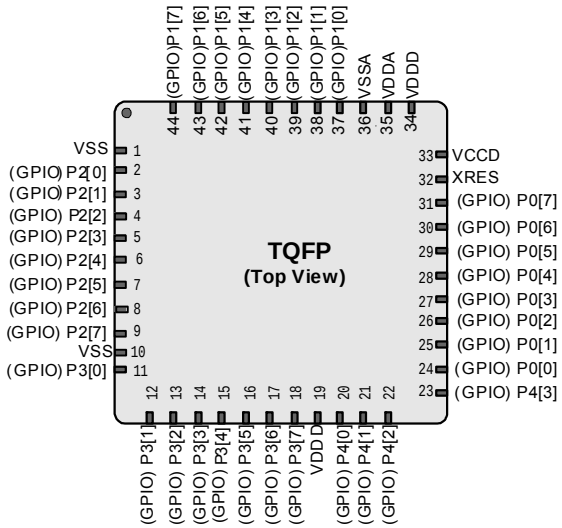


**Figure 9. 40-Pin QFN Pinout**

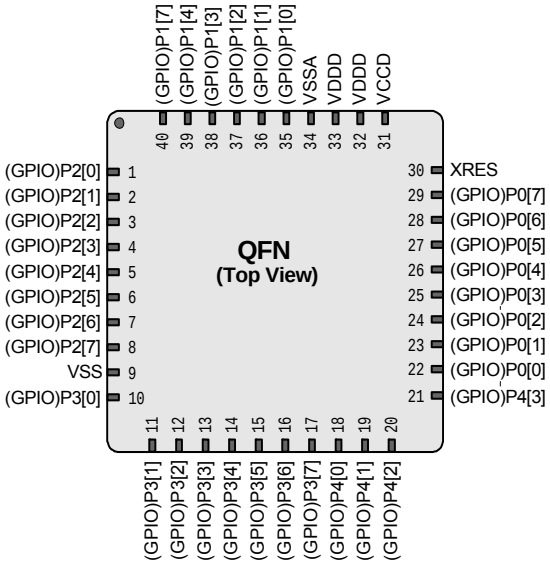



**Figure 10. 35-Ball WLCSP**

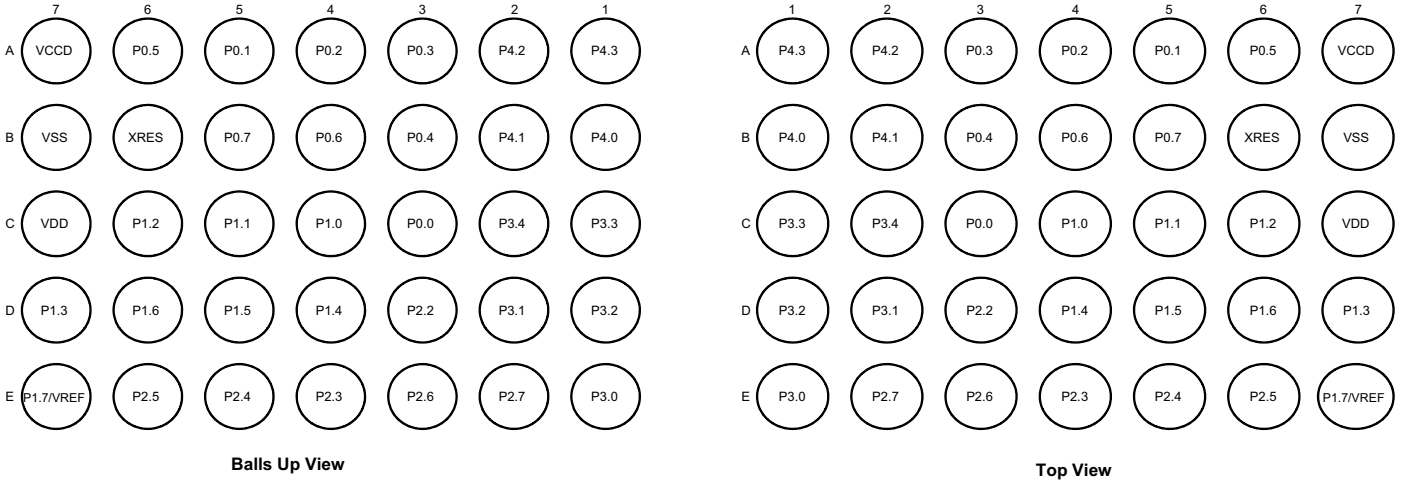
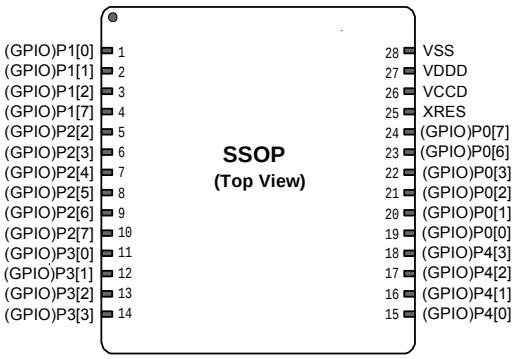


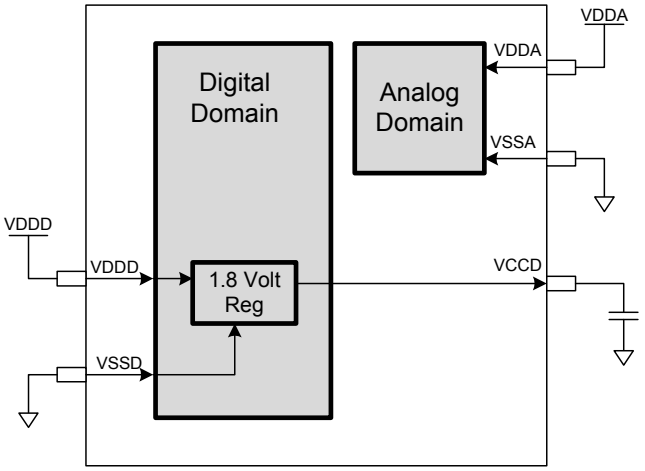

**Figure 11. 28-Pin SSOP Pinout**



## Power

The following power system diagrams show the minimum set of power supply pins as implemented for the PSoC 4200. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the $V_{DDA}$ input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

**Figure 12. PSoC 4 Power Supply**




The PSoC 4200 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

### Unregulated External Supply

In this mode, PSoC 4200 is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4200 supplies the internal logic and the $V_{CCD}$ output of PSoC 4200 must be bypassed to ground via an external capacitor (in the range of 1 µF to 1.6 µF; X5R ceramic or better).

$V_{DDA}$ and $V_{DDD}$ must be shorted together; the grounds, $V_{SSA}$ and $V_{SS}$ must also be shorted together. Bypass capacitors must be used from $V_{DDD}$ to ground, typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

**Figure 13. 48-TQFP Package Example**

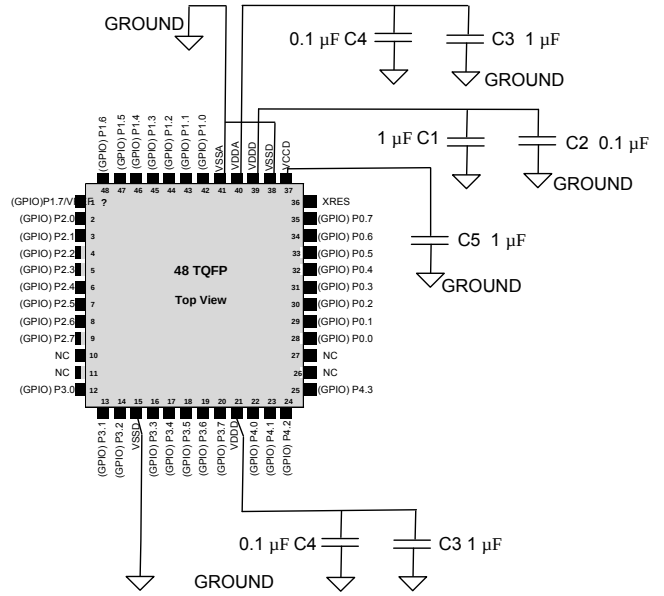
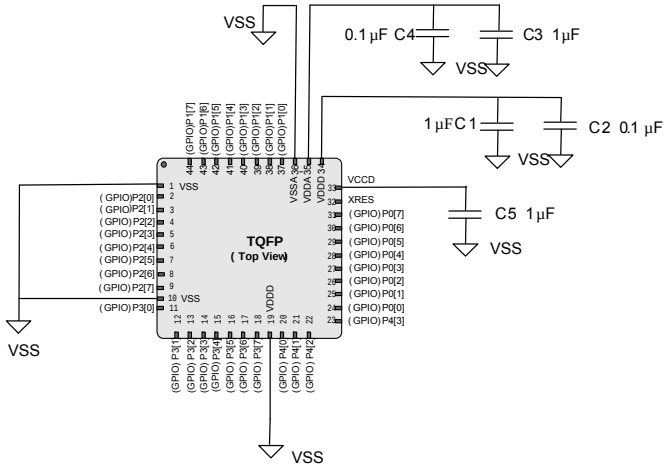



**Figure 14. 44-TQFP Package Example**




| Power Supply | Bypass Capacitors |
|---|---|
| $V_{DDD}$–$V_{SS}$ | 0.1-µF ceramic at each pin (C2, C6) plus bulk capacitor 1 µF to 10 µF (C1). Total capacitance may be greater than 10 µF. |
| $V_{DDA}$–$V_{SSA}$ | 0.1-µF ceramic at pin (C4). Additional 1 µF to 10 µF (C3) bulk capacitor. Total capacitance may be greater than 10 µF. |
| $V_{CCD}$–$V_{SS}$ | 1-µF ceramic capacitor at the VCCD pin (C5) |
| $V_{REF}$–$V_{SSA}$ (optional) | The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor. Total capacitance may be greater than 10 µF. |

## Analog Peripherals

*Opamp*

**Table 8. Opamp Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| | $I_{DD}$ | Opamp block current. No load. | – | – | – | – | |
| SID269 | $I_{DD\_HI}$ | Power = high | – | 1100 | 1850 | µA | |
| SID270 | $I_{DD\_MED}$ | Power = medium | – | 550 | 950 | µA | |
| SID271 | $I_{DD\_LOW}$ | Power = low | – | 150 | 350 | µA | |
| | GBW | Load = 20 pF, 0.1 mA. $V_{DDA}$ = 2.7 V | – | – | – | – | |
| SID272 | GBW_HI | Power = high | 6 | – | – | MHz | |
| SID273 | GBW_MED | Power = medium | 4 | – | – | MHz | |
| SID274 | GBW_LO | Power = low | – | 1 | – | MHz | |
| | $I_{OUT\_MAX}$ | $V_{DDA} \geq 2.7$ V, 500 mV from rail | – | – | – | – | |
| SID275 | $I_{OUT\_MAX\_HI}$ | Power = high | 10 | – | – | mA | |
| SID276 | $I_{OUT\_MAX\_MID}$ | Power = medium | 10 | – | – | mA | |
| SID277 | $I_{OUT\_MAX\_LO}$ | Power = low | – | 5 | – | mA | |
| | $I_{OUT}$ | $V_{DDA}$ = 1.71 V, 500 mV from rail | – | – | – | – | |
| SID278 | $I_{OUT\_MAX\_HI}$ | Power = high | 4 | – | – | mA | |
| SID279 | $I_{OUT\_MAX\_MID}$ | Power = medium | 4 | – | – | mA | |
| SID280 | $I_{OUT\_MAX\_LO}$ | Power = low | – | 2 | – | mA | |
| SID281 | $V_{IN}$ | Charge pump on, $V_{DDA} \geq 2.7$ V | –0.05 | – | VDDA – 0.2 | V | |
| SID282 | $V_{CM}$ | Charge pump on, $V_{DDA} \geq 2.7$ V | –0.05 | – | VDDA – 0.2 | V | |
| | $V_{OUT}$ | $V_{DDA} \geq 2.7$ V | – | – | – | | |
| SID283 | $V_{OUT\_1}$ | Power = high, Iload=10 mA | 0.5 | – | VDDA – 0.5 | V | |
| SID284 | $V_{OUT\_2}$ | Power = high, Iload=1 mA | 0.2 | – | VDDA – 0.2 | V | |
| SID285 | $V_{OUT\_3}$ | Power = medium, Iload=1 mA | 0.2 | – | VDDA – 0.2 | V | |
| SID286 | $V_{OUT\_4}$ | Power = low, Iload=0.1mA | 0.2 | – | VDDA – 0.2 | V | |
| SID288 | $V_{OS\_TR}$ | Offset voltage, trimmed | 1 | ±0.5 | 1 | mV | High mode |
| SID288A | $V_{OS\_TR}$ | Offset voltage, trimmed | – | ±1 | – | mV | Medium mode |
| SID288B | $V_{OS\_TR}$ | Offset voltage, trimmed | – | ±2 | – | mV | Low mode |
| SID290 | $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | –10 | ±3 | 10 | µV/°C | High mode. TA ≤ 85 °C |
| SID290Q | VOS_DR_TR | Offset voltage drift, trimmed | 15 | ±3 | 15 | µV/°C | High mode. TA ≤ 105 °C |
| SID290A | $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | – | ±10 | – | µV/°C | Medium mode |
| SID290B | $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | – | ±10 | – | µV/°C | Low mode |
| SID291 | CMRR | DC | 70 | 80 | – | dB | $V_{DDD}$ = 3.6 V |
| SID292 | PSRR | At 1 kHz, 100-mV ripple | 70 | 85 | – | dB | $V_{DDD}$ = 3.6 V |
| | Noise | | – | – | – | – | |
| SID293 | $V_{N1}$ | Input referred, 1 Hz - 1GHz, power = high | – | 94 | – | µVrms | |
| SID294 | $V_{N2}$ | Input referred, 1 kHz, power = high | – | 72 | – | nV/rtHz | |
| SID295 | $V_{N3}$ | Input referred, 10kHz, power = high | – | 28 | – | nV/rtHz | |

**Table 8. Opamp Specifications**

(Guaranteed by Characterization) *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID296 | $V_{N4}$ | Input referred, 100kHz, power = high | – | 15 | – | nV/rtHz | |
| SID297 | Cload | Stable up to maximum load. Performance specs at 50 pF. | – | – | 125 | pF | |
| SID298 | Slew_rate | Cload = 50 pF, Power = High, $V_{DDA} \geq$ 2.7 V | 6 | – | – | V/µs | |
| SID299 | T_op_wake | From disable to enable, no external RC dominating | – | 300 | – | µs | |
| SID299A | OL_GAIN | Open Loop Gain | – | 90 | – | dB | Guaranteed by design |
| | Comp_mode | Comparator mode; 50 mV drive, Trise = Tfall (approx.) | – | – | – | | |
| SID300 | $T_{PD1}$ | Response time; power = high | – | 150 | – | ns | |
| SID301 | $T_{PD2}$ | Response time; power = medium | – | 400 | – | ns | |
| SID302 | $T_{PD3}$ | Response time; power = low | – | 2000 | – | ns | |
| SID303 | Vhyst_op | Hysteresis | – | 10 | – | mV | |

*Comparatorr*

**Table 9. Comparator DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID85 | $V_{OFFSET2}$ | Input offset voltage, Common Mode voltage range from 0 to $V_{DD}$-1 | – | – | ±4 | mV | |
| SID85A | $V_{OFFSET3}$ | Input offset voltage. Ultra low-power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C) | – | ±12 | – | mV | |
| SID86 | $V_{HYST}$ | Hysteresis when enabled, Common Mode voltage range from 0 to $V_{DD}$ -1. | – | 10 | 35 | mV | Guaranteed by characterization |
| SID87 | $V_{ICM1}$ | Input common mode voltage in normal mode | 0 | – | $V_{DDD}$ – 0.1 | V | Modes 1 and 2. |
| SID247 | $V_{ICM2}$ | Input common mode voltage in low power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C) | 0 | – | $V_{DDD}$ | V | |
| SID247A | $V_{ICM3}$ | Input common mode voltage in ultra low power mode | 0 | – | $V_{DDD}$ – 1.15 | V | |
| SID88 | CMRR | Common mode rejection ratio | 50 | – | – | dB | $V_{DDD} \geq$ 2.7 V. Guaranteed by characterization |
| SID88A | CMRR | Common mode rejection ratio | 42 | – | – | dB | $V_{DDD}$ < 2.7 V. Guaranteed by characterization |
| SID89 | $I_{CMP1}$ | Block current, normal mode | – | – | 400 | µA | Guaranteed by characterization |
| SID248 | $I_{CMP2}$ | Block current, low power mode | – | – | 100 | µA | Guaranteed by characterization |
| SID259 | $I_{CMP3}$ | Block current, ultra low power mode ($V_{DDD} \geq$ 2.2 V for Temp < 0 °C, $V_{DDD} \geq$ 1.8 V for Temp > 0 °C) | – | 6 | 28 | µA | Guaranteed by characterization |

**Table 12. SAR ADC DC Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID111 | A_INL | Integral non linearity | –1.7 | – | +2 | LSB | $V_{DD}$ = 1.71 to 5.5, 1 Msps, Vref = 1 to 5.5. |
| SID111A | A_INL | Integral non linearity | –1.5 | – | +1.7 | LSB | $V_{DDD}$ = 1.71 to 3.6, 1 Msps, Vref = 1.71 to $V_{DDD}$. |
| SID111B | A_INL | Integral non linearity | –1.5 | – | +1.7 | LSB | $V_{DDD}$ = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5. |
| SID112 | A_DNL | Differential non linearity | –1 | – | +2.2 | LSB | $V_{DDD}$ = 1.71 to 5.5, 1 Msps, Vref = 1 to 5.5. |
| SID112A | A_DNL | Differential non linearity | –1 | – | +2 | LSB | $V_{DDD}$ = 1.71 to 3.6, 1 Msps, Vref = 1.71 to $V_{DDD}$. |
| SID112B | A_DNL | Differential non linearity | –1 | – | +2.2 | LSB | $V_{DDD}$ = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5. |

**Table 13. SAR ADC AC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID108 | A_SAMP_1 | Sample rate with external reference bypass cap | – | – | 1 | Msps | |
| SID108A | A_SAMP_2 | Sample rate with no bypass cap. Reference = $V_{DD}$ | – | – | 500 | Ksps | |
| SID108B | A_SAMP_3 | Sample rate with no bypass cap. Internal reference | – | – | 100 | Ksps | |
| SID109 | A_SNDR | Signal-to-noise and distortion ratio (SINAD) | 65 | – | – | dB | $F_{IN}$ = 10 kHz |
| SID113 | A_THD | Total harmonic distortion | – | – | –65 | dB | $F_{IN}$ = 10 kHz. |

## System Resources

*Power-on-Reset (POR) with Brown Out*

**Table 28. Imprecise Power On Reset (IPOR)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID185 | $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.45 | V | Guaranteed by characterization |
| SID186 | $V_{FALLIPOR}$ | Falling trip voltage | 0.75 | – | 1.4 | V | Guaranteed by characterization |
| SID187 | $V_{IPORHYST}$ | Hysteresis | 15 | – | 200 | mV | Guaranteed by characterization |

**Table 29. Precise Power On Reset (POR)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID190 | $V_{FALLPPOR}$ | BOD trip voltage in active and sleep modes | 1.64 | – | – | V | Full functionality between 1.71 V and BOD trip voltage is guaranteed by characterization |
| SID192 | $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep | 1.4 | – | – | V | Guaranteed by characterization |
| BID55 | Svdd | Maximum power supply ramp rate | – | – | 67 | kV/sec | |

*Voltage Monitors*

**Table 30. Voltage Monitors DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID195 | $V_{LVI1}$ | LVI_A/D_SEL[3:0] = 0000b | 1.71 | 1.75 | 1.79 | V | |
| SID196 | $V_{LVI2}$ | LVI_A/D_SEL[3:0] = 0001b | 1.76 | 1.80 | 1.85 | V | |
| SID197 | $V_{LVI3}$ | LVI_A/D_SEL[3:0] = 0010b | 1.85 | 1.90 | 1.95 | V | |
| SID198 | $V_{LVI4}$ | LVI_A/D_SEL[3:0] = 0011b | 1.95 | 2.00 | 2.05 | V | |
| SID199 | $V_{LVI5}$ | LVI_A/D_SEL[3:0] = 0100b | 2.05 | 2.10 | 2.15 | V | |
| SID200 | $V_{LVI6}$ | LVI_A/D_SEL[3:0] = 0101b | 2.15 | 2.20 | 2.26 | V | |
| SID201 | $V_{LVI7}$ | LVI_A/D_SEL[3:0] = 0110b | 2.24 | 2.30 | 2.36 | V | |
| SID202 | $V_{LVI8}$ | LVI_A/D_SEL[3:0] = 0111b | 2.34 | 2.40 | 2.46 | V | |
| SID203 | $V_{LVI9}$ | LVI_A/D_SEL[3:0] = 1000b | 2.44 | 2.50 | 2.56 | V | |
| SID204 | $V_{LVI10}$ | LVI_A/D_SEL[3:0] = 1001b | 2.54 | 2.60 | 2.67 | V | |
| SID205 | $V_{LVI11}$ | LVI_A/D_SEL[3:0] = 1010b | 2.63 | 2.70 | 2.77 | V | |
| SID206 | $V_{LVI12}$ | LVI_A/D_SEL[3:0] = 1011b | 2.73 | 2.80 | 2.87 | V | |
| SID207 | $V_{LVI13}$ | LVI_A/D_SEL[3:0] = 1100b | 2.83 | 2.90 | 2.97 | V | |
| SID208 | $V_{LVI14}$ | LVI_A/D_SEL[3:0] = 1101b | 2.93 | 3.00 | 3.08 | V | |
| SID209 | $V_{LVI15}$ | LVI_A/D_SEL[3:0] = 1110b | 3.12 | 3.20 | 3.28 | V | |
| SID210 | $V_{LVI16}$ | LVI_A/D_SEL[3:0] = 1111b | 4.39 | 4.50 | 4.61 | V | |
| SID211 | LVI_IDD | Block current | – | – | 100 | µA | Guaranteed by characterization |

**Table 31. Voltage Monitors AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID212 | $T_{MONTRIP}$ | Voltage monitor trip time | – | – | 1 | µs | Guaranteed by characterization |

*SWD Interface*

**Table 32. SWD Interface Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID213 | F_SWDCLK1 | 3.3 V ≤ $V_{DD}$ ≤ 5.5 V | – | – | 14 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| SID214 | F_SWDCLK2 | 1.71 V ≤ $V_{DD}$ ≤ 3.3 V | – | – | 7 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| SID215 | T_SWDI_SETUP | T = 1/f SWDCLK | 0.25*T | – | – | ns | Guaranteed by characterization |
| SID216 | T_SWDI_HOLD | T = 1/f SWDCLK | 0.25*T | – | – | ns | Guaranteed by characterization |
| SID217 | T_SWDO_VALID | T = 1/f SWDCLK | – | – | 0.5*T | ns | Guaranteed by characterization |
| SID217A | T_SWDO_HOLD | T = 1/f SWDCLK | 1 | – | – | ns | Guaranteed by characterization |

*Internal Main Oscillator*

**Table 33. IMO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID218 | $I_{IMO1}$ | IMO operating current at 48 MHz | – | – | 1000 | µA | |
| SID219 | $I_{IMO2}$ | IMO operating current at 24 MHz | – | – | 325 | µA | |
| SID220 | $I_{IMO3}$ | IMO operating current at 12 MHz | – | – | 225 | µA | |
| SID221 | $I_{IMO4}$ | IMO operating current at 6 MHz | – | – | 180 | µA | |
| SID222 | $I_{IMO5}$ | IMO operating current at 3 MHz | – | – | 150 | µA | |

**Table 34. IMO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID223 | $F_{IMOTOL1}$ | Frequency variation from 3 to 48 MHz | – | – | ±2 | % | ±3% if $T_A$ > 85 °C and IMO frequency < 24 MHz |
| SID226 | $T_{STARTIMO}$ | IMO startup time | – | – | 12 | µs | |
| SID227 | $T_{JITRMSIMO1}$ | RMS Jitter at 3 MHz | – | 156 | – | ps | |
| SID228 | $T_{JITRMSIMO2}$ | RMS Jitter at 24 MHz | – | 145 | – | ps | |
| SID229 | $T_{JITRMSIMO3}$ | RMS Jitter at 48 MHz | – | 139 | – | ps | |

*Internal Low-Speed Oscillator*

**Table 35. ILO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID231 | $I_{ILO1}$ | ILO operating current at 32 kHz | – | 0.3 | 1.05 | µA | Guaranteed by Characterization |
| SID233 | $I_{ILOLEAK}$ | ILO leakage current | – | 2 | 15 | nA | Guaranteed by Design |

**Table 39. Block Specs**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID256* | $T_{WS48}$* | Number of wait states at 48 MHz | 1 | – | – | | CPU execution from Flash. Guaranteed by characterization |
| SID257 | $T_{WS24}$* | Number of wait states at 24 MHz | 0 | – | – | | CPU execution from Flash. Guaranteed by characterization |
| SID260 | $V_{REFSAR}$ | Trimmed internal reference to SAR | –1 | – | +1 | % | Percentage of Vbg (1.024 V). Guaranteed by characterization |
| SID262 | $T_{CLKSWITCH}$ | Clock switching from clk1 to clk2 in clk1 periods | 3 | – | 4 | Periods | . Guaranteed by design |
| * Tws48 and Tws24 are guaranteed by Design | | | | | | | |

**Table 40. UDB Port Adaptor Specifications**

(Based on LPC Component Specs, Guaranteed by Characterization -10-pF load, 3-V $V_{DDIO}$ and $V_{DDD}$)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID263 | $T_{LCLKDO}$ | LCLK to output delay | – | – | 18 | ns | |
| SID264 | $T_{DINLCLK}$ | Input setup time to LCLCK rising edge | – | – | 7 | ns | |
| SID265 | $T_{DINLCLKHLD}$ | Input hold time from LCLK rising edge | 5 | – | – | ns | |
| SID266 | $T_{LCLKHIZ}$ | LCLK to output tristated | – | – | 28 | ns | |
| SID267 | $T_{FLCLK}$ | LCLK frequency | – | – | 33 | MHz | |
| SID268 | $T_{LCLKDUTY}$ | LCLK duty cycle (percentage high) | 40 | – | 60 | % | |

## Ordering Information

The PSoC 4200 part numbers and features are listed in the following table.

**Table 41. PSoC 4200 Family Ordering Information**

| Family | MPN | Features | | | | | | | | | | | | Package | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Max CPU Speed (MHz) | Flash (KB) | SRAM (KB) | UDB | Op-amp (CTBm) | CapSense | Direct LCD Drive | 12-bit SAR ADC | LP Comparators | TCPWM Blocks | SCB Blocks | GPIO | 28-SSOP | 35-WLCSP | 40-QFN | 44-TQFP | 48-TQFP |
| 4200 | CY8C4244PVI-432 | 48 | 16 | 4 | 2 | 1 | - | - | 1 Msps | 2 | 4 | 2 | 24 | √ | | | | |
| | CY8C4244PVI-442 | 48 | 16 | 4 | 2 | 1 | √ | √ | 1 Msps | 2 | 4 | 2 | 24 | √ | | | | |
| | CY8C4244PVQ-432 | 48 | 16 | 4 | 2 | 1 | - | - | 1 Msps | 2 | 4 | 2 | 24 | √ | | | | |
| | CY8C4244PVQ-442 | 48 | 16 | 4 | 2 | 1 | √ | √ | 1 Msps | 2 | 4 | 2 | 24 | √ | | | | |
| | CY8C4244FNI-443 | 48 | 16 | 4 | 2 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 31 | | √ | | | |
| | CY8C4244LQI-443 | 48 | 16 | 4 | 2 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 34 | | | √ | | |
| | CY8C4244AXI-443 | 48 | 16 | 4 | 2 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 36 | | | | √ | |
| | CY8C4244LQQ-443 | 48 | 16 | 4 | 2 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 34 | | | √ | | |
| | CY8C4244AXQ-443 | 48 | 16 | 4 | 2 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 36 | | | | √ | |
| | CY8C4244AZI-443 | 48 | 16 | 4 | 2 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 36 | | | | | √ |
| | CY8C4245AXI-473 | 48 | 32 | 4 | 4 | 2 | - | - | 1 Msps | 2 | 4 | 2 | 36 | | | | √ | |
| | CY8C4245AXQ-473 | 48 | 32 | 4 | 4 | 2 | - | - | 1 Msps | 2 | 4 | 2 | 36 | | | | √ | |
| | CY8C4245AZI-473 | 48 | 32 | 4 | 4 | 2 | - | - | 1 Msps | 2 | 4 | 2 | 36 | | | | | √ |
| | CY8C4245PVI-482 | 48 | 32 | 4 | 4 | 1 | √ | √ | 1 Msps | 2 | 4 | 2 | 24 | √ | | | | |
| | CY8C4245PVQ-482 | 48 | 32 | 4 | 4 | 1 | √ | √ | 1 Msps | 2 | 4 | 2 | 24 | √ | | | | |
| | CY8C4245FNI-483(T) | 48 | 32 | 4 | 4 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 31 | | √ | | | |
| | CY8C4245LQI-483 | 48 | 32 | 4 | 4 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 34 | | | √ | | |
| | CY8C4245AXI-483 | 48 | 32 | 4 | 4 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 36 | | | | √ | |
| | CY8C4245LQQ-483 | 48 | 32 | 4 | 4 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 34 | | | √ | | |
| | CY8C4245AXQ-483 | 48 | 32 | 4 | 4 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 36 | | | | √ | |
| | CY8C4245AZI-483 | 48 | 32 | 4 | 4 | 2 | √ | √ | 1 Msps | 2 | 4 | 2 | 36 | | | | | √ |

## Packaging

**Table 42. Package Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | | –40 | 25.00 | 105 | °C |
| $T_J$ | Operating junction temperature | | –40 | – | 125 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ (28-pin SSOP) | | – | 66.58 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (35-ball WLCSP) | | – | 28.00 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (40-pin QFN) | | – | 15.34 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (44-pin TQFP) | | – | 57.16 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (48-pin TQFP) | | – | 67.30 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (28-pin SSOP) | | – | 26.28 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (35-ball WLCSP) | | – | 00.40 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (40-pin QFN) | | – | 2.50 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (44-pin TQFP) | | – | 17.47 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (48-pin TQFP) | | – | 27.60 | – | °C/Watt |

**Table 43. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| 28-pin SSOP | 260 °C | 30 seconds |
| 35-ball WLCSP | 260 °C | 30 seconds |
| 40-pin QFN | 260 °C | 30 seconds |
| 44-pin TQFP | 260 °C | 30 seconds |
| 48-pin TQFP | 260 °C | 30 seconds |

**Table 44. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 28-pin SSOP | MSL 3 |
| 35-ball WLCSP | MSL 3 |
| 40-pin QFN | MSL 3 |
| 44-pin TQFP | MSL 3 |
| 48-pin TQFP | MSL 3 |

PSoC 4 CAB Libraries with Schematics Symbols and PCB Footprints are on the Cypress web site at http://www.cypress.com/cad-resources/psoc-4-cad-libraries?source=search&cat=technical_documents.

**Figure 17. 28-pin (210-mil) SSOP Package Outline**

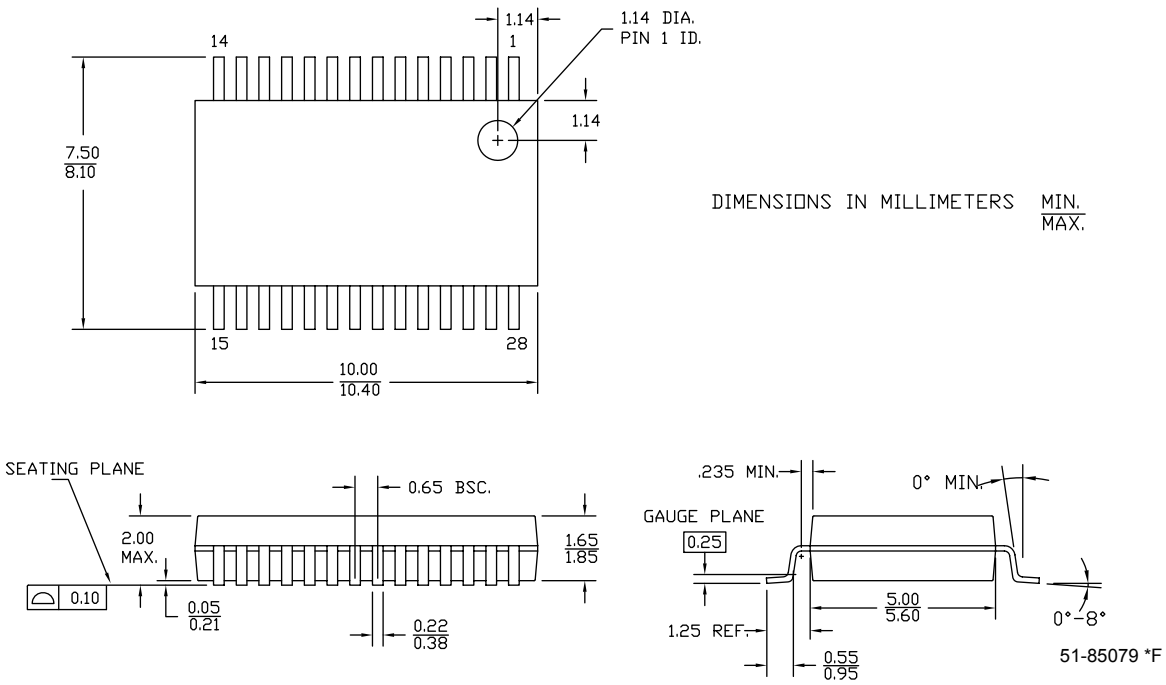
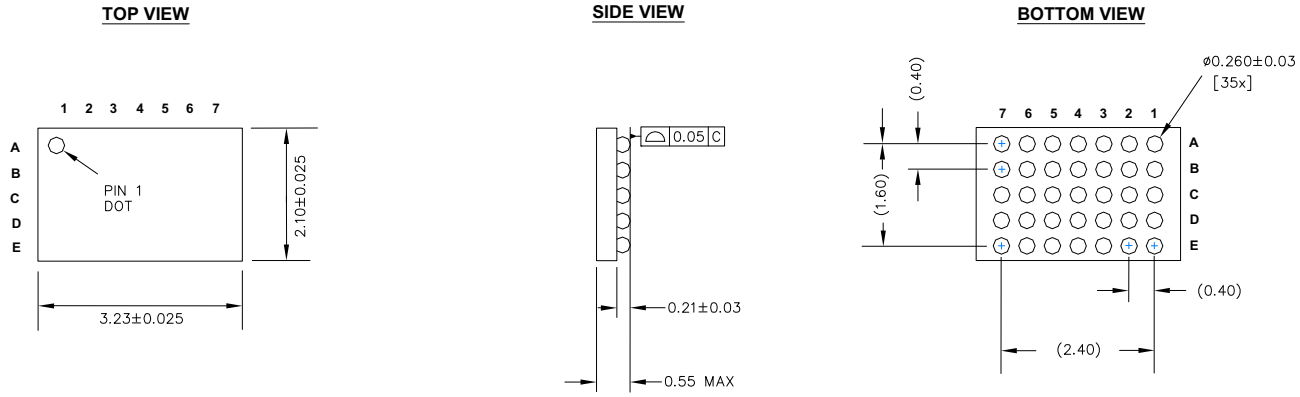



**Figure 18. 35-ball WLCSP Package Outline**




**NOTES:**

**1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18**

**2. ALL DIMENSIONS ARE IN MILLIMETERS**

001-93741 **

## Acronyms

**Table 45. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| ARM® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

**Table 45. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |

**Table 45. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | $I^2C$ serial clock |
| SDA | $I^2C$ serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |

**Table 45. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

## Document Conventions

### Units of Measure

**Table 46. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

## Revision History

| Description Title: PSoC® 4: PSoC 4200 Family Datasheet Programmable System-on-Chip (PSoC®)<br>Document Number: 001-87197 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *B | 4108562 | WKA | 08/29/2013 | Added clarifying note about the XRES pin in the Reset section.<br>Updated UDB Array diagram.<br>Added a link reference to the PSoC 4 TRM.<br>Updated the footnote in Absolute Maximum Ratings.<br>Updated Sleep Mode IDD specs in DC Specifications.<br>Updated Comparator DC Specifications<br>Updated SAR ADC AC Specifications<br>Updated LCD Direct Drive DC Specifications<br>Updated the number of GPIOs in Ordering Information. |
| *C | 4568937 | MKEA/ WKA | 11/19/2014 | Added More Information and PSoC Creator sections.<br>Added 48-pin TQFP pin and package details.<br>Added SID308A spec details.<br>Updated Ordering Information. |
| *D | 4617283 | WKA | 01/08/2015 | Corrected typo in the ordering information table.<br>Updated 28-pin SSOP package diagram. |
| *E | 4643655 | WKA | 04/29/2015 | Added 35 WLCSP pinout and package detail information.<br>Updated CSD specifications. |
| *F | 5287114 | WKA | 06/09/2016 | Added reference to AN90071 in the More Information section.<br>Updated Flash section with details of flash protection modes.<br>Added notes in the Pinouts section.<br>Updated 40-pin QFN and 28-pin SSOP pin diagrams.<br>Added PSoC 4 Power Supply diagram.<br>Updated the Bypass Capacitors column in the Power Supply table.<br>Updated values for SID32, SID34, SID38, SID269, SID270, SID271.<br>Added SID299A.<br>Updated Comparator Specifications.<br>Updated TCPWM Specifications.<br>Updated values for SID149, SID160, SID171.<br>Updated Conditions for SID190.<br>Added BID55.<br>Removed Conditions for SID237.<br>Added reference to PSoC 4 CAB Libraries with Schematics Symbols and PCB Footprints in the Packaging section. |
| *G | 5327384 | WKA | 06/28/2016 | Removed capacitor connection for Pin 15 in Figure 13. |
| *H | 5702140 | GNKK | 04/19/2017 | Updated the Cypress logo and copyright information. |