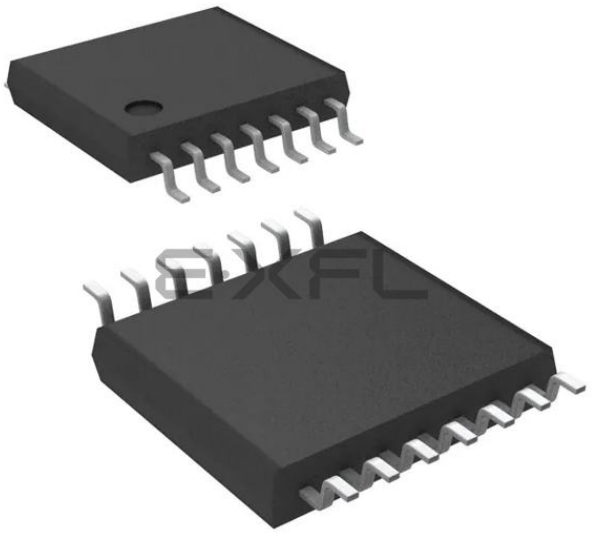

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	SPI
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	12
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc912fdh-129

5. Block diagram

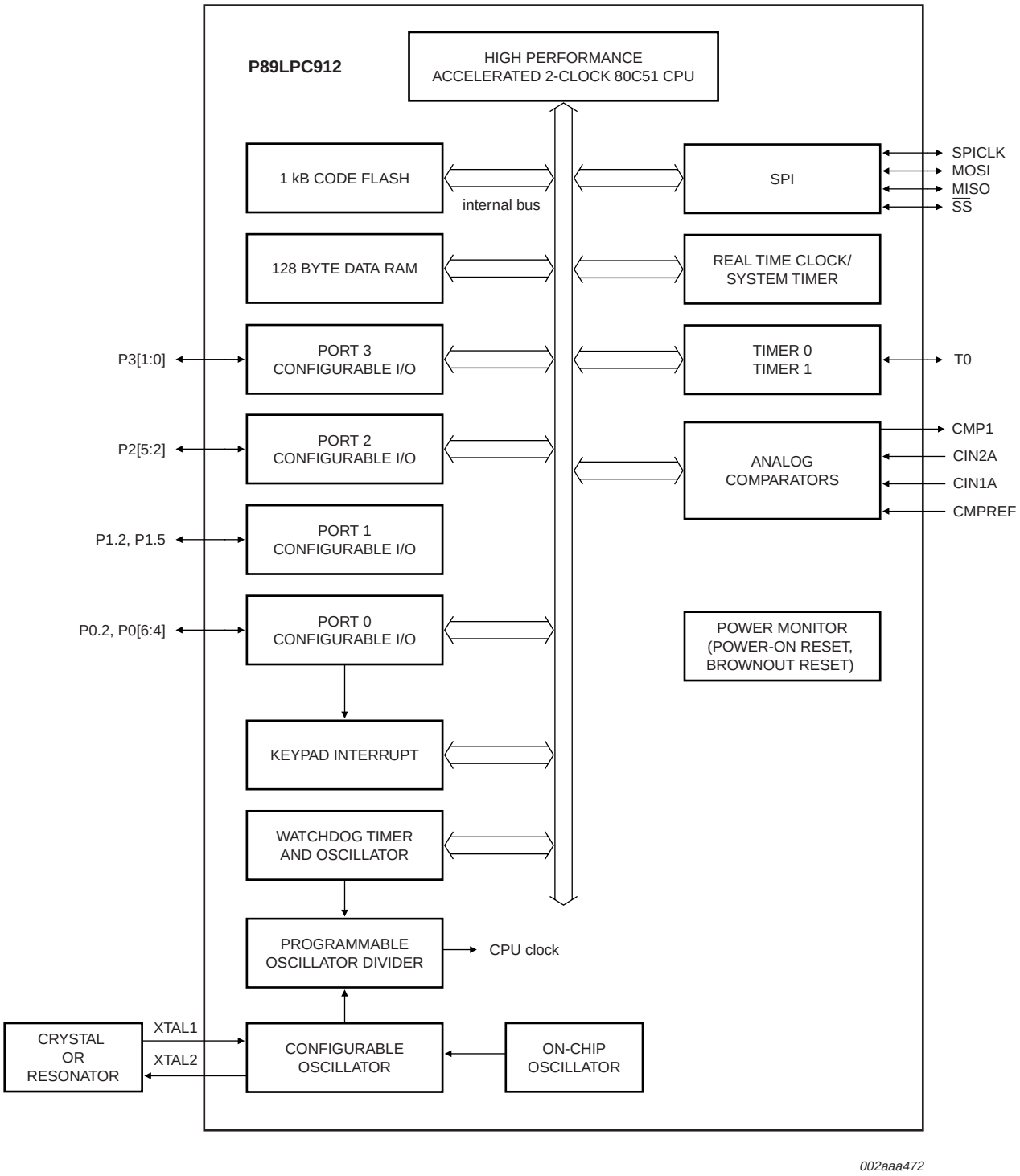


Fig 1. P89LPC912 block diagram

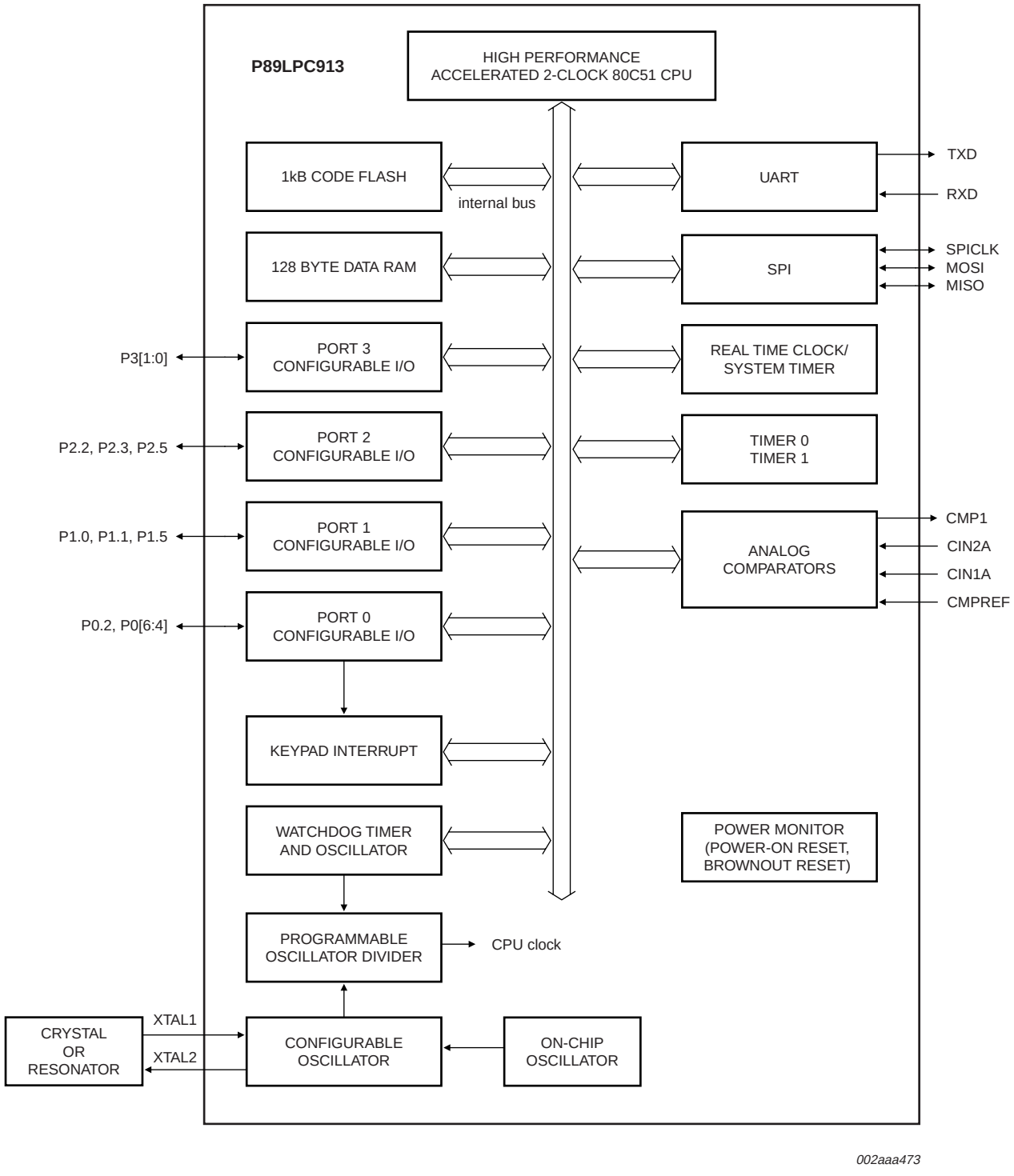


Fig 2. P89LPC913 block diagram

6. Functional diagram

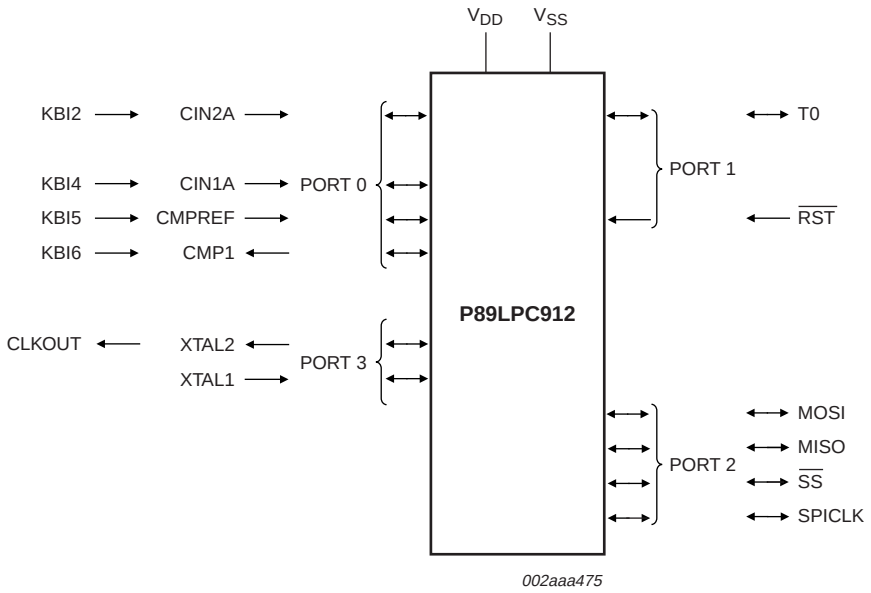


Fig 4. P89LPC912 functional diagram

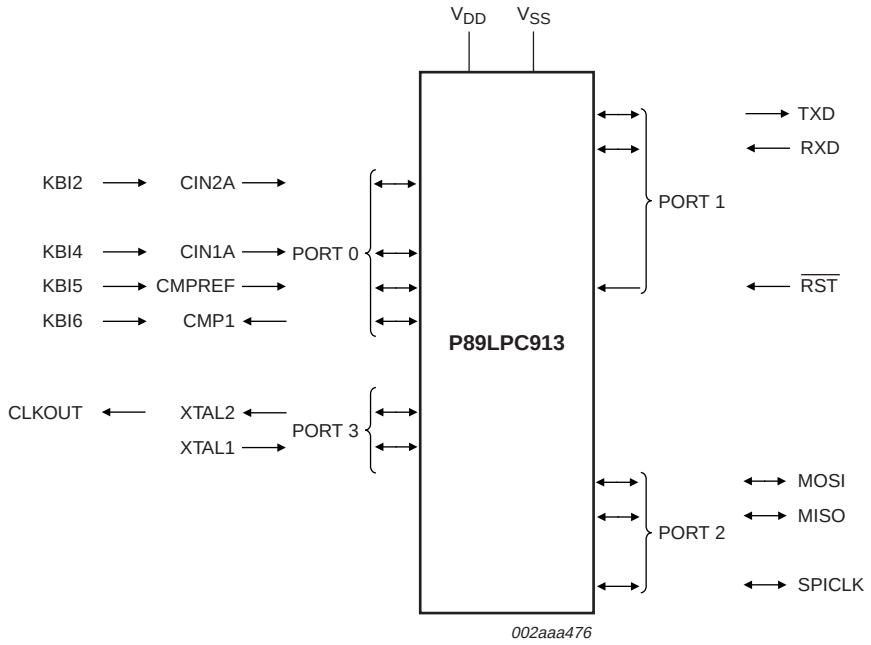


Fig 5. P89LPC913 functional diagram

Table 5. P89LPC913 pin description

Symbol	Pin	Type	Description
P0.2, P0.4 to P0.6		I/O	**Port 0:** Port 0 is a 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.2/CIN2A/ KBI2	13	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
P0.4/CIN1A/ KBI4	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
P0.5/CMPREF/ KBI5	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	5	I/O	**P0.6 —** Port 0 bit 6.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
P1.0, P1.1, P1.5		I/O (P1.0, P1.1); I (P1.5)	**Port 1:** Port 1 is a 3-bit I/O port with a user-configurable output type, except for P1.5 noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	9	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	6	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for the serial port.
P1.5/$\overline{\text{RST}}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

Table 5. P89LPC913 pin description *...continued*

Symbol	Pin	Type	Description
P2.2, P2.3, P2.5		I/O	**Port 2:** Port 2 is a 3-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	8	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
P3.1/XTAL1	7	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

8. Functional description

Remark: Please refer to the P89LPC912/913/914 *User manual* for a more detailed functional description.

8.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 7. P89LPC912 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H		CMP1/ KB6	CMPREF / KB5	CIN1A/ KB4		CIN2A/ KB2			[1]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H			$\overline{\text{RST}}$			T0			[1]	
		Bit address	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
P2*	Port 2	A0H			SPICLK	$\overline{\text{SS}}$	MISO	MOSI			[1]	
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H							XTAL1	XTAL2	[1]	
P0M1	Port 0 output mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)			FF	1111 1111
P0M2	Port 0 output mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)			00	0000 0000
P1M1	Port 1 output mode 1	91H						(P1M1.2)			D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H						(P1M2.2)		-	00[1]	00x0 xx00
P2M1	Port 2 output mode 1	A4H			(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)			FF	1111 1111
P2M2	Port 2 output mode 2	A5H			(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)			00	0000 0000
P3M1	Port 3 output mode 1	B1H							(P3M1.1)	(P3M1.0)	03[1]	xxxx xx11
P3M2	Port 3 output mode 2	B2H							(P3M2.1)	(P3M2.0)	00[1]	xxxx xx00
PCON	Power control register	87H	-	-	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	-	SPPD	-	-	00[1]	0000 0000
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF	R_EX	[2]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][5]	011x xx00
RTCH	Real-time clock register high	D2H									00[5]	0000 0000

Table 7. P89LPC912 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RTCL	Real-time clock register low	D3H									00[5]	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	-	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[4] [5]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[3] [5]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] The RSTSRC register reflects the cause of the P89LPC912 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[3] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[4] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[5] The only reset source that affects these SFRs is power-on reset.

Table 8. P89LPC913 Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any of them is written if BRGEN = 1, result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC912 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

Table 9. P89LPC914 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		**E7**	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**	**E0**		
ACC*	Accumulator	E0H									00	0000 0000
AUXR1	Auxiliary function register	A2H	-	EBRR	-	ENT0	SRST	0	-	DPS	00[1]	0000 00x0
	Bit address		**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator rate low	BEH									00	0000 0000
BRGR1[2]	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[6]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H	-	-	-	-	-	-			00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	0000 0000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	-	00[1]	00x0 0000

8.2 Enhanced CPU

The P89LPC912/913/914 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.3 Clocks

8.3.1 Clock definitions

The P89LPC912/913/914 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 10, 11, and 12) and can also be optionally divided to a slower frequency (see Section 8.8 “CCLK modification: DIVM register”).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.3.2 CPU clock (OSCCLK)

The P89LPC912/913/914 provide user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator and an on-chip RC oscillator.

In addition, both the P89LPC912 and P89LPC913 provide an oscillator using an external crystal or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.3.3 Low-speed oscillator option (P89LPC912, P89LPC913)

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.3.4 Medium-speed oscillator option (P89LPC912, P89LPC913)

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.3.5 High-speed oscillator option (P89LPC912, P89LPC913)

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

Table 10. Number of I/O pins available (P89LPC912, P89LPC913)

Clock source	Reset option	Number of I/O pins (14-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	12
	External $\overline{RST}$ pin supported	11
External clock input	No external reset (except during power-up)	11
	External $\overline{RST}$ pin supported	10
Low/medium/high-speed oscillator (external crystal or resonator)	No external reset (except during power-up)	10
	External $\overline{RST}$ pin supported[1]	9

[1] Required for operation above 12 MHz.

The P89LPC914 has three I/O ports: Port 0, Port 1, and Port 2. The exact number of I/O pins available depends upon the reset option chosen, as shown in Table 11.

Table 11. Number of I/O pins available (P89LPC914)

Reset option	Number of I/O pins (14-pin package)
No external reset (except during power-up)	12
External $\overline{RST}$ pin supported[1]	11

[1] Required for operation above 12 MHz.

8.12.1 Port configurations

Except as listed below, every I/O pin on the P89LPC912/913/914 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5/$\overline{RST}$ can only be an input and cannot be configured.

P1.2/T0 may only be configured to be either input-only or open drain (P89LPC912, P89LPC914).

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC912/913/914 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.14.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC912/913/914 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM data retention voltage V_{DDR}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators (note that comparators can be powered-down separately), and RTC/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled.

8.14.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

8.15 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

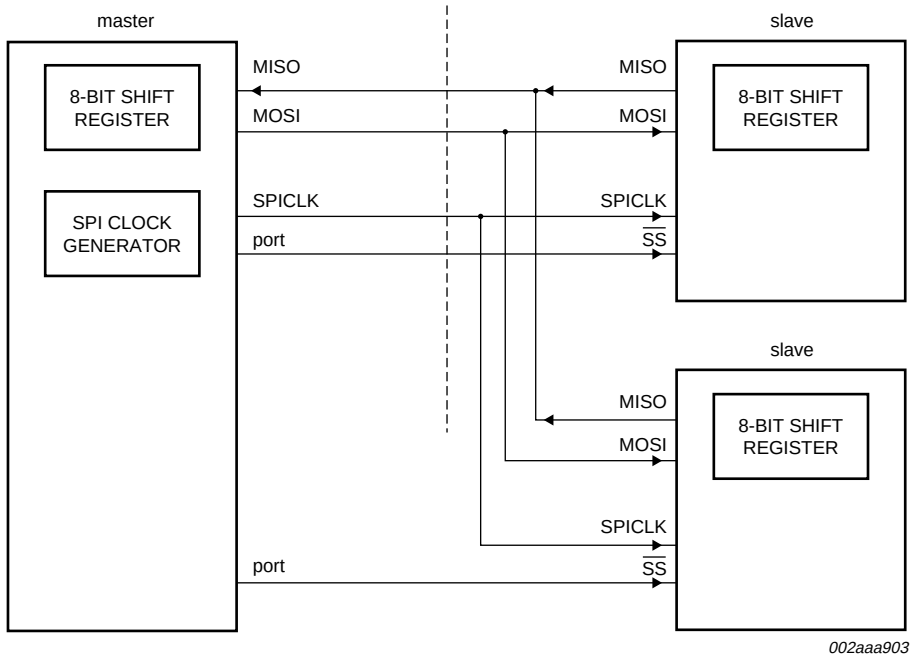


Fig 19. SPI single master multiple slaves configuration

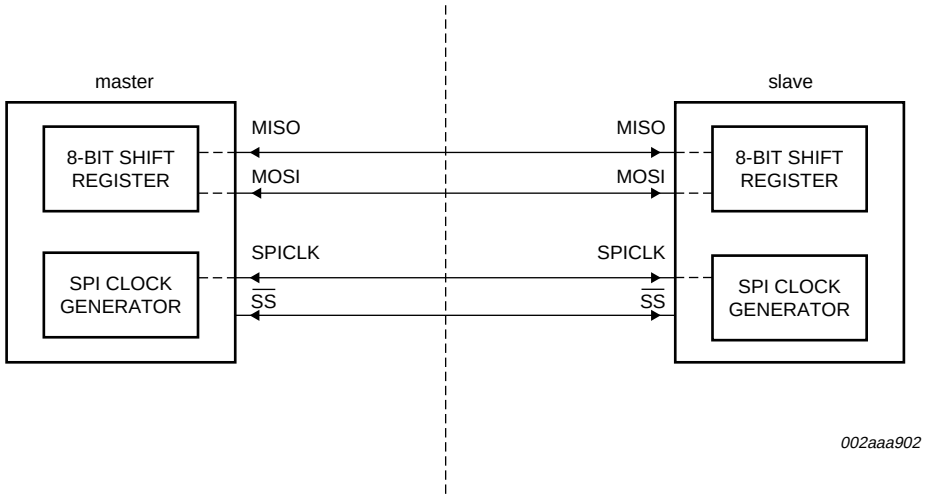


Fig 20. SPI dual device configuration, where either can be a master or a slave

8.27.4 Flash programming and erasing

Different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP-Lite) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock- serial data interface using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire 1 kB of user code space.

8.27.5 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC912/913/914 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector (with V_{DD}, V_{SS}, $\overline{RST}$, clock, and data signals) needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC912/913/914 *User manual*.

8.27.6 In-application programming (IAP-Lite)

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP-Lite facility consists of internal hardware resources to facilitate programming and erasing. The NXP In-Application Programming Lite has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC912/913/914 *User manual*.

8.27.7 Using flash as data storage

The flash code memory array of this device supports **individual** byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.27.8 User configuration bytes

Some user-configurable features of the P89LPC912/913/914 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC912/913/914 *User manual* for additional details.

8.27.9 User sector security bytes

There are four User Sector Security Bytes, each corresponding to one sector. Please see the P89LPC912/913/914 *User manual* for additional details.

9. Limiting values

Table 12. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	120	mA
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 12 “Limiting values”:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Table 13. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0	2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage		1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, V_{DD} = 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$ and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer (P89LPC912, P89LPC913).

[3] The $I_{DD(oper)}$, $I_{DD(idle)}$ and $I_{DD(pd)}$ specifications are measured with the following functions disabled: comparators, brownout detect, and watchdog timer (P89LPC914).

[4] Pin capacitance is characterized but not tested.

[5] Measured with port in quasi-bidirectional mode.

[6] Measured with port in high-impedance mode.

[7] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups)

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 15. Dynamic characteristics (P89LPC912, P89LPC913)

V_{DD} = 3.0 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions		Variable clock		f_{osc} = 18 MHz		Unit
				Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 °C		7.189	7.557	7.189	7.557	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	nominal f = 400 kHz		320	520	320	520	kHz
Crystal oscillator								
f_{osc}	oscillator frequency		[2]	0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 25		55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency			0	8	-	-	MHz
Glitch filter								
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin		-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin		125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock								
t_{CHCX}	clock HIGH time	see Figure 25		22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 25		22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 25		-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 25		-	5	-	5	ns
SPI interface								
f_{SPI}	SPI operating frequency							
	3.0 MHz (slave)			0	$^{CCLK}/_{6}$	0	3	MHz
	4.5 MHz (master)			-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 26, 27, 28, 29						
	slave			$^{6}/_{CCLK}$	-	333	-	ns
	master			$^{4}/_{CCLK}$	-	222	-	ns

Table 15. Dynamic characteristics (P89LPC912, P89LPC913) *…continued*

V_{DD} = 3.0 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
t_{SPIF}	SPI fall time	see Figure 26, 27, 28, 29					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

11.1 Waveforms

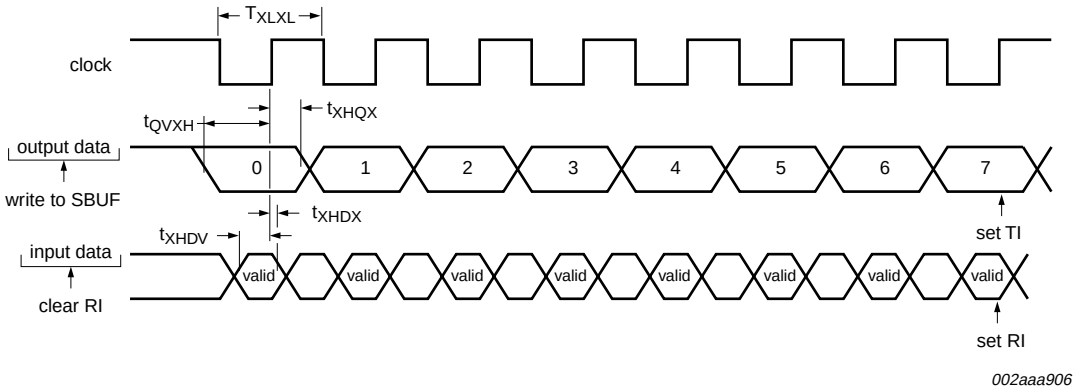


Fig 24. Shift register mode timing

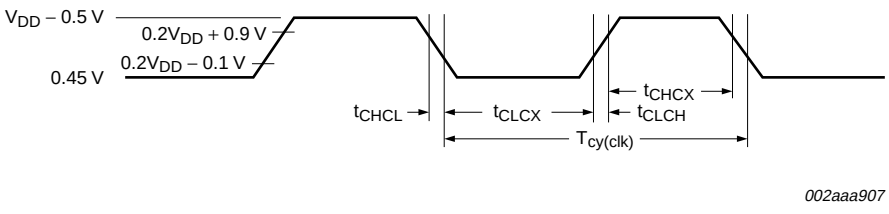
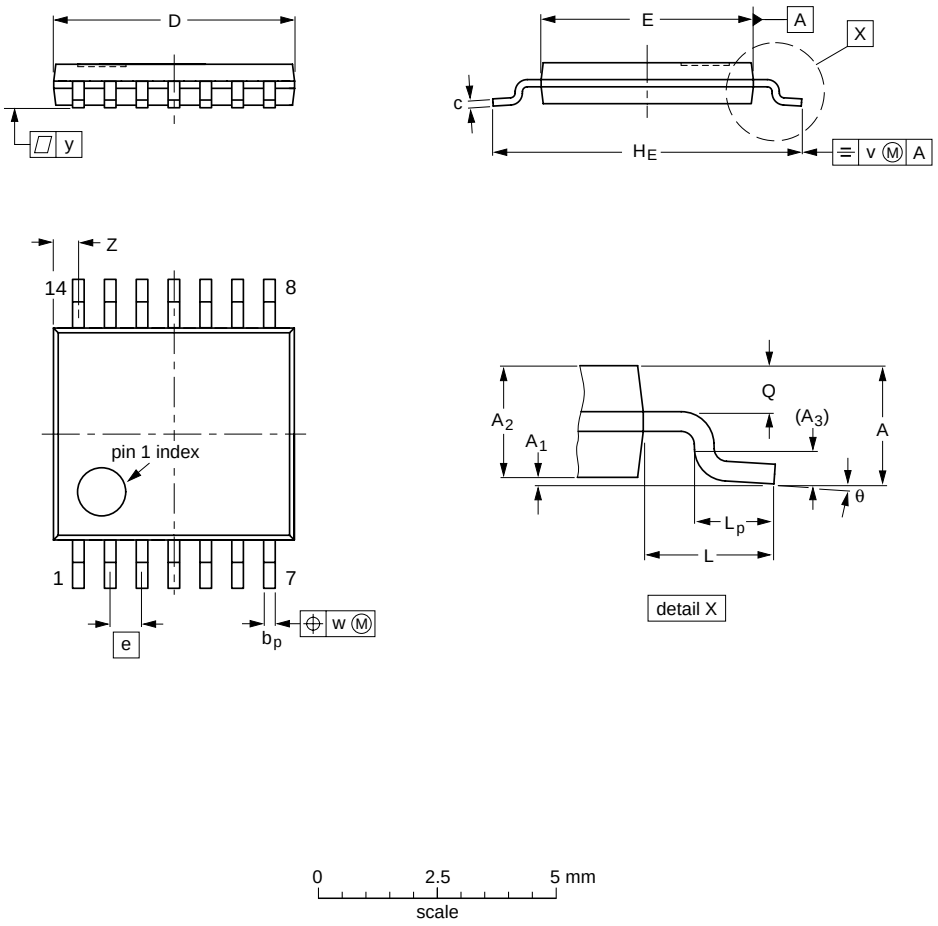


Fig 25. External clock timing

13. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 30. Package outline SOT402-1 (TSSOP14)