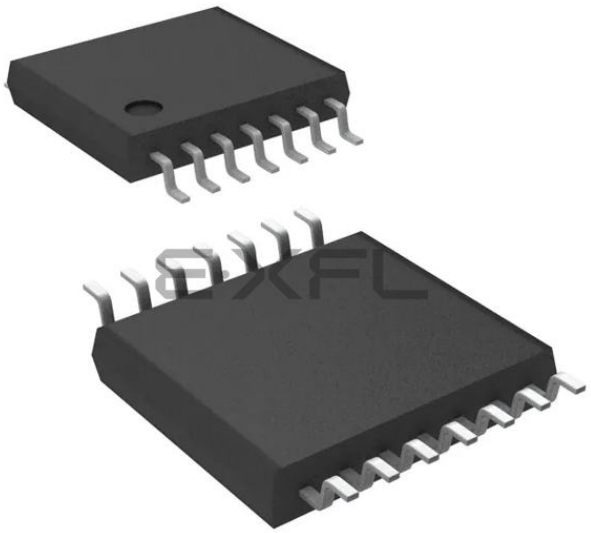

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	12
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc913fdh-129

3. Product comparison

Table 1 highlights the differences between these three devices. For a complete list of device features, please see Section 2 “Features” on page 1.

Table 1. Product comparison

Type number	External crystal pins	X2 CLKOUT	T0 PWM output	SPI with $\overline{SS}$ pin	SPI without $\overline{SS}$ pin	UART		Max f_{osc} (MHz)
						TXD	RXD	
P89LPC912	X	X	X	X	-	-	-	18
P89LPC913	X	X	-	-	X	X	X	18
P89LPC914	-	-	X	X	-	X	X	12

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC912FDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC912HDH			
P89LPC913FDH			
P89LPC914FDH			

4.1 Ordering options

Table 3. Ordering options

Type number	Temperature range	Frequency
P89LPC912FDH	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC912HDH	–40 °C to +125 °C	0 MHz to 18 MHz
P89LPC913FDH	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC914FDH	–40 °C to +85 °C	0 MHz to 12 MHz

5. Block diagram

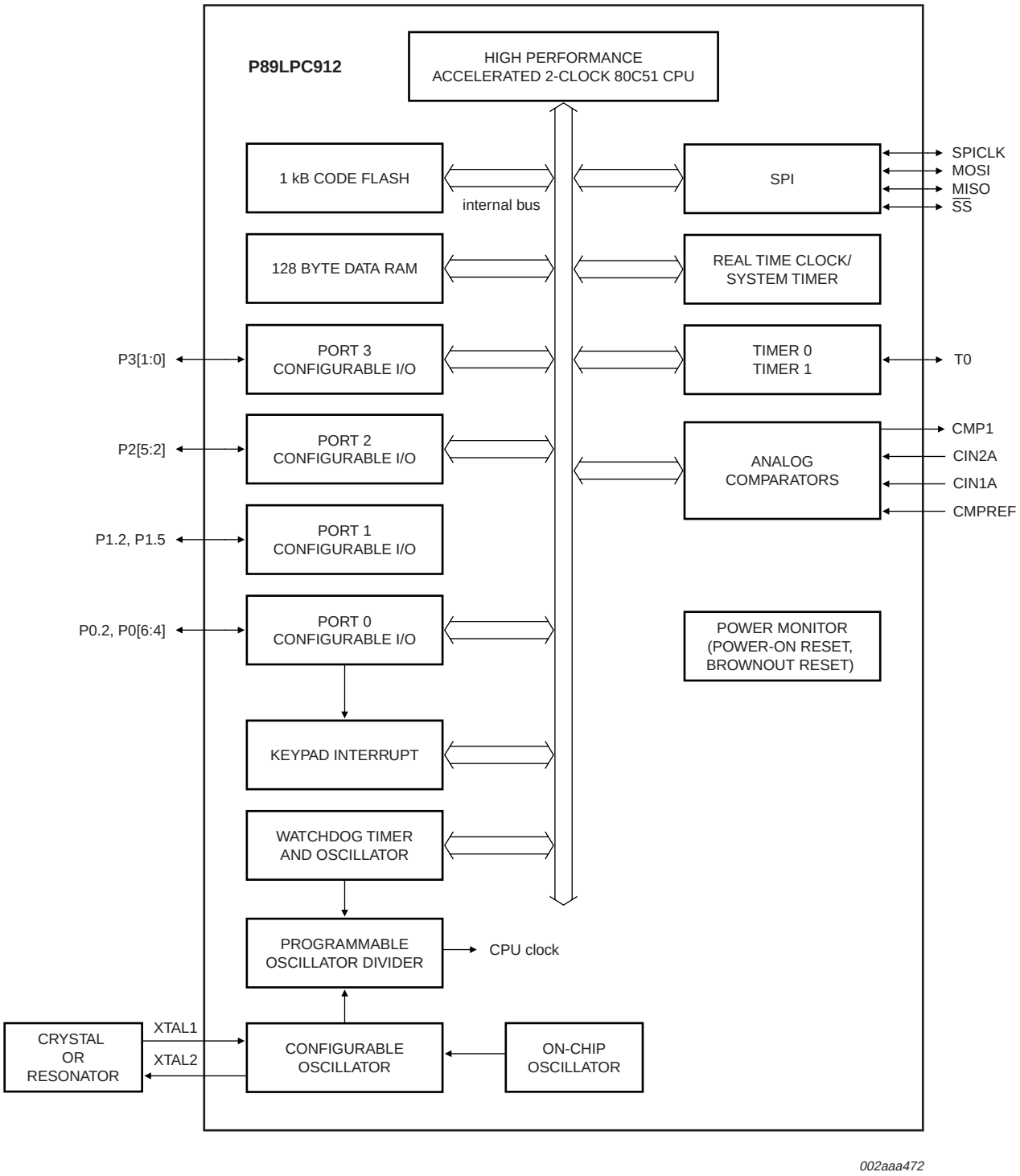

Fig 1. P89LPC912 block diagram

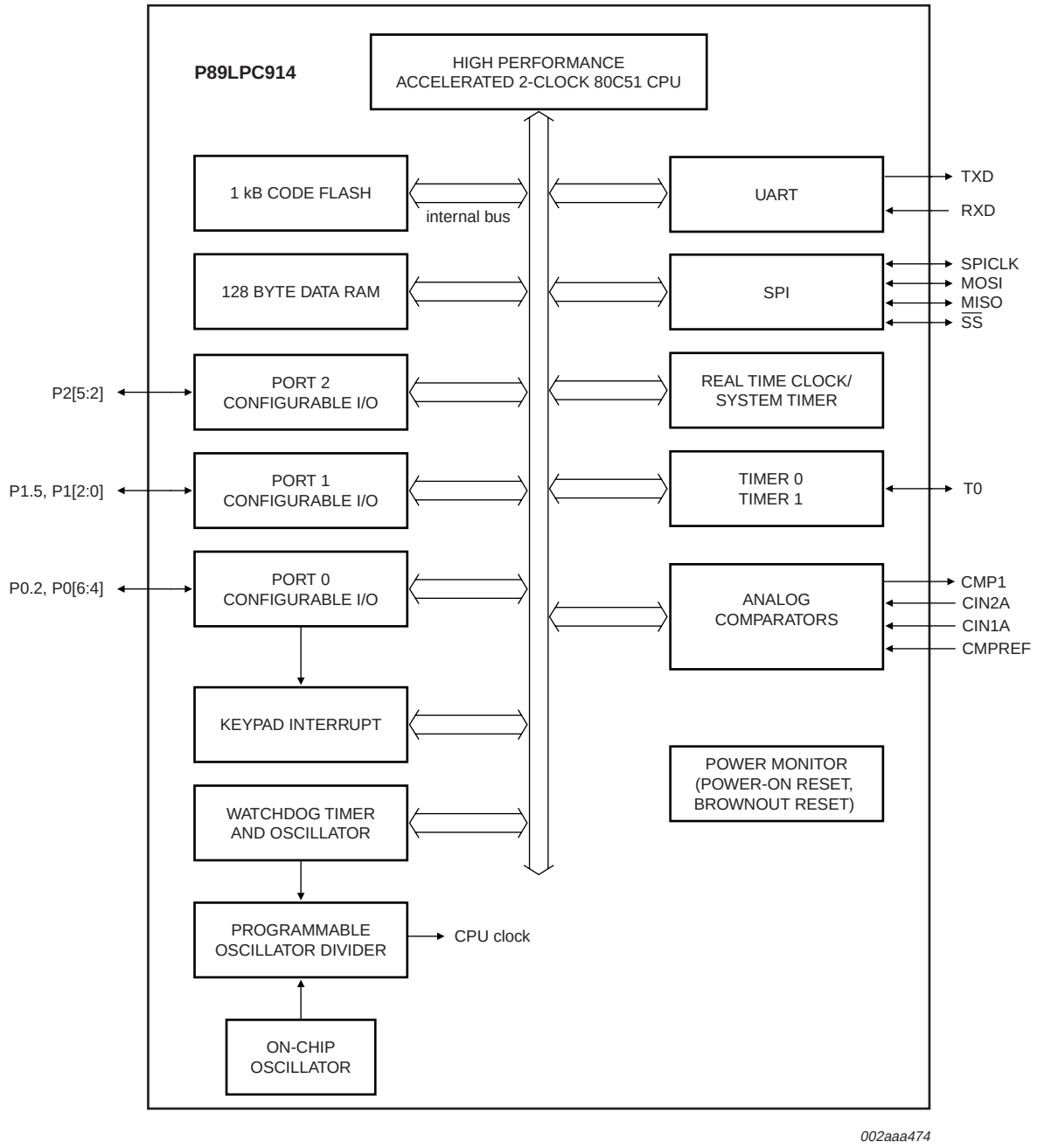

Fig 3. P89LPC914 block diagram

Table 4. P89LPC912 pin description *...continued*

Symbol	Pin	Type	Description
P2.2 to P2.5		I/O	**Port 2:** Port 2 is a 4-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	9	I/O	**P2.4 —** Port 2 bit 4.
		I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	8	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
P3.1/XTAL1	7	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 5. P89LPC913 pin description *...continued*

Symbol	Pin	Type	Description
P2.2, P2.3, P2.5		I/O	**Port 2:** Port 2 is a 3-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	8	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
P3.1/XTAL1	7	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 8. P89LPC913 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	-	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	-	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	87	86	85	84	83	82	81	80		
P0*	Port 0	80H		CMP1/ KB6	CMPREF / KB5	CIN1A/ KB4		CIN2A/ KB2			[1]	
		Bit address	97	96	95	94	93	92	91	90		
P1*	Port 1	90H			$\overline{\text{RST}}$				RXD	TXD	[1]	
		Bit address	A7	A6	A5	A4	A3	A2	A1	A0		
P2*	Port 2	A0H			SPICLK		MISO	MOSI			[1]	
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H							XTAL1	XTAL2	[1]	
P0M1	Port 0 output mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)			FF	1111 1111
P0M2	Port 0 output mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)			00	0000 0000
P1M1	Port 1 output mode 1	91H							(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H							(P1M2.1)	(P1M2.0)	00[1]	00x0 xx00
P2M1	Port 2 output mode 1	A4H			(P2M1.5)		(P2M1.3)	(P2M1.2)			FF	1111 1111
P2M2	Port 2 output mode 2	A5H			(P2M2.5)		(P2M2.3)	(P2M2.2)			00	0000 0000
P3M1	Port 3 output mode 1	B1H							(P3M1.1)	(P3M1.0)	03[1]	xxxx xx11
P3M2	Port 3 output mode 2	B2H							(P3M2.1)	(P3M2.0)	00[1]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	-	SPPD	SPD	-	00[1]	0000 0000

Table 8. P89LPC913 Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any of them is written if BRGEN = 1, result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC912 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

Table 9. P89LPC914 Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	011x xx00
RTCH	Real-time clock register high	D2H									00[6]	0000 0000
RTCL	Real-time clock register low	D3H									00[6]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial port data buffer register	99H									xx	xxxx xxxx
		Bit address	9F	9E	9D	9C	9B	9A	99	98		
SCON	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	-	-	-	-	T0M2	00	xxx0 xxx0
		Bit address	8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	-	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	

8.3.6 Clock output (P89LPC912, P89LPC913)

The P89LPC912 supports a user selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on X1) and if the Real-Time clock is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC912. This output is enabled by the ENCLK bit in the TRIM register. The frequency of this clock output is ½ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

8.4 On-chip RC oscillator option

The P89LPC912/913/914 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz, ± 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies.

8.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

8.6 External clock input option (P89LPC912, P89LPC913)

In this configuration, the processor clock is derived from an external source driving the XTAL1/P3.1 pin. The rate may be from 0 Hz up to 12 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed, V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

- DATA

  128 B of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC912/913/914 has 1 kB of on-chip Code memory.

8.11 Interrupts

The P89LPC912/913/914 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources.

The P89LPC912 supports 7 interrupt sources: timers 0 and 1, brownout detect, Watchdog/Real-Time clock, keyboard, comparators 1 and 2, and SPI.

The P89LPC913 and P89LPC914 devices support 10 interrupt sources: timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, Watchdog/Real-Time clock, keyboard, comparators 1 and 2, and SPI.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC912/913/914 has a Keypad Interrupt function. This can be used as an external interrupt input.

If enabled when the P89LPC912/913/914 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 “Power reduction modes” for details.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6 (P89LPC912, P89LPC914)

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.16.6 Timer overflow toggle output (P89LPC912, P89LPC914)

Timers 0 can be configured to automatically toggle the T0 output whenever a timer overflow occurs. The same device pins that are used for the T0 count input is also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.17 RTC/system timer

The P89LPC912/913/914 devices have a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered-down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set.

On the P89LPC914 the clock source for this counter is the CPU clock (CCLK). On the P89LPC912 and P89LPC913 devices, the clock source for this counter can either be the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source.

Only power-on reset will reset the RTC and its associated SFRs to the default state.

8.18 UART (P89LPC913, P89LPC914)

The P89LPC913 and P89LPC914 devices have an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC913 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CCLK/32 or CCLK/16.

8.18.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

8.18.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device.

8.18.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

8.18.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TX interrupt is generated when the double buffer is ready to receive new data.

8.18.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TX interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

8.19 Serial Peripheral Interface (SPI)

P89LPC912/913/914 provides another high-speed serial communication interface—the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 4.5 Mbit/s can be supported in Master mode or 3 Mbit/s in Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

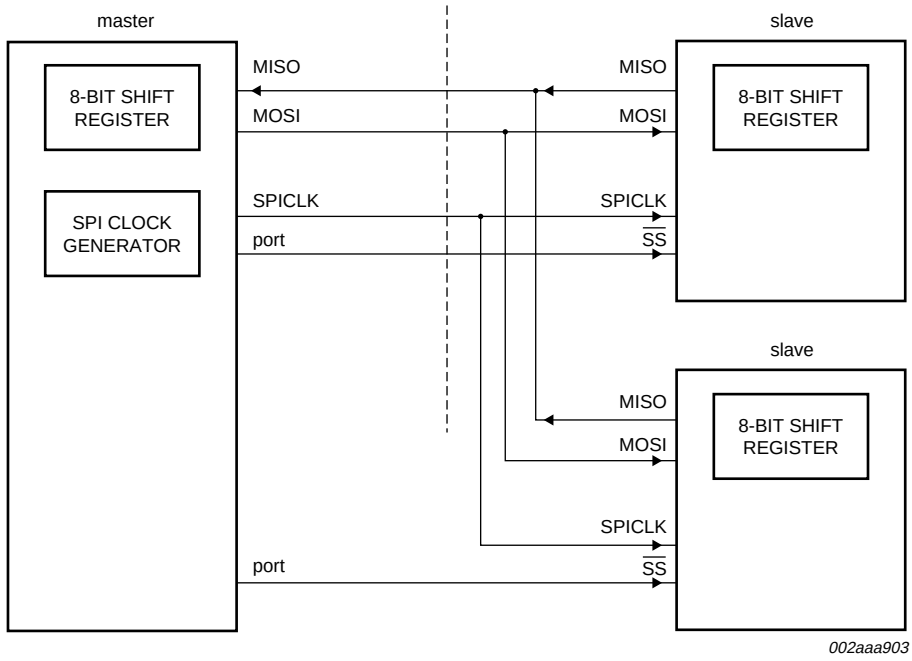

Fig 19. SPI single master multiple slaves configuration

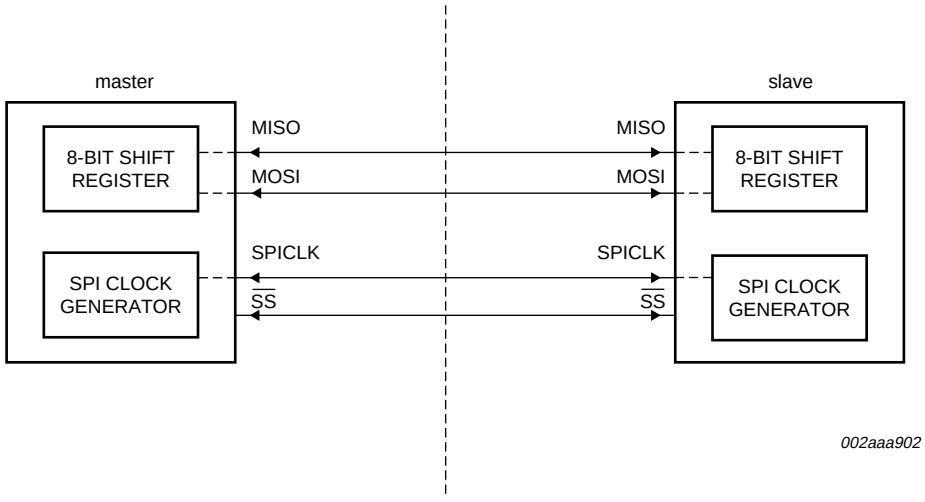

Fig 20. SPI dual device configuration, where either can be a master or a slave

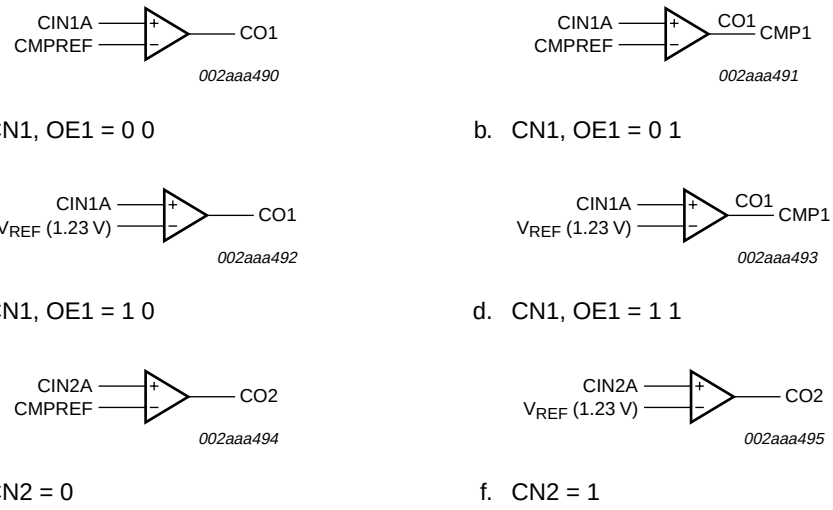

Fig 22. Comparator configurations

8.23 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.24 Keypad interrupt

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

8.27.4 Flash programming and erasing

Different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP-Lite) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock- serial data interface using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire 1 kB of user code space.

8.27.5 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC912/913/914 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector (with V_{DD}, V_{SS}, $\overline{RST}$, clock, and data signals) needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC912/913/914 *User manual*.

8.27.6 In-application programming (IAP-Lite)

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP-Lite facility consists of internal hardware resources to facilitate programming and erasing. The NXP In-Application Programming Lite has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC912/913/914 *User manual*.

8.27.7 Using flash as data storage

The flash code memory array of this device supports **individual** byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.27.8 User configuration bytes

Some user-configurable features of the P89LPC912/913/914 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC912/913/914 *User manual* for additional details.

8.27.9 User sector security bytes

There are four User Sector Security Bytes, each corresponding to one sector. Please see the P89LPC912/913/914 *User manual* for additional details.

10. Static characteristics

Table 13. Static characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current						
	P89LPC912, P89LPC913	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	7	13	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	11	16	mA
	P89LPC914	V_{DD} = 3.6 V; f_{osc} = 7.373 MHz	[3]	-	4	8	mA
$I_{DD(idle)}$	Idle mode supply current						
	P89LPC912, P89LPC913	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	1.5	5.6	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	4	6	mA
	P89LPC914	V_{DD} = 3.6 V; f_{osc} = 7.373 MHz	[3]	-	1	3	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.6 V	[2][3]	-	-	70	µA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.6 V	[2][3]	-	0.5	5	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{DDR}	data retention supply voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; all ports		-	0.6	1.0	V
		I_{OL} = 10 mA; all ports		-	0.3	0.5	V
		I_{OL} = 3.2 mA; all ports		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; all ports, push-pull mode		V_{DD} − 1.0	-	-	V
		I_{OH} = −3.2 mA; all ports, push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −20 µA; all ports, quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
C_{iss}	input capacitance		[4]	-	-	15	pF
I_{IL}	LOW-state input current	V_I = 0.4 V; all ports	[5]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}$ or V_{IH}; all ports	[6]	-	-	±1	µA
I_{THL}	HIGH-LOW transition current	V_I = 2.0 V at V_{DD} = 3.6 V; all ports	[7][8]	−30	-	−450	µA
$R_{RST\_N(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ

11. Dynamic characteristics

Table 14. Dynamic characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz; trimmed to ±1 % at T_{amb} = 25 °C	7.189	7.557	7.189	7.557	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	nominal f = 400 kHz	320	520	320	520	kHz
Crystal oscillator (P89LPC912, P89LPC913)							
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 25	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock (P89LPC912, P89LPC913)							
t_{CHCX}	clock HIGH time	see Figure 25	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 25	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 25	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 25	-	8	-	8	ns
Shift register (UART mode 0 - P89LPC913, P89LPC914)							
T_{XLXL}	serial port clock cycle time	see Figure 24	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge	see Figure 24	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge	see Figure 24	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge	see Figure 24	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge	see Figure 24	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	2.0 MHz (slave)		0	$^{CCLK}/_{6}$	0	2.0	MHz
	3.0 MHz (master)		-	$^{CCLK}/_{4}$	-	3.0	MHz
T_{SPICYC}	SPI cycle time	see Figure 26, 27, 28, 29					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns

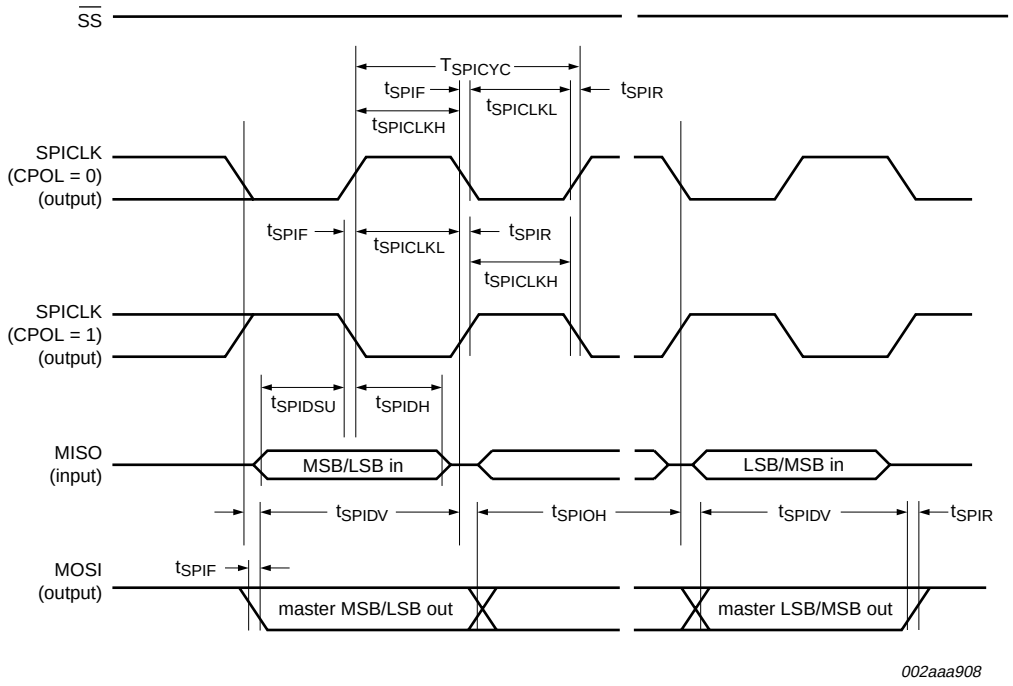

Fig 26. SPI master timing (CPHA = 0)

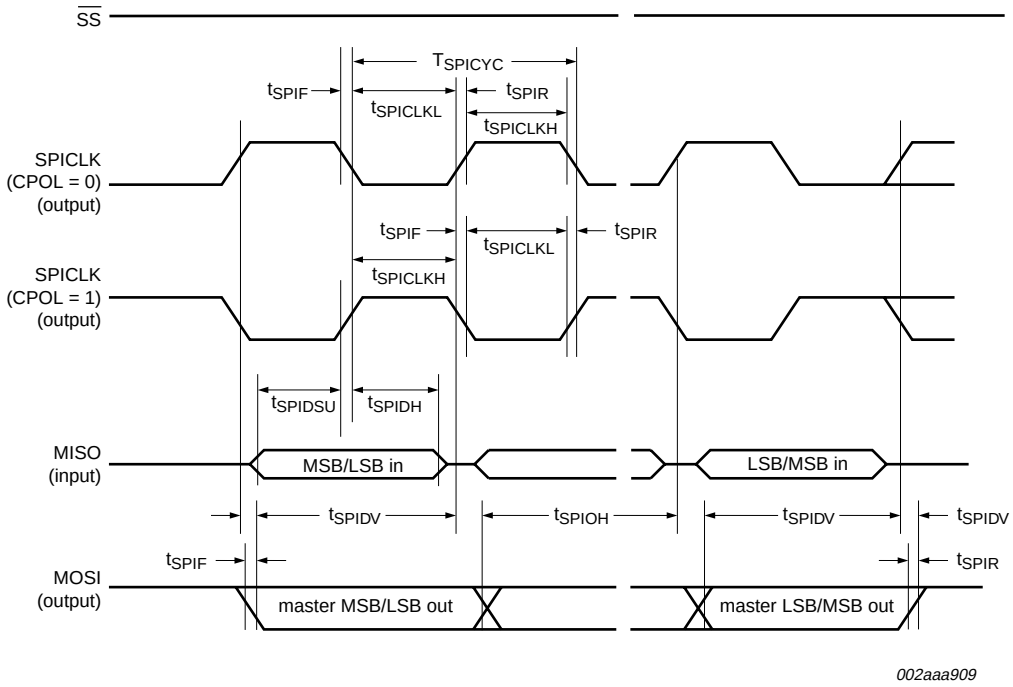

Fig 27. SPI master timing (CPHA = 1)

15. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC912_913_914_5	20070928	Product data sheet	-	P89LPC912_913_914_4
Modifications:	• Figure 10, 11 and 12: changed incorrect character font			
P89LPC912_913_914_4	20070830	Product data sheet	-	P89LPC912_913_914-03
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added P89LPC912HDH			
P89LPC912_913_914-03	20041217	Product data	-	P89LPC912_913_914-02
P89LPC912_913_914-02	20031212	Product data	01-A14930	P89LPC912_913_914-01
P89LPC912_913_914-01	20030711	Objective data	-	-

18. Contents

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