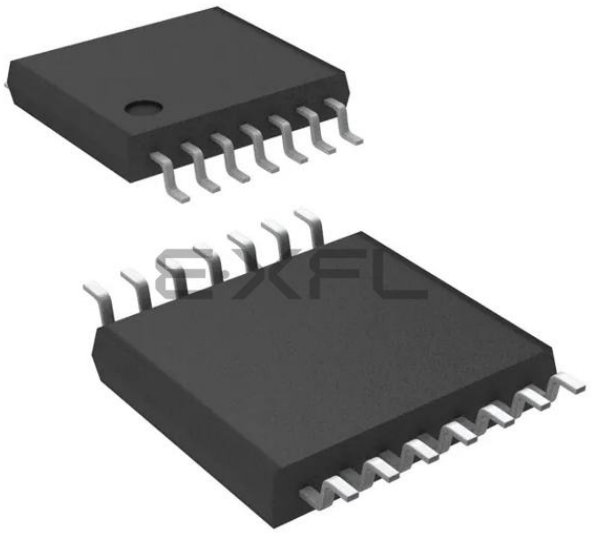

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	12MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	12
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc914fdh-129

- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz (P89LPC912, P89LPC913).
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open-drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC912/913/914 when internal reset option is selected.
- Four interrupt priority levels.
- Four keypad interrupt inputs.
- Second data pointer.
- Schmitt trigger port inputs.
- Emulation support.

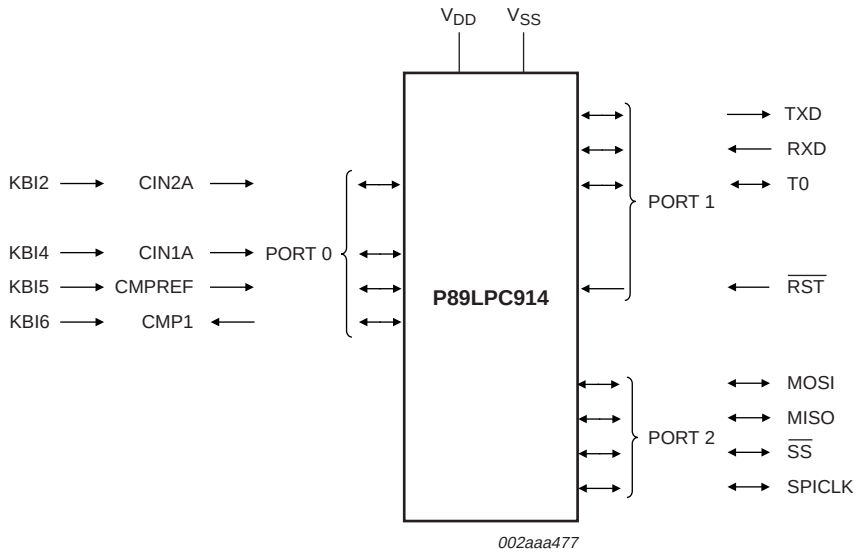


Fig 6. P89LPC914 functional diagram

Table 5. P89LPC913 pin description

Symbol	Pin	Type	Description
P0.2, P0.4 to P0.6		I/O	**Port 0:** Port 0 is a 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.2/CIN2A/ KBI2	13	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
P0.4/CIN1A/ KBI4	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
P0.5/CMPREF/ KBI5	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	5	I/O	**P0.6 —** Port 0 bit 6.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
P1.0, P1.1, P1.5		I/O (P1.0, P1.1); I (P1.5)	**Port 1:** Port 1 is a 3-bit I/O port with a user-configurable output type, except for P1.5 noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	9	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	6	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for the serial port.
P1.5/$\overline{\text{RST}}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

Table 5. P89LPC913 pin description *...continued*

Symbol	Pin	Type	Description
P2.2, P2.3, P2.5		I/O	**Port 2:** Port 2 is a 3-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	8	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
P3.1/XTAL1	7	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

8. Functional description

Remark: Please refer to the P89LPC912/913/914 *User manual* for a more detailed functional description.

8.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 9. P89LPC914 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		**E7**	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**	**E0**		
ACC*	Accumulator	E0H									00	0000 0000
AUXR1	Auxiliary function register	A2H	-	EBRR	-	ENT0	SRST	0	-	DPS	00[1]	0000 00x0
	Bit address		**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator rate low	BEH									00	0000 0000
BRGR1[2]	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[6]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H	-	-	-	-	-	-			00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	0000 0000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	-	00[1]	00x0 0000

- DATA

  128 B of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC912/913/914 has 1 kB of on-chip Code memory.

8.11 Interrupts

The P89LPC912/913/914 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources.

The P89LPC912 supports 7 interrupt sources: timers 0 and 1, brownout detect, Watchdog/Real-Time clock, keyboard, comparators 1 and 2, and SPI.

The P89LPC913 and P89LPC914 devices support 10 interrupt sources: timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, Watchdog/Real-Time clock, keyboard, comparators 1 and 2, and SPI.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC912/913/914 has a Keypad Interrupt function. This can be used as an external interrupt input.

If enabled when the P89LPC912/913/914 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 “Power reduction modes” for details.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.14.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC912/913/914 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM data retention voltage V_{DDR}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators (note that comparators can be powered-down separately), and RTC/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled.

8.14.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

8.15 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1. This option must be used for an oscillator frequency above 12 MHz.)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset (P89LPC913, P89LPC914).

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.16 Timers/counters 0 and 1

The P89LPC912/913/914 devices have two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. An option to automatically toggle the T0 pin upon timer overflow has been added (P89LPC912, P89LPC914). In the ‘Timer’ function, the register is incremented every machine cycle. In the ‘Counter’ function, the register of Timer 0 is incremented in response to a 1-to-0 transition at its external input pin, T0. This external input is sampled once very machine cycle.

Timer 0 has four operating modes (modes 0, 1, 2, and 3) on the P89LPC913).

Timer 0 has five operating modes (modes 0, 1, 2, 3, and 6 on the P89LPC912 and P89LPC914.

Timer 1 has four operating modes (modes 0, 1, 2, and 3) on all devices. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different.

8.16.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.16.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6 (P89LPC912, P89LPC914)

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.16.6 Timer overflow toggle output (P89LPC912, P89LPC914)

Timers 0 can be configured to automatically toggle the T0 output whenever a timer overflow occurs. The same device pins that are used for the T0 count input is also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.17 RTC/system timer

The P89LPC912/913/914 devices have a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered-down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set.

On the P89LPC914 the clock source for this counter is the CPU clock (CCLK). On the P89LPC912 and P89LPC913 devices, the clock source for this counter can either be the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source.

Only power-on reset will reset the RTC and its associated SFRs to the default state.

8.18 UART (P89LPC913, P89LPC914)

The P89LPC913 and P89LPC914 devices have an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC913 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CCLK/32 or CCLK/16.

8.18.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

8.18.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.18.5 "Baud rate generator and selection").

8.18.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $1/16$ or $1/32$ of the CCLK frequency, as determined by the SMOD1 bit in PCON.

8.18.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in section Section 8.18.5 "Baud rate generator and selection").

8.18.5 Baud rate generator and selection

The P89LPC913 and P89LPC914 devices have an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 15). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses CCLK.

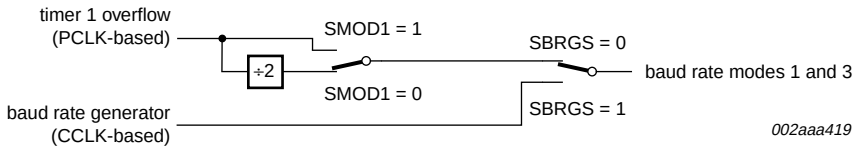


Fig 15. Baud rate sources for UART (Modes 1, 3)

8.18.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7, respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON[7:6]) are set up when SMOD0 is logic 0.

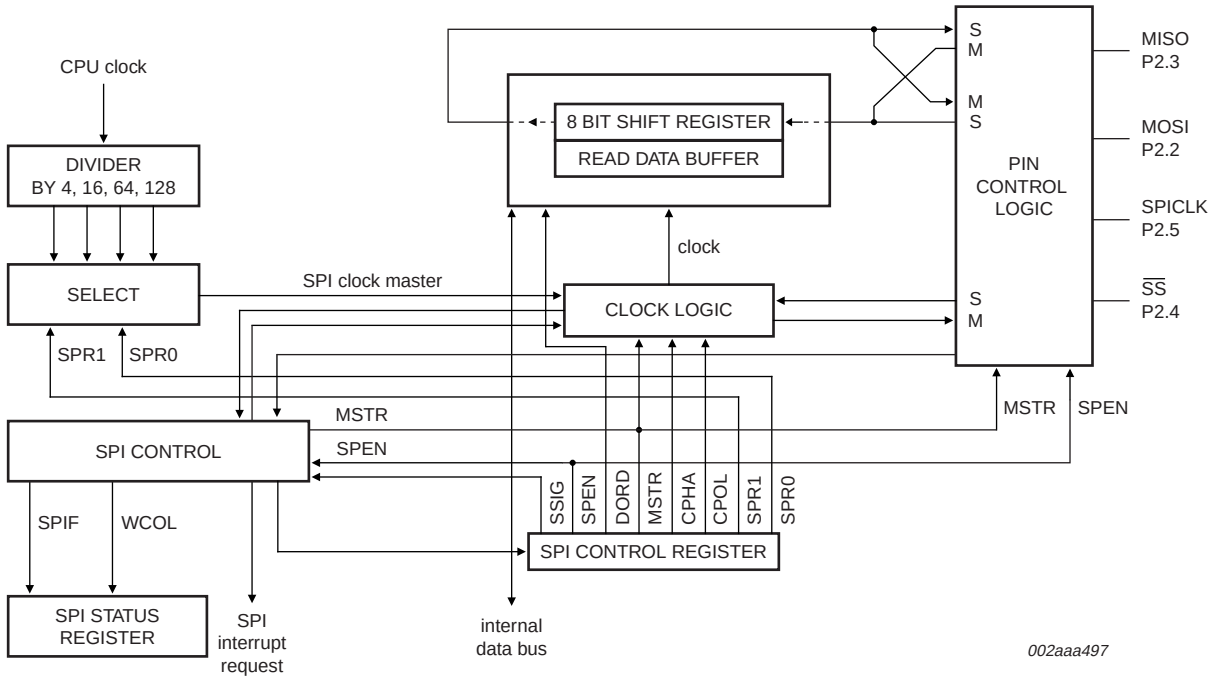


Fig 16. SPI block diagram (P89LPC912, P89LPC914)

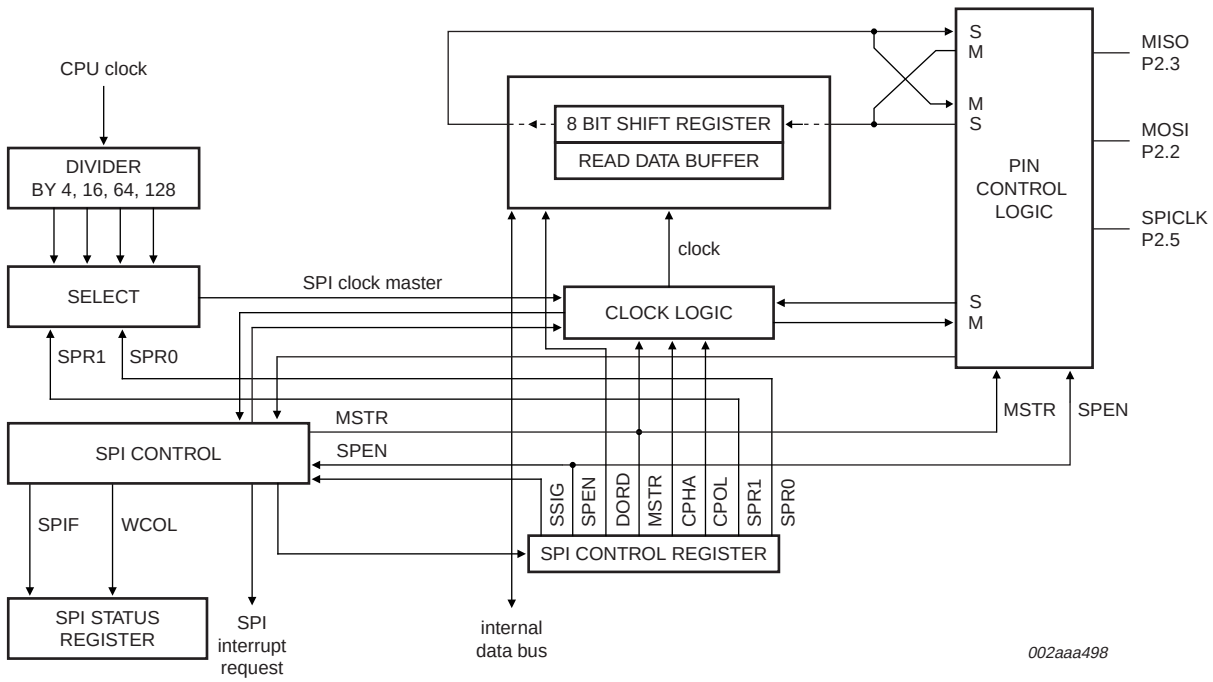


Fig 17. SPI block diagram (P89LPC913)

The SPI interface has four pins: SPICLK, MOSI, MISO, and $\overline{SS}$:

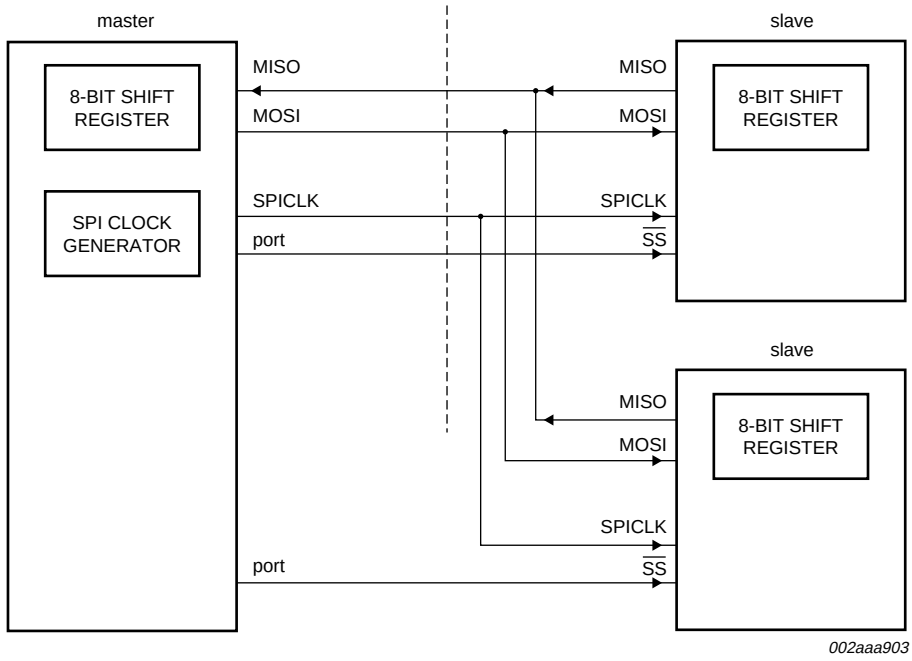


Fig 19. SPI single master multiple slaves configuration

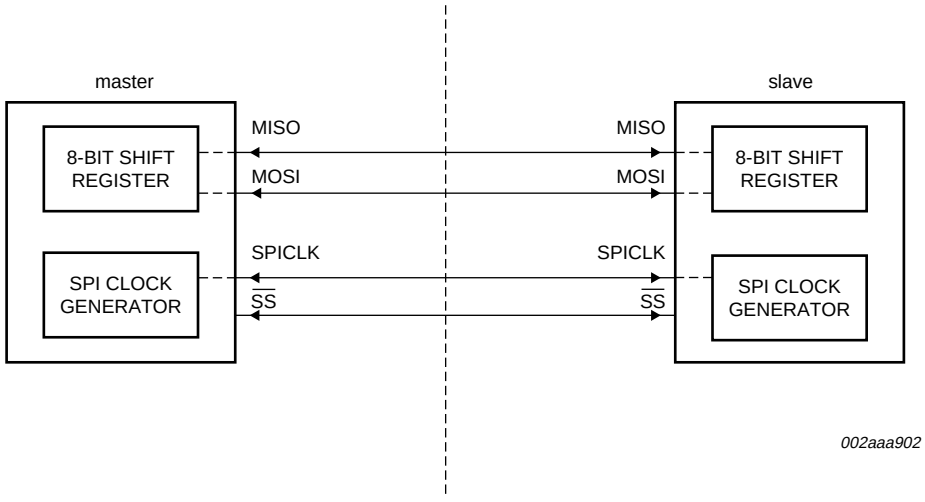


Fig 20. SPI dual device configuration, where either can be a master or a slave

8.20 Analog comparators

Two analog comparators are provided on the P89LPC912/913/914. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes. Comparator 1 may be output to a port pin.

The overall connections to both comparators are shown in Figure 21. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

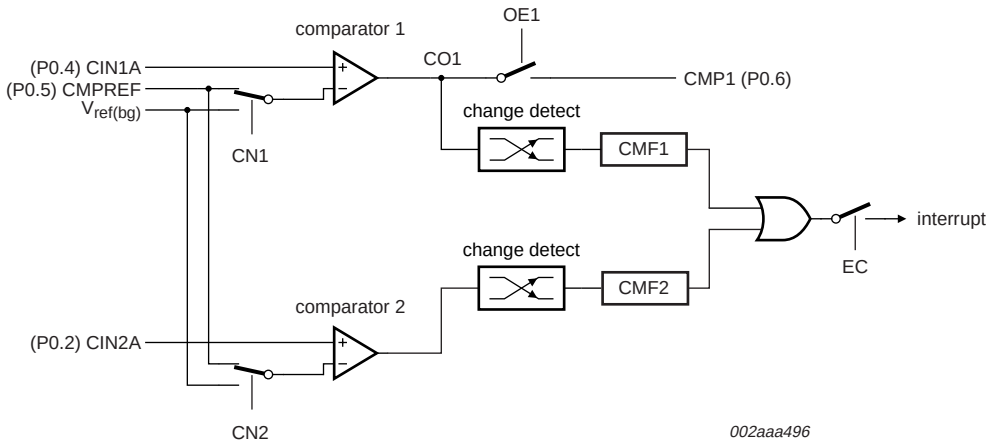


Fig 21. Comparator input and output connections

8.21 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is 1.23 V ± 3 %.

8.22 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

Possible comparator configurations are shown in Figure 22.

8.27.4 Flash programming and erasing

Different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP-Lite) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock- serial data interface using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire 1 kB of user code space.

8.27.5 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC912/913/914 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector (with V_{DD}, V_{SS}, $\overline{RST}$, clock, and data signals) needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC912/913/914 *User manual*.

8.27.6 In-application programming (IAP-Lite)

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP-Lite facility consists of internal hardware resources to facilitate programming and erasing. The NXP In-Application Programming Lite has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC912/913/914 *User manual*.

8.27.7 Using flash as data storage

The flash code memory array of this device supports **individual** byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.27.8 User configuration bytes

Some user-configurable features of the P89LPC912/913/914 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC912/913/914 *User manual* for additional details.

8.27.9 User sector security bytes

There are four User Sector Security Bytes, each corresponding to one sector. Please see the P89LPC912/913/914 *User manual* for additional details.

Table 13. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0	2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage		1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, V_{DD} = 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$ and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer (P89LPC912, P89LPC913).

[3] The $I_{DD(oper)}$, $I_{DD(idle)}$ and $I_{DD(pd)}$ specifications are measured with the following functions disabled: comparators, brownout detect, and watchdog timer (P89LPC914).

[4] Pin capacitance is characterized but not tested.

[5] Measured with port in quasi-bidirectional mode.

[6] Measured with port in high-impedance mode.

[7] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups)

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 15. Dynamic characteristics (P89LPC912, P89LPC913)

V_{DD} = 3.0 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions		Variable clock		f_{osc} = 18 MHz		Unit
				Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 °C		7.189	7.557	7.189	7.557	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	nominal f = 400 kHz		320	520	320	520	kHz
Crystal oscillator								
f_{osc}	oscillator frequency		[2]	0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 25		55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency			0	8	-	-	MHz
Glitch filter								
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin		-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin		125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock								
t_{CHCX}	clock HIGH time	see Figure 25		22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 25		22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 25		-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 25		-	5	-	5	ns
SPI interface								
f_{SPI}	SPI operating frequency							
	3.0 MHz (slave)			0	$^{CCLK}/_{6}$	0	3	MHz
	4.5 MHz (master)			-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 26, 27, 28, 29						
	slave			$^{6}/_{CCLK}$	-	333	-	ns
	master			$^{4}/_{CCLK}$	-	222	-	ns

12. Other characteristics

12.1 Comparator electrical characteristics

Table 16. Comparator electrical characteristics

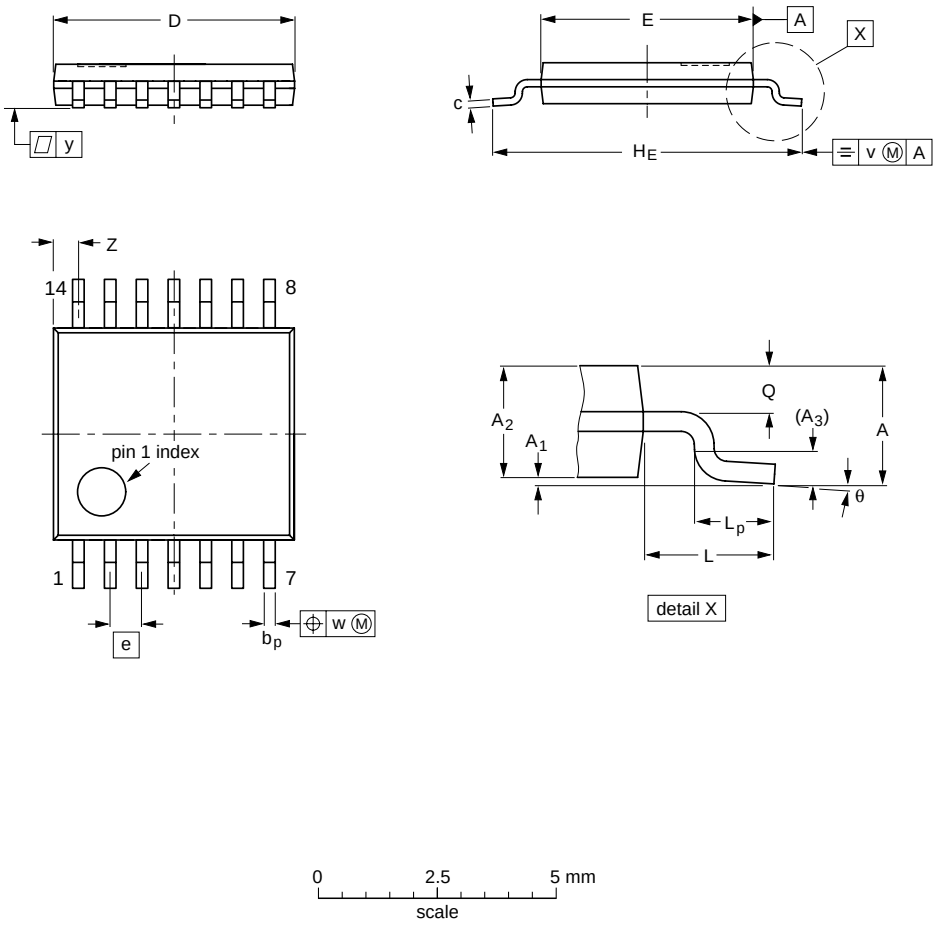
V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±10	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	µs
I_{LI}	input leakage current	0 V < V_I < V_{DD}	-	-	±1	µA

[1] This parameter is characterized, but not tested in production.

13. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 30. Package outline SOT402-1 (TSSOP14)

15. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC912_913_914_5	20070928	Product data sheet	-	P89LPC912_913_914_4
Modifications:	• Figure 10, 11 and 12: changed incorrect character font			
P89LPC912_913_914_4	20070830	Product data sheet	-	P89LPC912_913_914-03
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added P89LPC912HDH			
P89LPC912_913_914-03	20041217	Product data	-	P89LPC912_913_914-02
P89LPC912_913_914-02	20031212	Product data	01-A14930	P89LPC912_913_914-01
P89LPC912_913_914-01	20030711	Objective data	-	-