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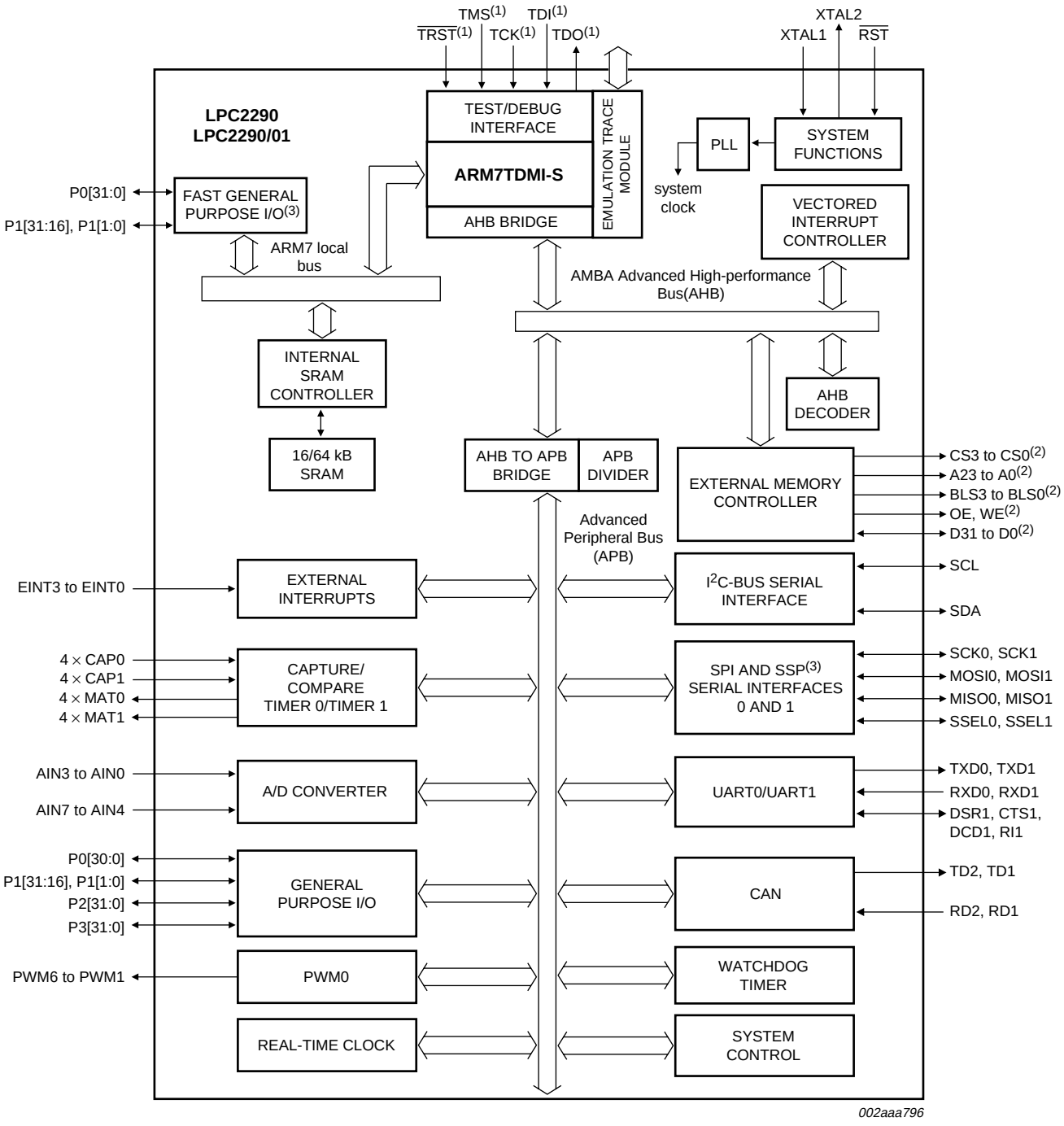
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2290fbd144-01-5

4. Block diagram



(1) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(2) Pins shared with GPIO.

(3) Available in LPC2290/01 only.

Fig 1. Block diagram

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0.0/TXD0/ PWM1	42[1]	I/O	**P0.0 —** General purpose digital input/output pin.
		O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	49[2]	I/O	**P0.1 —** General purpose digital input/output pin.
		I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input
P0.2/SCL/ CAP0.0	50[3]	I/O	**P0.2 —** General purpose digital input/output pin.
		I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA/ MAT0.0/EINT1	58[3]	I/O	**P0.3 —** General purpose digital input/output pin.
		I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0.4/SCK0/ CAP0.1	59[1]	I/O	**P0.4 —** General purpose digital input/output pin.
		I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
P0.5/MISO0/ MAT0.1	61[1]	I/O	**P0.5 —** General purpose digital input/output pin.
		I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.6/MOSI0/ CAP0.2	68[1]	I/O	**P0.6 —** General purpose digital input/output pin.
		I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.7/SSEL0/ PWM2/EINT2	69[2]	I/O	**P0.7 —** General purpose digital input/output pin.
		I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0.8/TXD1/ PWM4	75[1]	I/O	**P0.8 —** General purpose digital input/output pin.
		O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P1.0/CS0	91[5]	I/O	**P1.0 —** General purpose digital input/output pin.
		O	**CS0 —** LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1.1/OE	90[5]	I/O	**P1.1 —** General purpose digital input/output pin.
		O	**OE —** LOW-active Output Enable signal.
P1.16/ TRACEPKT0	34[5]	I/O	**P1.16 —** General purpose digital input/output pin.
		O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17/ TRACEPKT1	24[5]	I/O	**P1.17 —** General purpose digital input/output pin.
		O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18/ TRACEPKT2	15[5]	I/O	**P1.18 —** General purpose digital input/output pin.
		O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19/ TRACEPKT3	7[5]	I/O	**P1.19 —** General purpose digital input/output pin.
		O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20/ TRACESYNC	102[5]	I/O	**P1.20 —** General purpose digital input/output pin.
		O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1.21/ PIPESTAT0	95[5]	I/O	**P1.21 —** General purpose digital input/output pin.
		O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22/ PIPESTAT1	86[5]	I/O	**P1.22 —** General purpose digital input/output pin.
		O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23/ PIPESTAT2	82[5]	I/O	**P1.23 —** General purpose digital input/output pin.
		O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1.24/ TRACECLK	70[5]	I/O	**P1.24 —** General purpose digital input/output pin.
		O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P1.25/EXTIN0	60[5]	I/O	**P1.25 —** General purpose digital input/output pin.
		I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1.26/RTCK	52[5]	I/O	**P1.26 —** General purpose digital input/output pin.
		I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1.27/TDO	144[5]	I/O	**P1.27 —** General purpose digital input/output pin.
		O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	140[5]	I/O	**P1.28 —** General purpose digital input/output pin.
		I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	126[5]	I/O	**P1.29 —** General purpose digital input/output pin.
		I	**TCK —** Test Clock for JTAG interface.
P1.30/TMS	113[5]	I/O	**P1.30 —** General purpose digital input/output pin.
		I	**TMS —** Test Mode Select for JTAG interface.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P3.0/A0	89[5]	I/O	**P3.0 —** General purpose digital input/output pin.
		O	**A0 —** External memory address line 0.
P3.1/A1	88[5]	I/O	**P3.1 —** General purpose digital input/output pin.
		O	**A1 —** External memory address line 1.
P3.2/A2	87[5]	I/O	**P3.2 —** General purpose digital input/output pin.
		O	**A2 —** External memory address line 2.
P3.3/A3	81[5]	I/O	**P3.3 —** General purpose digital input/output pin.
		O	**A3 —** External memory address line 3.
P3.4/A4	80[5]	I/O	**P3.4 —** General purpose digital input/output pin.
		O	**A4 —** External memory address line 4.
P3.5/A5	74[5]	I/O	**P3.5 —** General purpose digital input/output pin.
		O	**A5 —** External memory address line 5.
P3.6/A6	73[5]	I/O	**P3.6 —** General purpose digital input/output pin.
		O	**A6 —** External memory address line 6.
P3.7/A7	72[5]	I/O	**P3.7 —** General purpose digital input/output pin.
		O	**A7 —** External memory address line 7.
P3.8/A8	71[5]	I/O	**P3.8 —** General purpose digital input/output pin.
		O	**A8 —** External memory address line 8.
P3.9/A9	66[5]	I/O	**P3.9 —** General purpose digital input/output pin.
		O	**A9 —** External memory address line 9.
P3.10/A10	65[5]	I/O	**P3.10 —** General purpose digital input/output pin.
		O	**A10 —** External memory address line 10.
P3.11/A11	64[5]	I/O	**P3.11 —** General purpose digital input/output pin.
		O	**A11 —** External memory address line 11.
P3.12/A12	63[5]	I/O	**P3.12 —** General purpose digital input/output pin.
		O	**A12 —** External memory address line 12.
P3.13/A13	62[5]	I/O	**P3.13 —** General purpose digital input/output pin.
		O	**A13 —** External memory address line 13.
P3.14/A14	56[5]	I/O	**P3.14 —** General purpose digital input/output pin.
		O	**A14 —** External memory address line 14.
P3.15/A15	55[5]	I/O	**P3.15 —** General purpose digital input/output pin.
		O	**A15 —** External memory address line 15.
P3.16/A16	53[5]	I/O	**P3.16 —** General purpose digital input/output pin.
		O	**A16 —** External memory address line 16.
P3.17/A17	48[5]	I/O	**P3.17 —** General purpose digital input/output pin.
		O	**A17 —** External memory address line 17.
P3.18/A18	47[5]	I/O	**P3.18 —** General purpose digital input/output pin.
		O	**A18 —** External memory address line 18.
P3.19/A19	46[5]	I/O	**P3.19 —** General purpose digital input/output pin.
		O	**A19 —** External memory address line 19.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P3.20/A20	45[5]	I/O	**P3.20 —** General purpose digital input/output pin.
		O	**A20 —** External memory address line 20.
P3.21/A21	44[5]	I/O	**P3.21 —** General purpose digital input/output pin.
		O	**A21 —** External memory address line 21.
P3.22/A22	41[5]	I/O	**P3.22 —** General purpose digital input/output pin.
		O	**A22 —** External memory address line 22.
P3.23/A23/ XCLK	40[5]	I/O	**P3.23 —** General purpose digital input/output pin.
		I/O	**A23 —** External memory address line 23.
		O	**XCLK —** Clock output.
P3.24/CS3	36[5]	I/O	**P3.24 —** General purpose digital input/output pin.
		O	**CS3 —** LOW-active Chip Select 3 signal. (Bank 3 addresses range 0x8300 0000 to 0x83FF FFFF)
P3.25/CS2	35[5]	I/O	**P3.25 —** General purpose digital input/output pin.
		O	**CS2 —** LOW-active Chip Select 2 signal. (Bank 2 addresses range 0x8200 0000 to 0x82FF FFFF)
P3.26/CS1	30[5]	I/O	**P3.26 —** General purpose digital input/output pin.
		O	**CS1 —** LOW-active Chip Select 1 signal. (Bank 1 addresses range 0x8100 0000 to 0x81FF FFFF)
P3.27/WE	29[5]	I/O	**P3.27 —** General purpose digital input/output pin.
		O	**WE —** LOW-active Write enable signal.
P3.28/BLS3/ AIN7	28[2]	I/O	**P3.28 —** General purpose digital input/output pin.
		O	**BLS3 —** LOW-active Byte Lane Select signal (Bank 3).
		I	**AIN7 —** ADC, input 7. This analog input is always connected to its pin.
P3.29/BLS2/ AIN6	27[4]	I/O	**P3.29 —** General purpose digital input/output pin.
		O	**BLS2 —** LOW-active Byte Lane Select signal (Bank 2).
		I	**AIN6 —** ADC, input 6. This analog input is always connected to its pin.
P3.30/BLS1	97[4]	I/O	**P3.30 —** General purpose digital input/output pin.
		O	**BLS1 —** LOW-active Byte Lane Select signal (Bank 1).
P3.31/BLS0	96[4]	I/O	**P3.31 —** General purpose digital input/output pin.
		O	**BLS0 —** LOW-active Byte Lane Select signal (Bank 0).
TD1	22[5]	O	**TD1:** CAN1 transmitter output.
$\overline{\text{RESET}}$	135[6]	I	**External Reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	142[7]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	141[7]	O	Output from the oscillator amplifier.
V_{SS}	3, 9, 26, 38, 54, 67, 79, 93, 103, 107, 111, 128	I	**Ground:** 0 V reference.
V_{SSA}	139	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.

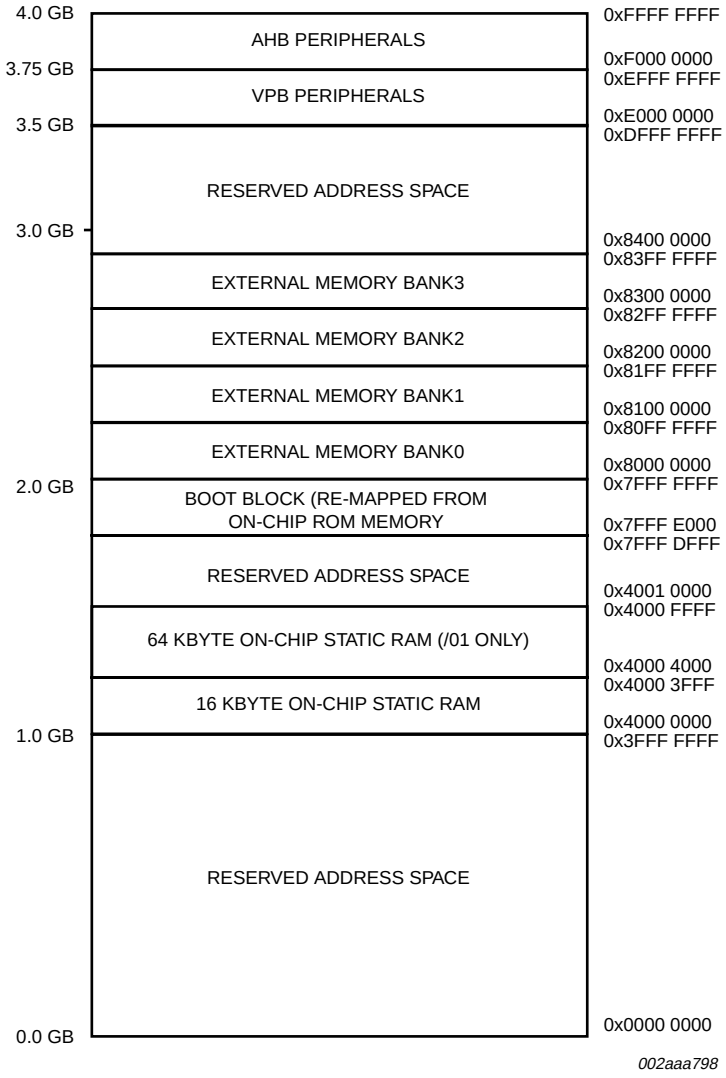


Fig 3. LPC2290 and LPC2290/01 memory map

6.4 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Table 4. Interrupt sources *...continued*

Block	Flag(s)	VIC channel #
SPI1/SSP	**Source: SPI1** SPI Interrupt Flag (SPIF), Mode Fault (MODF)	11
	Source: SSP (available in LPC2290/01 only)	
	TX FIFO at least half empty (TXRIS)	
	RX FIFO at least half full (RXRIS)	
	Receive Timeout condition (RTRIS)	
	Receive Overrun (RORRIS)	
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
A/D	ADC	18
CAN	1 ORed CAN Acceptance Filter	19
	CAN1 (TX int, RX int)	20, 21
	CAN2 (TX int, RX int)	22, 23

6.5 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.6 External memory controller

The external Static Memory Controller is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MB each with byte lane enable control) simultaneously. Each memory bank is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory, or some external I/O devices.

Each memory bank may be 8-bit, 16-bit, or 32-bit wide.

6.7 General purpose parallel I/O and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.7.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.

- All I/O default to inputs after reset.

6.7.2 Fast I/O features available in LPC2290/01 only

- Fast I/O registers are located on the ARM local bus for the fastest possible I/O timing.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Mask registers allow single instruction to set or clear any number of bits in one port.

6.8 10-bit ADC

The LPC2290 each contain a single 10-bit successive approximation ADC with eight multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

6.8.2 ADC features available in LPC2290/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.

6.9 CAN controllers and acceptance filter

The LPC2290 contains two CAN controllers. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

6.9.1 Features

- Data rates up to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with CAN specification 2.0B, ISO 11898-1.
- Global Acceptance Filter recognizes 11-bit and 29-bit RX identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identifiers.
- Full CAN messages can generate interrupts.

6.10 UARTs

The LPC2290 contains two UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.18 System control

6.18.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 30 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 “PLL” for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 µs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2290: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

6.19 Emulation and debugging

The LPC2290 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a coprocessor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

6.19.2 Embedded trace

Since the LPC2290 has significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2290 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

8. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)	internal rail		1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail		3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[2][3][4]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[5]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[5]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[5]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[5]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[6]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[6]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[7]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[8]	−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V	[7]	0	0	0	µA
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V, CCLK = 60 MHz, T_{amb} = 25 °C, code `while(1){}` executed from flash, no active peripherals		-	50	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V, T_{amb} = 25 °C,		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V, T_{amb} = 85 °C		-	110	500	µA
		$V_{DD(1V8)}$ = 1.8 V, T_{amb} = 125 °C		-	300	1000	µA

Table 7. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +125 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	±2	LSB
E_O	offset error	[1][5]	-	-	±3	LSB
E_G	gain error	[1][6]	-	-	±0.5	%
E_T	absolute error	[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

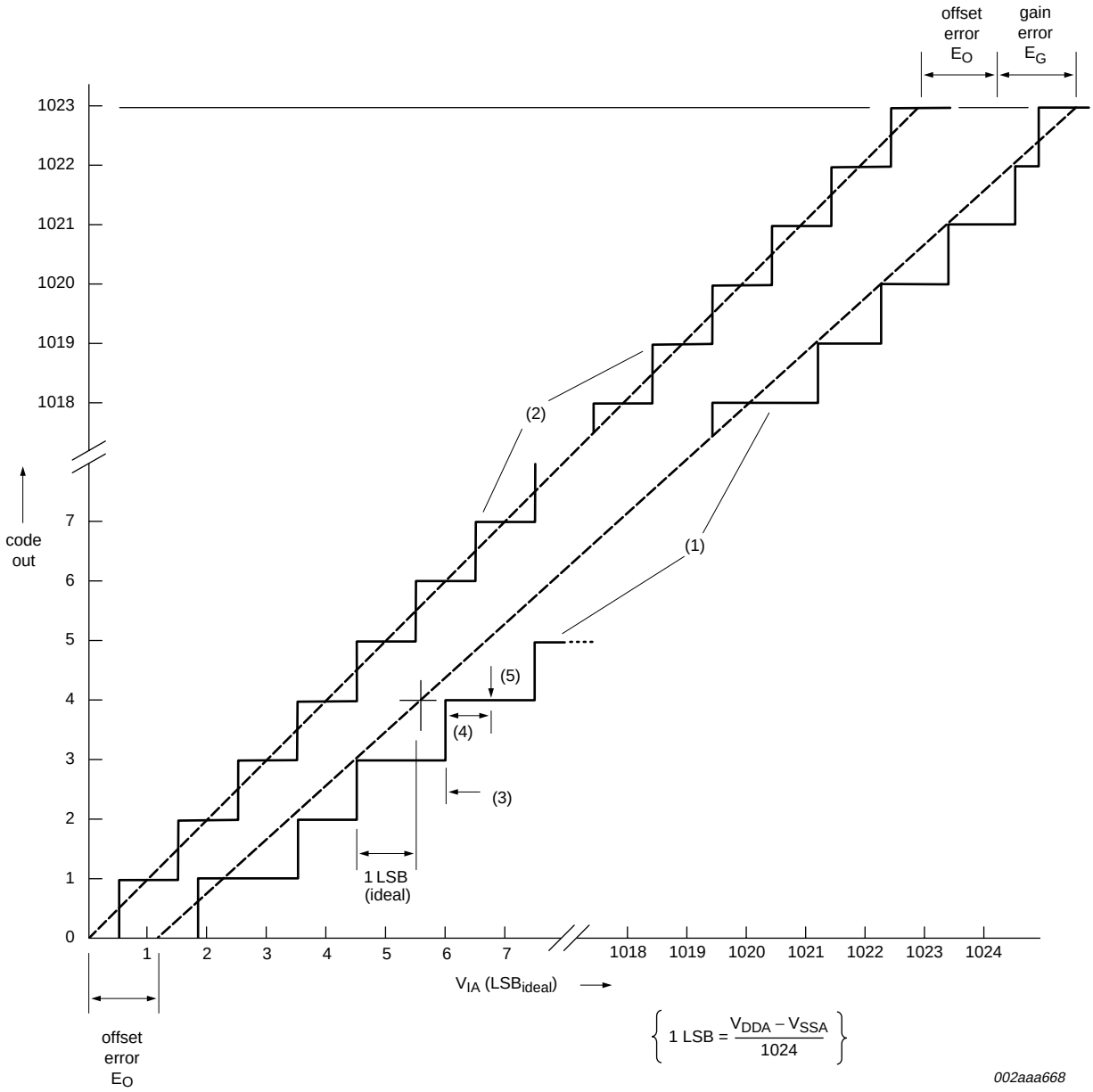
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 4.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 4.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 4.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 4.

[7] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 4.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 4. ADC characteristics

9. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = −40 °C to +125 °C; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	50	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	30	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
t_f	fall time	V_{IH} to V_{IL} [2]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

9.1 Timing

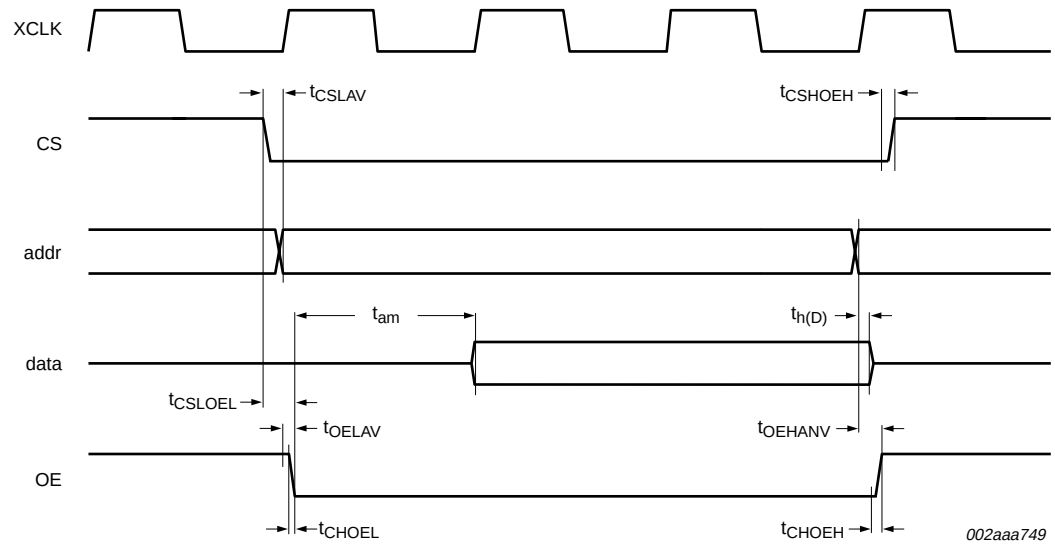


Fig 5. External memory read access

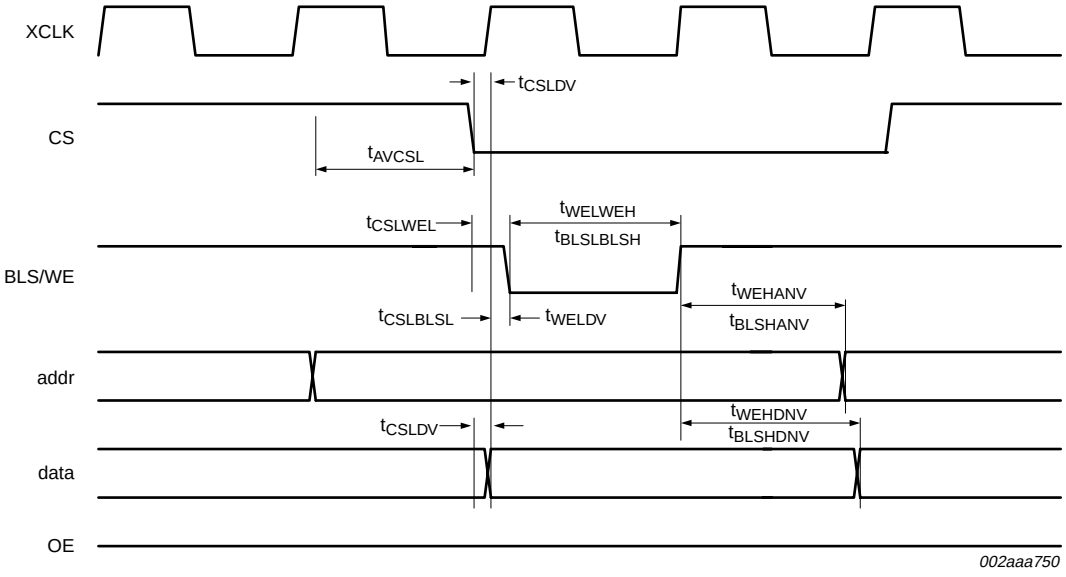


Fig 6. External memory write access

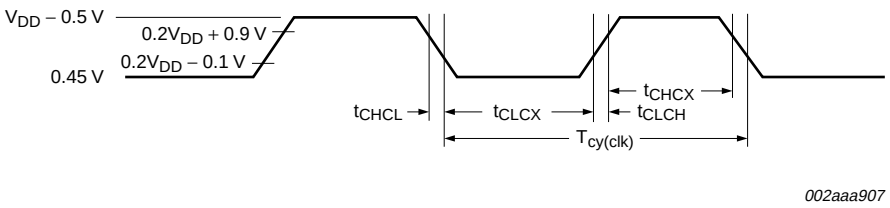
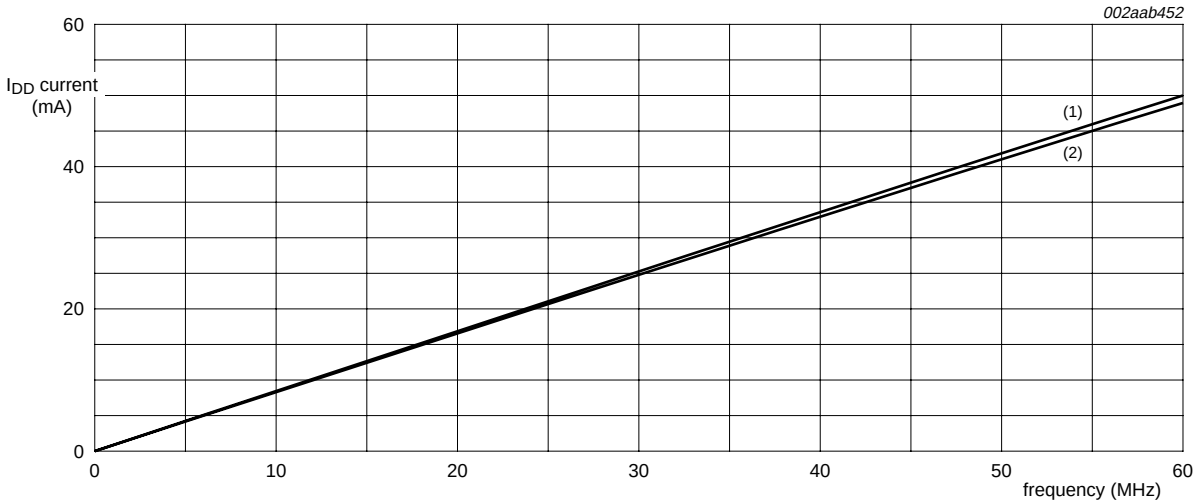


Fig 7. External clock timing

9.2 LPC2290 power consumption measurements

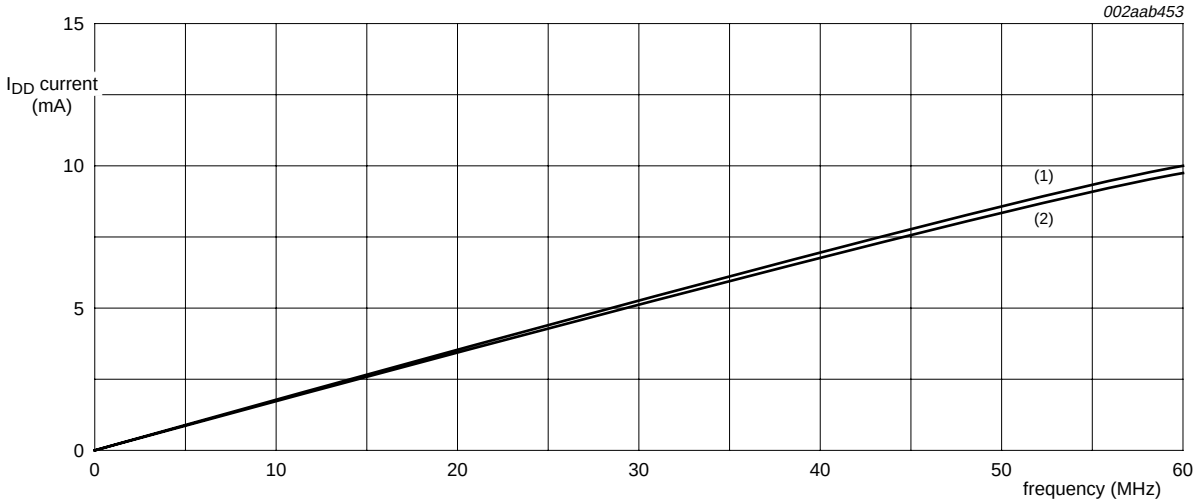


Test conditions: code executed from on-chip RAM; all peripherals are enabled in PCONP register; PCLK = $^{CCLK}/_{4}$.

(1) 1.8 V core at 25 °C (typical)

(2) 1.65 V core at 25 °C (typical)

Fig 8. LPC2290 $I_{DD(act)}$ measured at different frequencies (CCLK) and temperatures

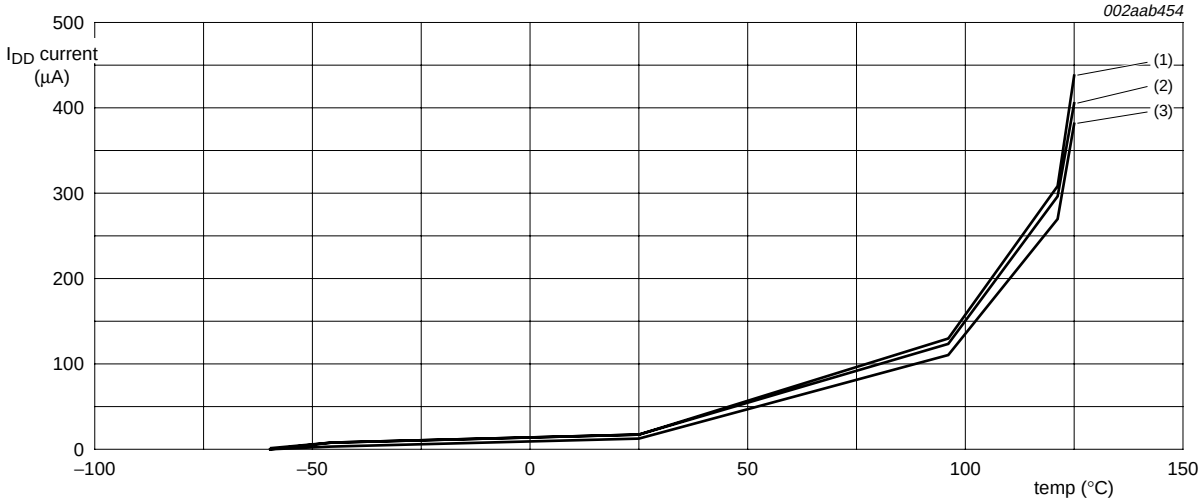


Test conditions: Idle mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register; PCLK = $^{CCLK}/_{4}$.

(1) 1.8 V core at 25 °C (typical)

(2) 1.65 V core at 25 °C (typical)

Fig 9. LPC2290 I_{DD} idle measured at different frequencies (CCLK) and temperatures



Test conditions: Power-down mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register.

(1) 1.95 V core

(2) 1.8 V core

(3) 1.65 V core

Fig 10. LPC2290 $I_{DD(pd)}$ measured at different temperatures

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	AMBA Peripheral Bus
CAN	Controller Area Network
CISC	Complex Instruction Set Computer
CPU	Central Processing Unit
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2290_3	20061116	Product data sheet	-	LPC2290-02
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • New features specific to the LPC2290/01 have been added throughout.			
LPC2290-02	20041223	Product data	-	LPC2290-01
LPC2290-01	20040209	Preliminary data	-	-

15. Contents

For more information, please visit: http://www.nxp.com
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Date of release: 16 November 2006
Document identifier: LPC2290_3