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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2290fbd144-551

Table 3. Pin description *Écontinued*

Symbol	Pin	Type	Description
P0.9/RXD1/ PWM6/EINT3	76[2]	I/O	P0.9 Ñ General purpose digital input/output pin.
		I	RXD1 Ñ Receiver input for UART1.
		O	PWM6 Ñ Pulse Width Modulator output 6.
		I	EINT3 Ñ External interrupt 3 input.
P0.10/RTS1/ CAP1.0	78[1]	I/O	P0.10 Ñ General purpose digital input/output pin.
		O	RTS1 Ñ Request to Send output for UART1.
		I	CAP1.0 Ñ Capture input for Timer 1, channel 0.
P0.11/CTS1/ CAP1.1	83[1]	I/O	P0.11 Ñ General purpose digital input/output pin.
		I	CTS1 Ñ Clear to Send input for UART1.
		I	CAP1.1 Ñ Capture input for Timer 1, channel 1.
P0.12/DSR1/ MAT1.0	84[1]	I/O	P0.12 Ñ General purpose digital input/output pin.
		I	DSR1 Ñ Data Set Ready input for UART1.
		O	MAT1.0 Ñ Match output for Timer 1, channel 0.
P0.13/DTR1/ MAT1.1	85[1]	I/O	P0.13 Ñ General purpose digital input/output pin.
		O	DTR1 Ñ Data Terminal Ready output for UART1.
		O	MAT1.1 Ñ Match output for Timer 1, channel 1.
P0.14/DCD1/ EINT1	92[2]	I/O	P0.14 Ñ General purpose digital input/output pin.
		I	DCD1 Ñ Data Carrier Detect input for UART1.
		I	EINT1 Ñ External interrupt 1 input. Note: LOW on this pin while $\overline{RESET}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0.15/RI1/ EINT2	99[2]	I/O	P0.15 Ñ General purpose digital input/output pin.
		I	RI1 Ñ Ring Indicator input for UART1.
		I	EINT2 Ñ External interrupt 2 input.
P0.16/EINT0/ MAT0.2/CAP0.2	100[2]	I/O	P0.16 Ñ General purpose digital input/output pin.
		I	EINT0 Ñ External interrupt 0 input.
		O	MAT0.2 Ñ Match output for Timer 0, channel 2.
		I	CAP0.2 Ñ Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	101[1]	I/O	P0.17 Ñ General purpose digital input/output pin.
		I	CAP1.2 Ñ Capture input for Timer 1, channel 2.
		I/O	SCK1 Ñ Serial Clock for SPI1/SSP. SPI clock output from master or input to slave (SSP is available in LPC2290/01 only).
		O	MAT1.2 Ñ Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	121[1]	I/O	P0.18 Ñ General purpose digital input/output pin.
		I	CAP1.3 Ñ Capture input for Timer 1, channel 3.
		I/O	MISO1 Ñ Master In Slave Out for SPI1/SSP. Data input to SPI master or data output from SPI slave (SSP is available in LPC2290/01 only).
		O	MAT1.3 Ñ Match output for Timer 1, channel 3.

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Table 3. Pin description *Écontinued*

Symbol	Pin	Type	Description
P0.19/MAT1.2/ MOSI1/CAP1.2	122[1]	I/O	P0.19 Ñ General purpose digital input/output pin.
		O	MAT1.2 Ñ Match output for Timer 1, channel 2.
		I/O	MOSI1 Ñ Master Out Slave In for SPI1/SSP. Data output from SPI master or data input to SPI slave (SSP is available in LPC2290/01 only).
		I	CAP1.2 Ñ Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	123[2]	I/O	P0.20 Ñ General purpose digital input/output pin.
		O	MAT1.3 Ñ Match output for Timer 1, channel 3.
		I	SSEL1 Ñ Slave Select for SPI1/SSP. Selects the SPI interface as a slave (SSP is available in LPC2290/01 only).
		I	EINT3 Ñ External interrupt 3 input.
P0.21/PWM5/ CAP1.3	4[1]	I/O	P0.21 Ñ General purpose digital input/output pin.
		O	PWM5 Ñ Pulse Width Modulator output 5.
		I	CAP1.3 Ñ Capture input for Timer 1, channel 3.
P0.22/CAP0.0/ MAT0.0	5[1]	I/O	P0.22 Ñ General purpose digital input/output pin.
		I	CAP0.0 Ñ Capture input for Timer 0, channel 0.
		O	MAT0.0 Ñ Match output for Timer 0, channel 0.
P0.23/RD2	6[1]	I/O	P0.23 Ñ General purpose digital input/output pin.
		I	RD2 Ñ CAN2 receiver input.
P0.24/TD2	8[1]	I/O	P0.24 Ñ General purpose digital input/output pin.
		O	TD2 Ñ CAN2 transmitter output.
P0.25	21[1]	I/O	P0.25 Ñ General purpose digital input/output pin.
		I	RD1 Ñ CAN1 receiver input.
P0.27/AIN0/ CAP0.1/MAT0.1	23[4]	I/O	P0.27 Ñ General purpose digital input/output pin.
		I	AIN0 Ñ ADC, input 0. This analog input is always connected to its pin.
		I	CAP0.1 Ñ Capture input for Timer 0, channel 1.
		O	MAT0.1 Ñ Match output for Timer 0, channel 1.
P0.28/AIN1/ CAP0.2/MAT0.2	25[4]	I/O	P0.28 Ñ General purpose digital input/output pin.
		I	AIN1 Ñ ADC, input 1. This analog input is always connected to its pin.
		I	CAP0.2 Ñ Capture input for Timer 0, channel 2.
		O	MAT0.2 Ñ Match output for Timer 0, channel 2.
P0.29/AIN2/ CAP0.3/MAT0.3	32[4]	I/O	P0.29 Ñ General purpose digital input/output pin.
		I	AIN2 Ñ ADC, input 2. This analog input is always connected to its pin.
		I	CAP0.3 Ñ Capture input for Timer 0, Channel 3.
		O	MAT0.3 Ñ Match output for Timer 0, channel 3.
P0.30/AIN3/ EINT3/CAP0.0	33[4]	I/O	P0.30 Ñ General purpose digital input/output pin.
		I	AIN3 Ñ ADC, input 3. This analog input is always connected to its pin.
		I	EINT3 Ñ External interrupt 3 input.
		I	CAP0.0 Ñ Capture input for Timer 0, channel 0.
P1.0 to P1.31		I/O	Port 1: Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 2 through 15 of port 1 are not available.

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25.4ctors

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Table 3. Pin description *Écontinued*

Symbol	Pin	Type	Description
P3.0/A0	89[5]	I/O	P3.0 Ñ General purpose digital input/output pin.
		O	A0 Ñ External memory address line 0.
P3.1/A1	88[5]	I/O	P3.1 Ñ General purpose digital input/output pin.
		O	A1 Ñ External memory address line 1.
P3.2/A2	87[5]	I/O	P3.2 Ñ General purpose digital input/output pin.
		O	A2 Ñ External memory address line 2.
P3.3/A3	81[5]	I/O	P3.3 Ñ General purpose digital input/output pin.
		O	A3 Ñ External memory address line 3.
P3.4/A4	80[5]	I/O	P3.4 Ñ General purpose digital input/output pin.
		O	A4 Ñ External memory address line 4.
P3.5/A5	74[5]	I/O	P3.5 Ñ General purpose digital input/output pin.
		O	A5 Ñ External memory address line 5.
P3.6/A6	73[5]	I/O	P3.6 Ñ General purpose digital input/output pin.
		O	A6 Ñ External memory address line 6.
P3.7/A7	72[5]	I/O	P3.7 Ñ General purpose digital input/output pin.
		O	A7 Ñ External memory address line 7.
P3.8/A8	71[5]	I/O	P3.8 Ñ General purpose digital input/output pin.
		O	A8 Ñ External memory address line 8.
P3.9/A9	66[5]	I/O	P3.9 Ñ General purpose digital input/output pin.
		O	A9 Ñ External memory address line 9.
P3.10/A10	65[5]	I/O	P3.10 Ñ General purpose digital input/output pin.
		O	A10 Ñ External memory address line 10.
P3.11/A11	64[5]	I/O	P3.11 Ñ General purpose digital input/output pin.
		O	A11 Ñ External memory address line 11.
P3.12/A12	63[5]	I/O	P3.12 Ñ General purpose digital input/output pin.
		O	A12 Ñ External memory address line 12.
P3.13/A13	62[5]	I/O	P3.13 Ñ General purpose digital input/output pin.
		O	A13 Ñ External memory address line 13.
P3.14/A14	56[5]	I/O	P3.14 Ñ General purpose digital input/output pin.
		O	A14 Ñ External memory address line 14.
P3.15/A15	55[5]	I/O	P3.15 Ñ General purpose digital input/output pin.
		O	A15 Ñ External memory address line 15.
P3.16/A16	53[5]	I/O	P3.16 Ñ General purpose digital input/output pin.
		O	A16 Ñ External memory address line 16.
P3.17/A17	48[5]	I/O	P3.17 Ñ General purpose digital input/output pin.
		O	A17 Ñ External memory address line 17.
P3.18/A18	47[5]	I/O	P3.18 Ñ General purpose digital input/output pin.
		O	A18 Ñ External memory address line 18.
P3.19/A19	46[5]	I/O	P3.19 Ñ General purpose digital input/output pin.
		O	A19 Ñ External memory address line 19.

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Table 3. Pin description *Écontinued*

Symbol	Pin	Type	Description
$V_{SSA(PLL)}$	138	I	PLL analog ground: 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(1V8)}$	37, 110	I	1.8 V core power supply: This is the power supply voltage for internal circuitry.
$V_{DDA(1V8)}$	143	I	Analog 1.8 V core power supply: This is the power supply voltage for internal circuitry. This should be nominally the same voltage as $V_{DD(1V8)}$ but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	2, 31, 39, 51, 57, 77, 94, 104, 112, 119	I	3.3 V pad power supply: This is the power supply voltage for the I/O ports.
$V_{DDA(3V3)}$	14	I	Analog 3.3 V pad power supply: This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If conÞgured for an input function, this pad utilizes built-in glitch Þlter that blocks pulses shorter than 3 ns.

[3] Open-drain 5 V tolerant digital I/O I^2C-bus 400 kHz speciÞcation compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If conÞgured for a digital input function, this pad utilizes built-in glitch Þlter that blocks pulses shorter than 3 ns. When conÞgured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistorÕs value ranges from 60 kΩ to 300 kΩ.

[6] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[7] Pad provides special analog functionality.

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6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISC. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

¥ The standard 32-bit ARM set.

¥ A 16-bit Thumb set.

The Thumb setÕs 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARMÕs performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2290 provides 16 kB of SRAM and the LPC2290/01 provides 64 kB of SRAM.

6.3 Memory map

The LPC2290 memory maps incorporate several distinct regions, as shown in Figure 3.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either on-chip bootloader, external memory BANK0 or on-chip static RAM. This is described in Section 6.18 ÒSystem controlÓ.

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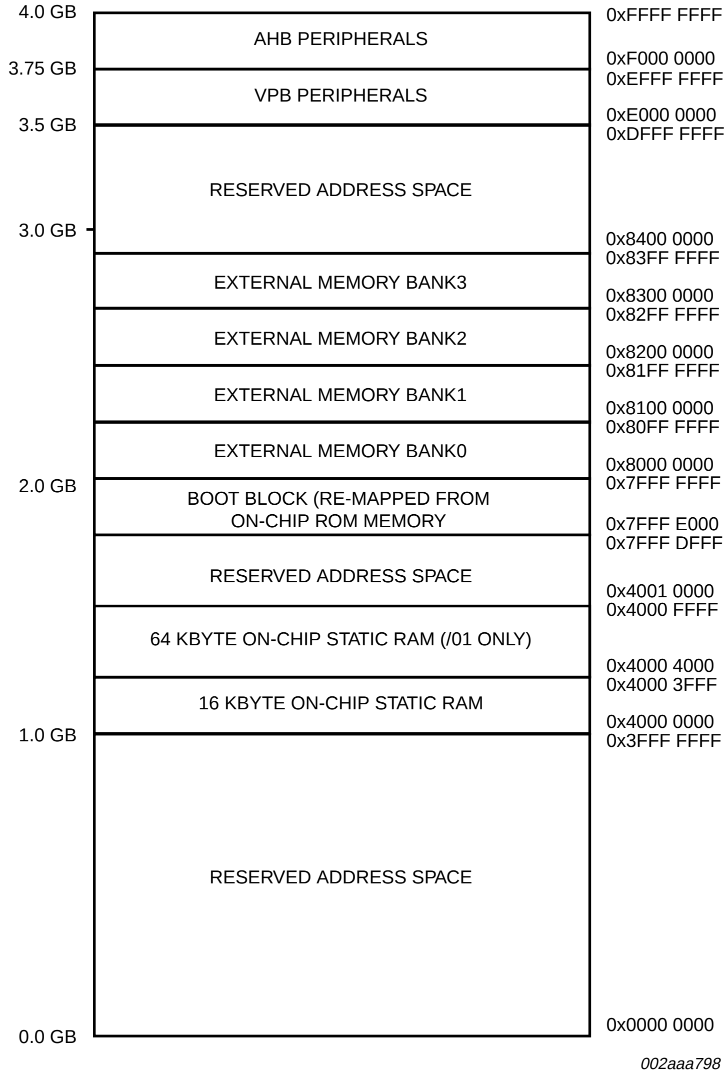

Fig 3. LPC2290 and LPC2290/01 memory map

6.4 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as deÞned by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classiÞed as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identiÞes which FIQ source(s) is (are) requesting an interrupt.

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¥ All I/O default to inputs after reset.

6.7.2 Fast I/O features available in LPC2290/01 only

¥ Fast I/O registers are located on the ARM local bus for the fastest possible I/O timing.

¥ All GPIO registers are byte addressable.

¥ Entire port value can be written in one instruction.

¥ Mask registers allow single instruction to set or clear any number of bits in one port.

6.8 10-bit ADC

The LPC2290 each contain a single 10-bit successive approximation ADC with eight multiplexed channels.

6.8.1 Features

¥ Measurement range of 0 V to 3.3 V.

¥ Capable of performing more than 400000 10-bit samples per second.

¥ Burst conversion mode for single or multiple inputs.

¥ Optional conversion on transition on input pin or Timer Match signal.

6.8.2 ADC features available in LPC2290/01 only

¥ Every analog input has a dedicated result register to reduce interrupt overhead.

¥ Every analog input can generate an interrupt once the conversion is completed.

6.9 CAN controllers and acceptance Þlter

The LPC2290 contains two CAN controllers. The CAN is a serial communications protocol which efÞciently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

6.9.1 Features

¥ Data rates up to 1 Mbit/s on each bus.

¥ 32-bit register and RAM access.

¥ Compatible with CAN speciÞcation 2.0B, ISO 11898-1.

¥ Global Acceptance Filter recognizes 11-bit and 29-bit RX identiÞers for all CAN buses.

¥ Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identiÞers.

¥ Full CAN messages can generate interrupts.

6.10 UARTs

The LPC2290 contains two UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

6.10.1 Features

¥ 16 B Receive and Transmit FIFOs.

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- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in baud rate generator.
- Standard modem interface signals included on UART1.

6.10.2 UART features available in LPC2290/01 only

- The transmission FIFO control enables implementation of software (XON/XOFF) ßow control on both UARTs and hardware (CTS/RTS) ßow control on UART1 only.
- Fractional baud rate generator enables standard baud rates such as 115200 to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS ßow-control fully implemented in hardware.

6.11 I^{2}C-bus serial I/O controller

The I^{2}C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^{2}C-bus implemented in LPC2290 supports bit rate up to 400 kbit/s (Fast I^{2}C-bus).

6.11.1 Features

- Compliant with standard I^{2}C-bus interface.
- Easy to conÞgure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^{2}C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The LPC2290 contains two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

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6.12.1 Features

¥ Compliant with SPI speciÞcation.

¥ Synchronous, serial, full duplex, communication.

¥ Combined SPI master and slave.

¥ Maximum data bit rate of one eighth of the input clock rate.

6.13 SSP serial I/O controller (available in LPC2290/01 only)

The LPC2290/01 contains one Serial Synchronous Port controller (SSP). The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data ßowing from the master to the slave and from the slave to the master. Often only one of these data ßows carries meaningful data.

The SSP and SPI1 share the same pins on LPC2290/01. After a reset, SPI1 is enabled and SSP is disabled.

6.13.1 Features

¥ Synchronous Serial Communication.

¥ 8-frame FIFOs for both transmit and receive.

¥ Compatible with Motorola SPI, 4-wire TI SSI and National Semiconductor Microwire buses.

¥ Master or slave operation.

¥ Four bits to 16 bits per SPI frame.

6.14 General purpose timers

The TIMER0 and TIMER1 are designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions at speciÞed timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ÔorÕ and ÔandÕ, as well as ÔbroadcastÕ functions among them.

6.14.1 Features

¥ A 32-bit Timer/Counter with a programmable 32-bit prescaler.

¥ Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.

¥ Four 32-bit match registers that allow:

  Ð Continuous operation with optional interrupt generation on match.

  Ð Stop timer on match with optional interrupt generation.

  Ð Reset timer on match with optional interrupt generation.

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¥ Four external outputs per timer corresponding to match registers, with the following capabilities:

  Ð Set LOW on match.

  Ð Set HIGH on match.

  Ð Toggle on match.

  Ð Do nothing on match.

6.14.2 Timer features available in LPC2290/01 only

¥ Timers can count cycles of the externally supplied clock providing external event counting functionality

6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ÔfeedÕ (or reload) the watchdog within a predetermined amount of time.

6.15.1 Features

¥ Internally resets chip if not periodically reloaded.

¥ Debug mode.

¥ Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

¥ Incorrect/incomplete feed sequence causes reset/interrupt if enabled.

¥ Flag to indicate watchdog reset.

¥ Programmable 32-bit timer with internal pre-scaler.

¥ Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

¥ Measures the passage of time to maintain a calendar and clock.

¥ Ultra-low power design to support battery powered systems.

¥ Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.

¥ Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

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¥ Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ÔreleaseÕ new match values before they can become effective.

¥ May be used as a standard timer if the PWM mode is not enabled.

¥ A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.18 System control

6.18.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 30 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 ÒPLLÓ for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must conÞgure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 µs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2290: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch Þlter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a Þxed number of clocks have passed, and the on-chip ßash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

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7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)	internal rail		–0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail		–0.5	+3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			–0.5	+4.6	V
V_{IA}	analog input voltage			–0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins	[2][3]	–0.5	+6.0	V
		other I/O pins	[2][4]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current	per supply pin	[5]	-	100	mA
I_{SS}	ground current	per ground pin	[5]	-	100	mA
T_{stg}	storage temperature		[6]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[7]	–2000	+2000	V

[1] The following applies to Table 5:

a) This product includes circuitry speciÞcally designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise speciÞed. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[4] Not to exceed 4.6 V.

[5] The peak current is limited to 25 times the corresponding maximum current.

[6] Dependent on package type.

[7] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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8. Static characteristics

Table 6. Static characteristics

T_{amb} = –40 °C to +85 °C for industrial applications, unless otherwise speciÞed.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)	internal rail		1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail		3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	V_I = $V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V, V_O = $V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	–(0.5$V_{DD(3V3)}$) < V_I < (1.5$V_{DD(3V3)}$); T_j < 125 °C		100	-	-	mA
V_I	input voltage		[2][3][4]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	[5]	$V_{DD(3V3)}$ – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = –4 mA	[5]	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = $V_{DD(3V3)}$ – 0.4 V	[5]	–4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[5]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[6]	-	-	–45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = $V_{DD(3V3)}$	[6]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[7]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[8]	–15	–50	–85	µA
		$V_{DD(3V3)}$ < V_I < 5 V	[7]	0	0	0	µA
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V, CCLK = 60 MHz, T_{amb} = 25 °C, code `while(1){}` executed from ßash, no active peripherals		-	50	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V, T_{amb} = 25 °C,		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V, T_{amb} = 85 °C		-	110	500	µA
		$V_{DD(1V8)}$ = 1.8 V, T_{amb} = 125 °C		-	300	1000	µA

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Table 6. Static characteristics Écontinued

T_{amb} = –40 °C to +85 °C for industrial applications, unless otherwise speciÞed.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.5V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[5]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$; to V_{SS}		-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Including voltage on outputs in 3-state mode.

[3] $V_{DD(3V3)}$ supply voltages must be present.

[4] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[5] Accounts for 100 mV voltage drop in all supply lines.

[6] Only allowed for a short time period.

[7] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[8] Applies to P1[25:16].

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Table 7. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +125 °C unless otherwise speciÞed. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	±2	LSB
E_O	offset error	[1][5]	-	-	±3	LSB
E_G	gain error	[1][6]	-	-	±0.5	%
E_T	absolute error	[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 4.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 4.

[5] The offset error (E_O) is the absolute difference between the straight line which Þts the actual curve and the straight line which Þts the ideal curve. See Figure 4.

[6] The gain error (E_G) is the relative difference in percent between the straight line Þtting the actual transfer curve after removing offset error, and the straight line which Þts the ideal transfer curve. See Figure 4.

[7] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 4.

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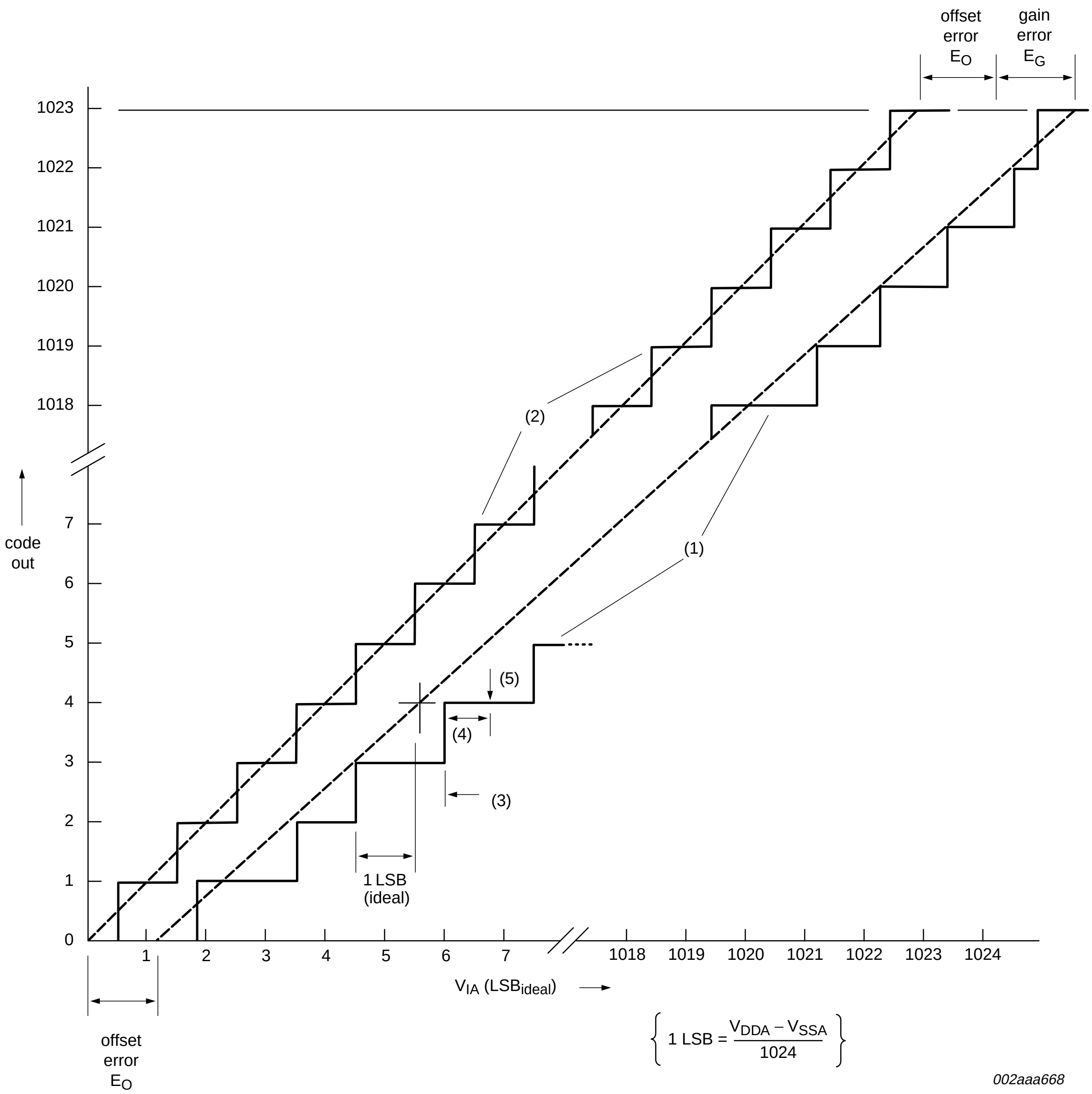

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 4. ADC characteristics

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9. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = −40 °C to +125 °C; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over speciÞed ranges[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
External clock							
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)		1	-	50	MHz
		external clock frequency supplied by an external crystal oscillator		1	-	30	MHz
		external clock frequency if on-chip PLL is used		10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time			20	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns
Port pins (except P0.2 and P0.3)							
t_r	rise time			-	10	-	ns
t_f	fall time			-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)							
t_f	fall time	V_{IH} to V_{IL}	[2]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise speciÞed.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

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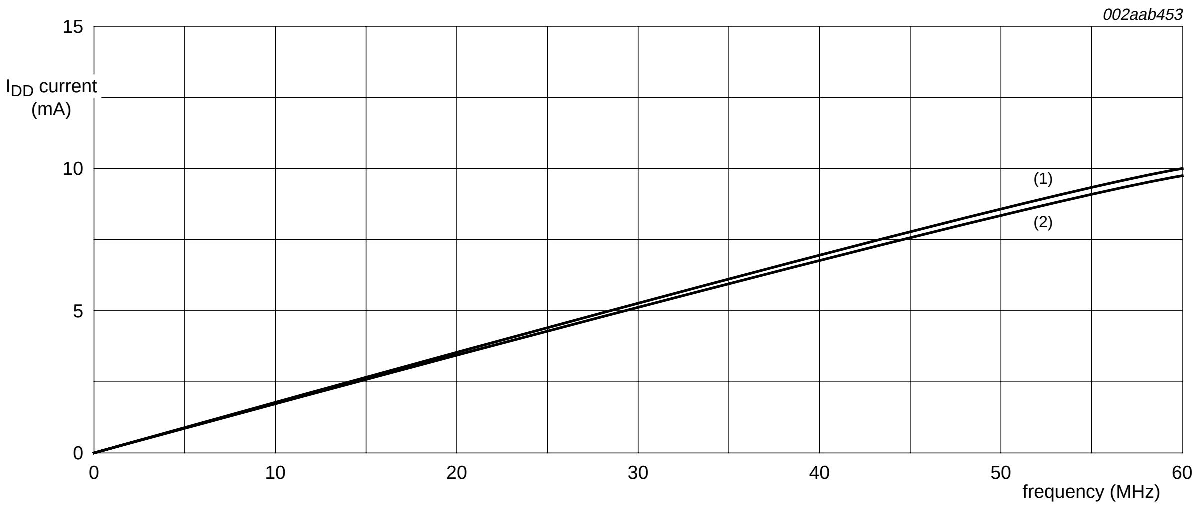
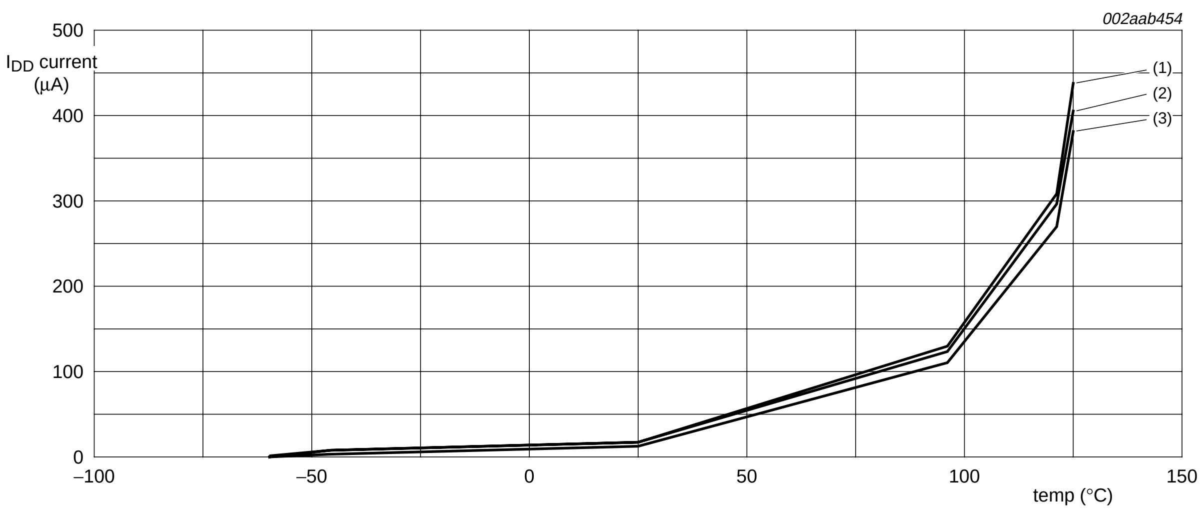


Test conditions: Idle mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register; PCLK = CCLK⁄4.

(1) 1.8 V core at 25 °C (typical)

(2) 1.65 V core at 25 °C (typical)

Fig 9. LPC2290 I_{DD} idle measured at different frequencies (CCLK) and temperatures



Test conditions: Power-down mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register.

(1) 1.95 V core

(2) 1.8 V core

(3) 1.65 V core

Fig 10. LPC2290 $I_{DD(pd)}$ measured at different temperatures

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