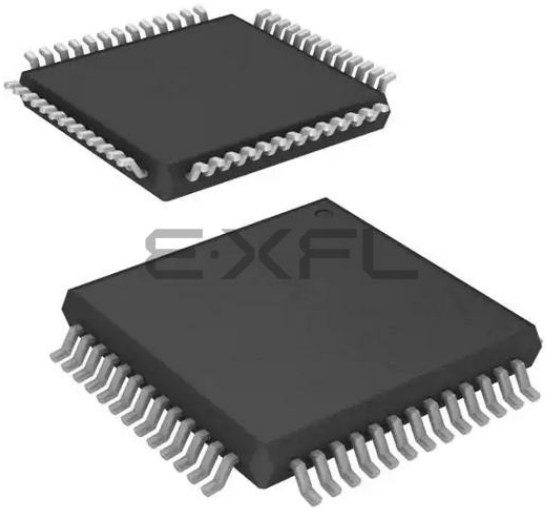

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.98K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f398kpmc1-g-sne2

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

Low-voltage detection reset circuit

- Built-in low-voltage detector

Clock supervisor counter

- Built-in clock supervisor counter function

Programmable port input voltage level

- CMOS input level / hysteresis input level

Dual operation Flash memory

- The erase/write operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

- Protects the content of the Flash memory

(Continued)

Part number / Parameter	MB95F394H	MB95F396H	MB95F398H	MB95F394K	MB95F396K	MB95F398K
UART/SIO	1 channel					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
I^2C	1 channel					
	• Master/slave transmission and receiving • It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.					
8/16-bit PPG	3 channels					
	• Each channel of PPG can be used as two 8-bit PPG channels or a single 16-bit PPG channel. • The counter operating clock can be selected from eight clock sources.					
16-bit PPG	• PWM mode and one-shot mode are available to use. • The counter operating clock can be selected from eight clock sources. • It supports external trigger start. • It can work independently or together with the multi-pulse generator.					
16-bit reload timer	• Two clock modes and two counter operating modes are available to use. • It can output square waveform. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Two counter operating modes: reload mode and one-shot mode • It can work independently or together with the multi-pulse generator.					
Multi-pulse generator (for DC motor control)	• 16-bit PPG timer: 1 channel • 16-bit reload timer operations: toggle output, one-shot output • Event counter: 1 channel • Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, and write/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of write/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-48P-M49 FPT-52P-M02 LCC-48P-M11					

5. Pin Functions

Pin no.			Pin name	I/O circuit type*4	Function
LQFP48*1	QFN48*2	LQFP52*3			
1	1	1	PG2	C	General-purpose I/O port
			X1A		Subclock I/O oscillation pin
			SNI2		Trigger input pin for the position detection function of the MPG waveform sequencer
2	2	2	PG1	C	General-purpose I/O port
			X0A		Subclock input oscillation pin
			SNI1		Trigger input pin for the position detection function of the MPG waveform sequencer
3	3	3	V_{CC}	—	Power supply pin
4	4	4	C	—	Capacitor connection pin
5	5	5	P40	K	General-purpose I/O port
			AN08		A/D converter analog input pin
6	6	6	P41	K	General-purpose I/O port
			AN09		A/D converter analog input pin
—	—	7	NC	—	It is an internally connected pin. Always leave it unconnected.
7	7	8	P42	K	General-purpose I/O port
			AN10		A/D converter analog input pin
8	8	9	P43	K	General-purpose I/O port
			AN11		A/D converter analog input pin
9	9	10	P44	G	General-purpose I/O port
			TO1		16-bit reload timer ch. 0 output pin
10	10	11	P45	G	General-purpose I/O port
			SCK		LIN-UART clock I/O pin
11	11	12	P46	G	General-purpose I/O port
			SOT		LIN-UART data output pin
12	12	13	P47	J	General-purpose I/O port
			SIN		LIN-UART data input pin
13	13	14	P10	G	General-purpose I/O port
			PPG10		8/16-bit PPG ch. 1 output pin
14	14	15	P11	G	General-purpose I/O port
			PPG11		8/16-bit PPG ch. 1 output pin
15	15	16	P12	H	General-purpose I/O port
			DBG		DBG input pin
16	16	17	P13	G	General-purpose I/O port
			PPG00		8/16-bit PPG ch. 0 output pin

(Continued)

Pin no.			Pin name	I/O circuit type*4	Function
LQFP48*1	QFN48*2	LQFP52*3			
17	17	18	P14	G	General-purpose I/O port
			PPG01		8/16-bit PPG ch. 0 output pin
18	18	19	P15	G	General-purpose I/O port
			PPG20		8/16-bit PPG ch. 2 output pin
—	—	20	NC	—	It is an internally connected pin. Always leave it unconnected.
19	19	21	P16	G	General-purpose I/O port
			PPG21		8/16-bit PPG ch. 2 output pin
20	20	22	P17	G	General-purpose I/O port
			SNI0		Trigger input pin for the position detection function of the MPG waveform sequencer
21	21	23	P70	G	General-purpose I/O port
			TO00		8/16-bit composite timer ch. 0 output pin
22	22	24	P71	G	General-purpose I/O port
			TO01		8/16-bit composite timer ch. 0 output pin
23	23	25	P72	I	General-purpose I/O port
			SCL		I^2C clock I/O pin
24	24	26	P73	I	General-purpose I/O port
			SDA		I^2C data I/O pin
25	25	27	P74	G	General-purpose I/O port
			EC0		8/16-bit composite timer ch. 0 clock input pin
26	26	28	P75	G	General-purpose I/O port
			UCK0		UART/SIO ch. 0 clock I/O pin
27	27	29	P76	G	General-purpose I/O port
			UO0		UART/SIO ch. 0 data output pin
28	28	30	P77	J	General-purpose I/O port
			UI0		UART/SIO ch. 0 data input pin
29	29	31	P60	G	General-purpose I/O port
			DTTI		MPG waveform sequencer input pin
30	30	32	P61	G	General-purpose I/O port
			TI1		16-bit reload timer ch. 0 input pin
—	—	33	NC	—	It is an internally connected pin. Always leave it unconnected.
31	31	34	P62	D	General-purpose I/O port High-current pin
			OPT0		MPG waveform sequencer output pin
			PPG00		8/16-bit PPG ch. 0 output pin
			TO10		8/16-bit composite timer ch. 1 output pin

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0060_H	IBCR00	I^2C bus control register 0	R/W	00000000_B
0061_H	IBCR10	I^2C bus control register 1	R/W	00000000_B
0062_H	IBCR0	I^2C bus status register	R/W	00000000_B
0063_H	IDDR0	I^2C data register	R/W	00000000_B
0064_H	IAAR0	I^2C address register	R/W	00000000_B
0065_H	ICCR0	I^2C clock control register	R/W	00000000_B
0066_H	OPCUR	Output control register (upper)	R/W	00000000_B
0067_H	OPCLR	Output control register (lower)	R/W	00000000_B
0068_H	IPCUR	Input control register (upper)	R/W	00000000_B
0069_H	IPCLR	Input control register (lower)	R/W	00000000_B
$006A_H$	NCCR	Noise cancellation control register	R/W	00000000_B
$006B_H$	TCSR	Timer control status register	R/W	00000000_B
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	00000000_B
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and mirror of direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B

(Continued)

13. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0, ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 1, ch. 5	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 2, ch. 6	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 3, ch. 7	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
UART/SIO ch. 0, MPG (DTTI)	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
8/16-bit PPG ch. 2 (upper)	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
8/16-bit PPG ch. 2 (lower)	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
16-bit reload timer ch. 1, MPG (write timing/compare clear), I^2C	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
16-bit PPG timer ch. 1, MPG (position detection/compare match)	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

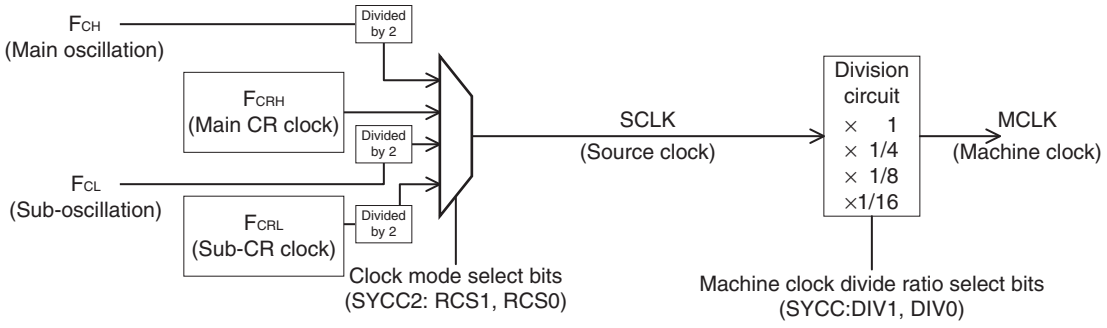
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*3	Max		
Power supply current*2	I_{CCTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz Time-base timer mode T_A = +25°C	—	0.9	3	mA	
	I_{CCH}		V_{CC} = 5.5 V Substop mode T_A = +25°C	—	3.4	22.5	µA	
	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	31	54	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	

*1: The input levels of P47, P72, P73 and P77 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

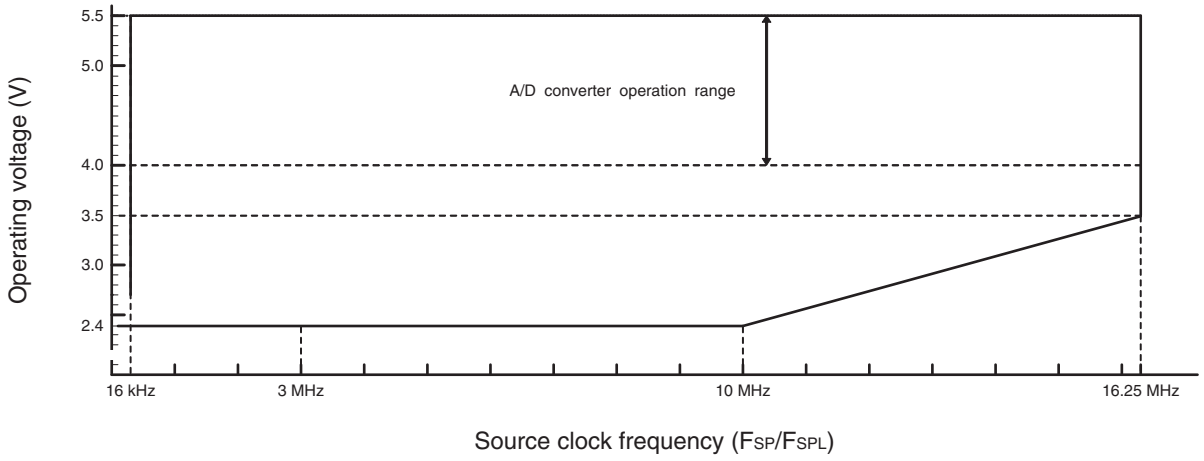
*2:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See "AC Characteristics: Clock Timing" for F_{CH} and F_{CL}.
- See "AC Characteristics: Source Clock/Machine Clock" for F_{MP} and F_{MPL}.

*3: V_{CC} = 5.0 V, T_A = 25°C

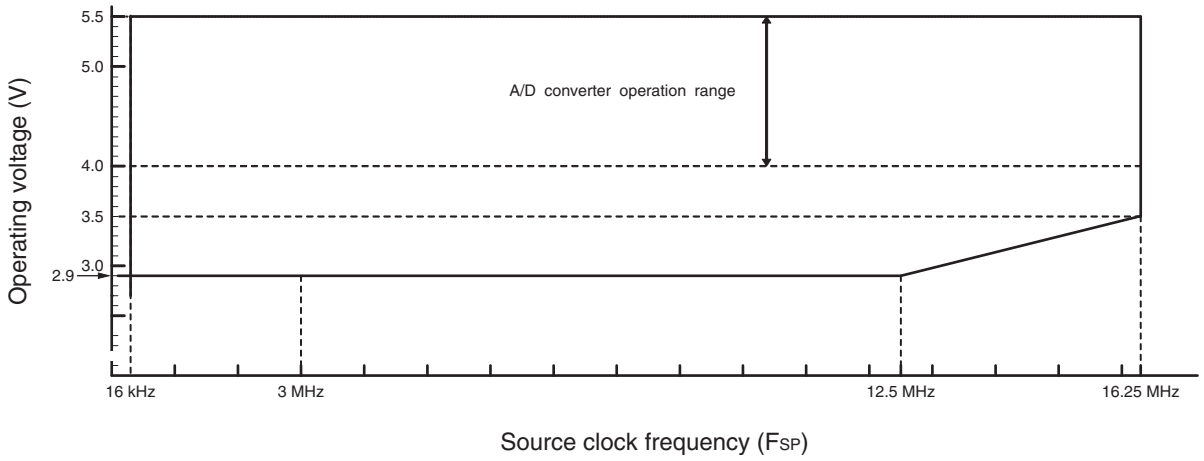
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (When T_A = −40°C to +85°C)
  MB95390H (without the on-chip debug function)



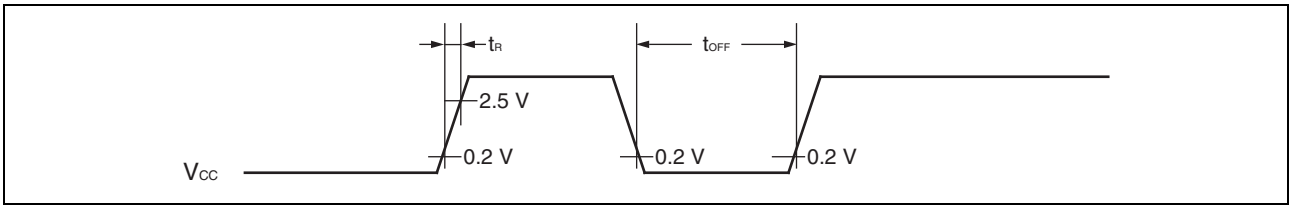
- Operating voltage - Operating frequency (When T_A = −40°C to +85°C)
  MB95390H (with the on-chip debug function)



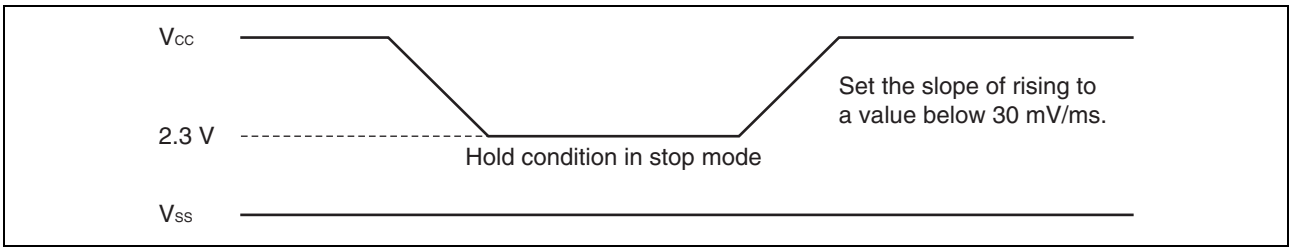
14.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

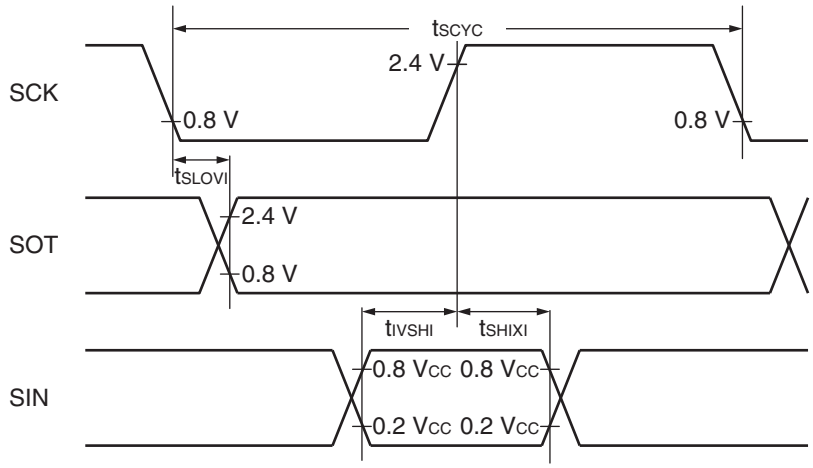
Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



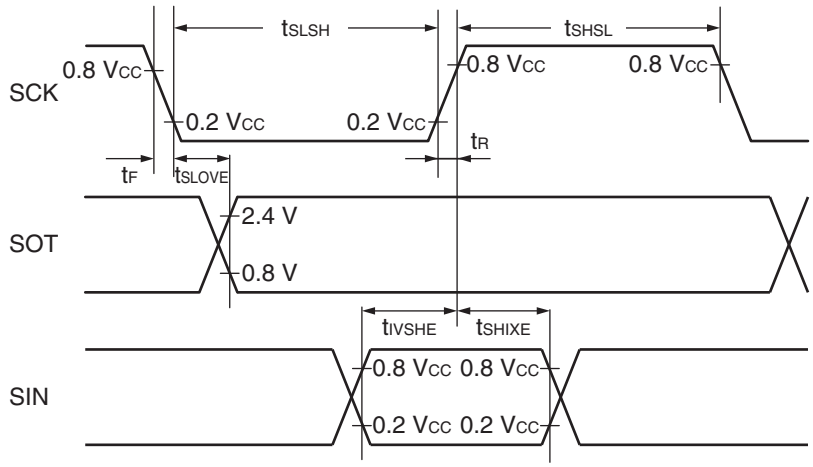
Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



- Internal shift clock mode



- External shift clock mode



Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

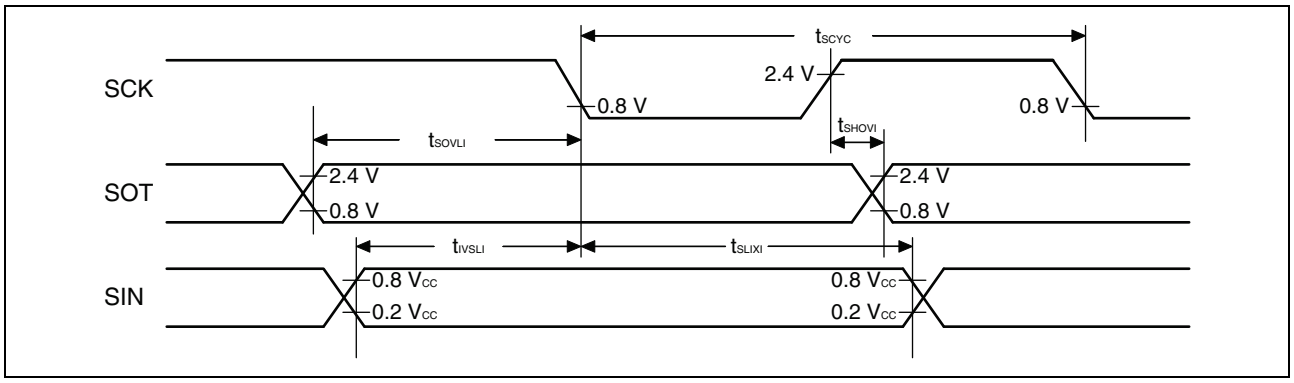
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

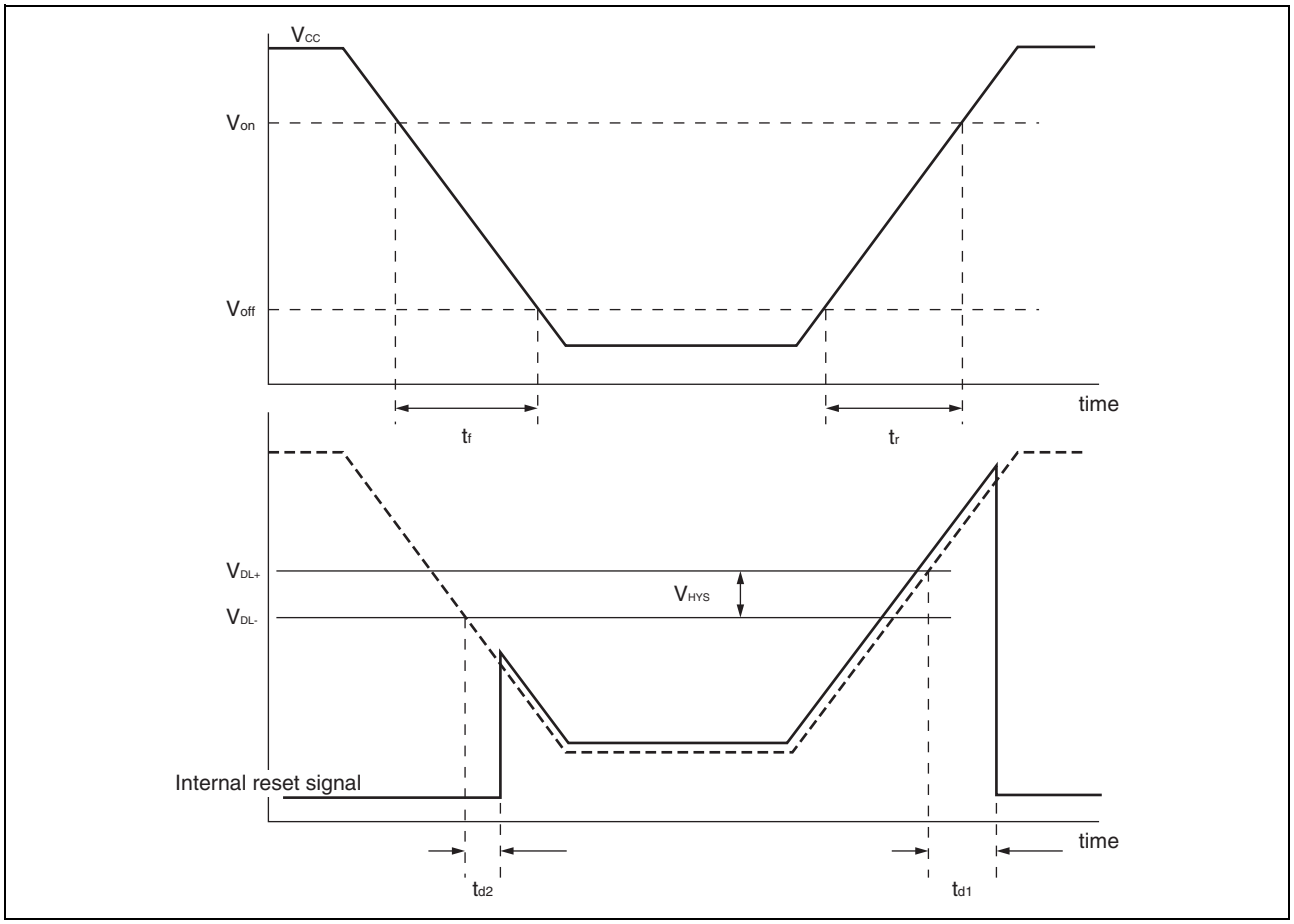
*3: See “Source Clock/Machine Clock” for t_{MCLK}.



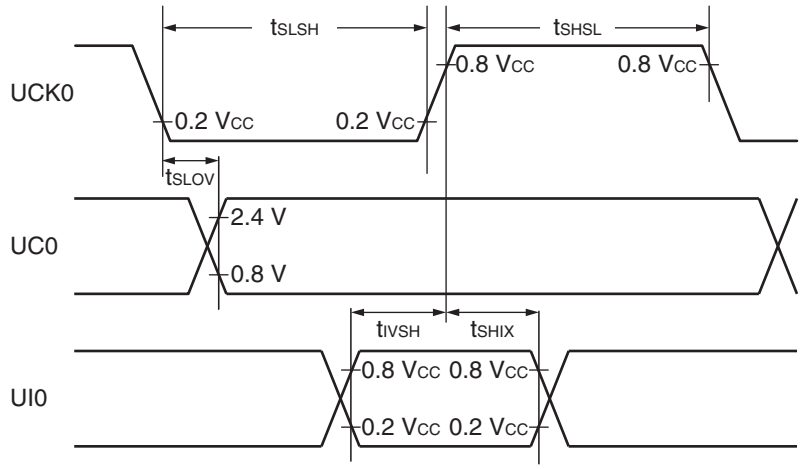
14.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	



- External shift clock mode



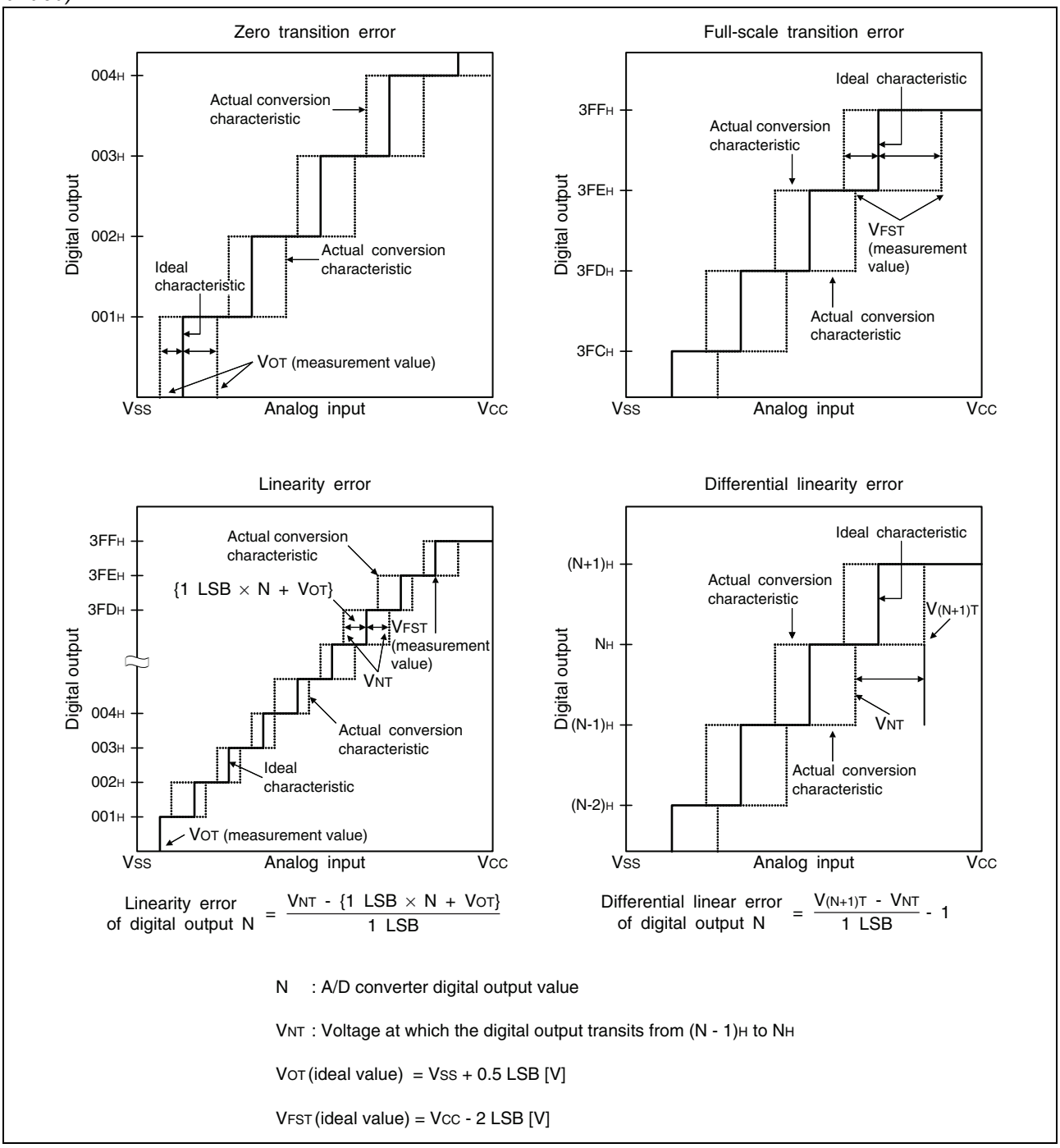
14.5 A/D Converter

14.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linear error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS} − 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} − 4.5 LSB	V_{CC} − 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

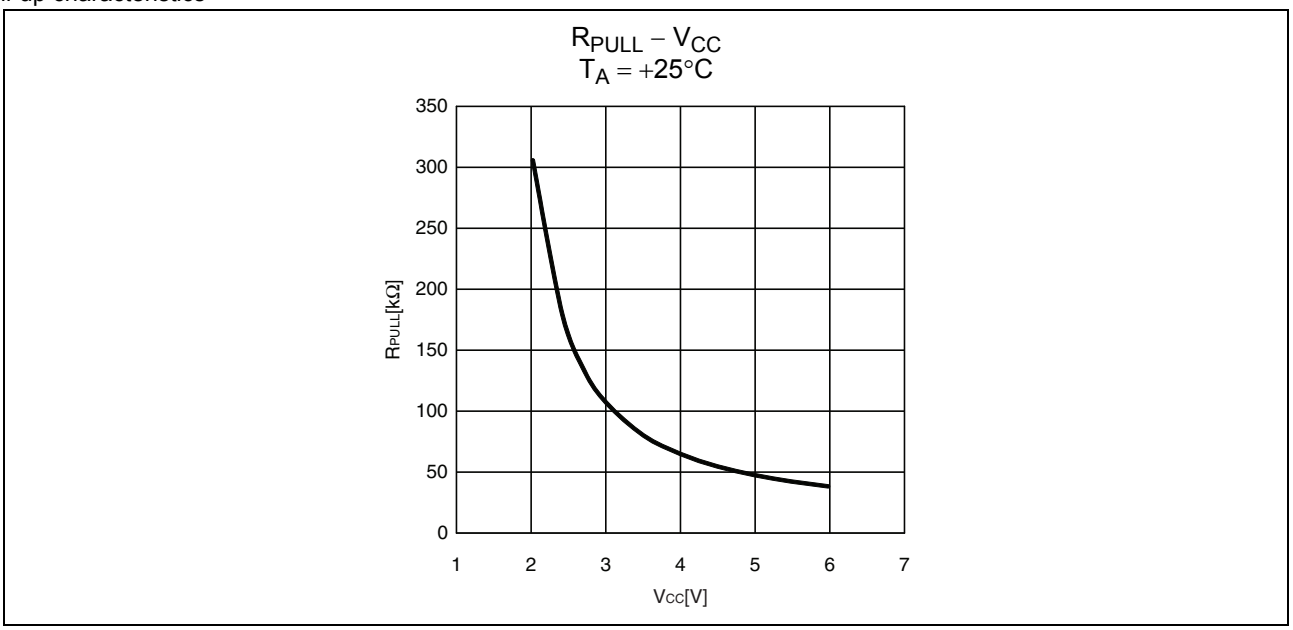
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

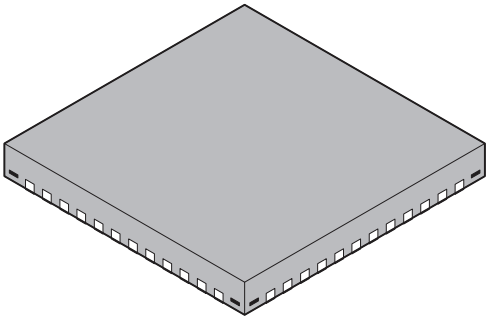
■ Pull-up characteristics



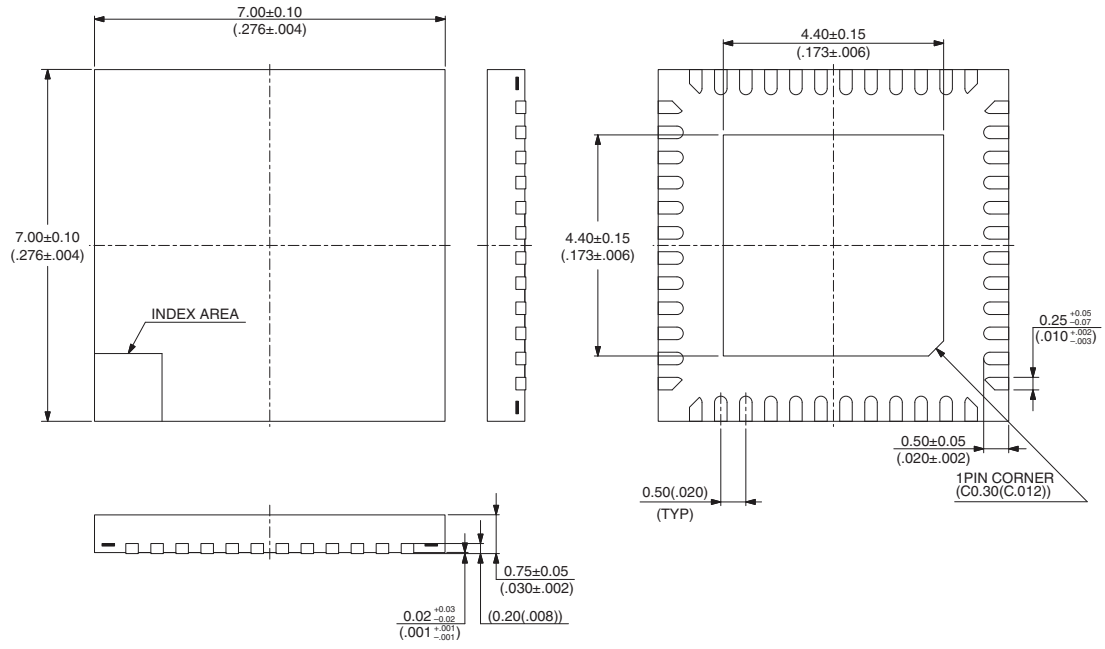
16. Mask Options

No.	Part Number	MB95F394H MB95F396H MB95F398H	MB95F394K MB95F396K MB95F398K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

(Continued)

48-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.12 g
(LCC-48P-M11)		

48-pin plastic QFN
(LCC-48P-M11)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

19. Major Changes

Page	Section	Details
1	Features	Changed the main CR clock oscillation accuracy. ±2% → ±2% or ±2.5% Added a remark about the main CR clock accuracy.
4	Product Line-up	Added FPT-52P-M02.
5	Packages And Corresponding Products	Added FPT-52P-M02.
6	Differences Among Products And Notes On Product Selection	Added a reference for the connection method in "• On-chip debug function".
8	Pin Assignment	Added the pin assignment diagram of FPT-52P-M02.
10 to 13	Pin Functions	Added the pin numbers of FPT-52P-M02.
34	Electrical Characteristics AC Characteristics Clock Timing	Changed the values of clock frequency (F_{CRH}). Added conditions related to the LQFP package and the QFN package for the values of clock frequency (F_{CRH}). Added footnotes *2 and *3.
58 to 63	Sample Characteristics	Added "Sample Characteristics".
65	Ordering Information	Added the part numbers of FPT-52P-M02.
67	Package Dimension	Added the package diagram of FPT-52P-M02.

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB95F394H/F396K/F398H/F394K/F396H/F398K CMOS F2MC-8FX MB95390H Series 8-bit Microcontrollers Document Number: 002-07573				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	07/27/2010	Migrated to Cypress and assigned document number 002-07573. No change to document contents or format.
*A	5185613	AKIH	3/31/2016	Updated to Cypress template

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