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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (32KB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912f634bv1aer2

Table 6. Maximum Electrical Ratings - MCU Die

Ratings	Symbol	Value	Unit
5.0 V Supply Voltage	V_{EDDX}	-0.3 to 6.0	V
2.5 V Supply Voltage	V_{EDD}	-0.3 to 2.75	V
Digital I/O input voltage (PA0...PA7, PE0, PE1)	V_{IN}	-0.3 to 6.0	V
EXTAL, XTAL	V_{ILV}	-0.3 to 2.16	V
TEST input	V_{TEST}	-0.3 to 10.0	V
Instantaneous maximum current Single pin limit for all digital I/O pins	I_D	-25 to 25	mA
Instantaneous maximum current Single pin limit for EXTAL, XTAL	I_{DL}	-25 to 25	mA

Table 7. Maximum Thermal Ratings

Ratings	Symbol	Value	Unit
Storage Temperature	T_{STG}	-55 to 150	°C
Package Thermal Resistance - LQFP48-EP Four layer board (JEDEC 2s2p) Junction to Ambient Natural Convection (7) Junction to Board (9) Two layer board (JEDEC 1s) Junction to Ambient Natural Convection (7), (8)	 $R_{\theta JA}$ $R_{\theta JB}$ $R_{\theta JA}$	 39 16 91	°C/W
Package Thermal Resistance - LQFP48 Four layer board (JEDEC 2s2p) Junction to Ambient Natural Convection (7) Junction to Board (9) Two layer board (JEDEC 1s) Junction to Ambient Natural Convection (7), (8)	 $R_{\theta JA}$ $R_{\theta JB}$ $R_{\theta JA}$	 59 31 96	°C/W
Peak Package Reflow Temperature During Reflow (10),(11)	T_{PPRT}	300	°C

Notes
7. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
8. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
9. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
10. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
11. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC34xxxD enter 34xxx), and review parametrics.

3.3 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

Table 8. Operating Conditions

Ratings	Symbol	Value	Unit
Analog Die Nominal Operating Voltage	V_{SUP}	5.5 to 18	V
Analog Die Functional Operating Voltage - Device is fully functional. All features are operating.	V_{SUPOP}	5.5 to 27	V
MCU I/O and supply voltage(12)	V_{EDDX}	4.5 to 5.5	V

Table 22. Static Electrical Characteristics - Current Sense Module - ISENSE

Ratings	Symbol	Min	Typ	Max	Unit
Gain	G				
CSGS (Current Sense Gain Select) = 000		-	7.0	-	
CSGS (Current Sense Gain Select) = 001		-	9.0	-	
CSGS (Current Sense Gain Select) = 010		-	10	-	
CSGS (Current Sense Gain Select) = 011		-	12	-	
CSGS (Current Sense Gain Select) = 100		-	14	-	
CSGS (Current Sense Gain Select) = 101		-	18	-	
CSGS (Current Sense Gain Select) = 110		-	24	-	
CSGS (Current Sense Gain Select) = 111		-	36	-	
Gain Accuracy		-3.0	-	3.0	%
Offset		-1.5	-	1.5	%
Resolution[26]	RES	-	51	-	mA/LSB
ISENSEH, ISENSEL Input Common Mode Voltage Range	V_{IN}	-0.2	-	3.0	V
Current Sense Module - Normal Mode Current Consumption Adder (CSE = 1)	I_{ISENSE}	-	600	-	µA

Note:
26. RES = 2.44 mV/(GAIN*R_{SHUNT})

Table 23. Static Electrical Characteristics - Temperature Sensor - TSENSE

Ratings	Symbol	Min	Typ	Max	Unit
Internal Chip Temperature Sense Gain[27]	TS_G	-	9.17	-	mV/k
Internal Chip Temperature Sense Error at the end of conversion[27]	TS_{ERR}	–5.0	-	5.0	°C
Temperature represented by a ADC_{IN} Voltage of 0.150 V[27]	$T_{0.15V}$	-55	-50	-45	°C
Temperature represented by a ADC_{IN} Voltage of 1.984 V[27]	$T_{1.984V}$	145	150	155	°C

Note:
27. Guaranteed by design and characterization.

Table 24. Static Electrical Characteristics - Supply Voltage Sense - VSENSE and VS1SENSE

Ratings	Symbol	Min	Typ	Max	Unit
VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VSENSE}$		10.8		
VSENSE error - whole path (VSENSE pin to Digital value)	ER_{VSENSE}	-	-	5.0	%
VS1SENSE Input Divider Ratio ($RATIO_{VS1SENSE}$ = $V_{VS1SENSE}$ / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VS1SENSE}$		10.8		
VS1SENSE error - whole path (VS1 pin to Digital value)	$ER_{VS1SENSE}$	-	-	5.0	%
VSENSE Series Resistor	R_{VSENSE}	9.5	10	10.5	kΩ
VSENSE Capacitor (optional)[28]	C_{VSENSE}	-	100	-	nF

Note:
28. The ESD behavior specified in Section 3.8, “ESD Protection and Latch-up Immunity" is guaranteed without the optional capacitor.

Table 36. Dynamic Electrical Characteristics - Analog Digital Converter - ADC

Ratings	Symbol	Min	Typ	Max	Unit
ADC Operating Frequency[39]	f_{ADC}	1.6	2.0	2.4	MHz
Conversion Time (from ACCR write to CC Flag)[39]	t_{CONV}		26		clk
Sample Frequency Channel 14 (Bandgap)[39]	f_{CH14}	-	-	2.5	kHz

Note:
39. Guaranteed by design.

3.6.2 Dynamic Electrical Characteristics MCU Die

3.6.2.1 NVM Timing

The time base for all NVM program or erase operations is derived from the bus block. A minimum bus frequency f_{NVMBUS} is required for performing program or erase operations. The NVM module do not has any means to monitor the frequency and does not prevent a program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency, a full program, or erase transition is not assured.

The Flash program and erase operations are timed using a clock derived from the bus clock using the FCLKDIV and register. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in Table 37 are calculated for maximum f_{NVMOP} and maximum f_{BUS}. The maximum times are calculated for minimum f_{NVMOP} and a f_{BUS} of 2.0 MHz.

3.6.2.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP}, and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

3.6.2.1.2 Burst Programming

This applies only to the Flash, where up to 64 words in a row can be programmed consecutively, using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 63 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

3.6.2.1.3 Sector Erase

NOTE

The sector erase cycle is divided into 16 individual erase pulses to achieve faster system response during the erase flow. The given erase time (t_{ERA}) specifies the time considering consecutive pulses.

3.6.2.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress tests during qualification, constant process monitors, and burn-in to screen early life failures. The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table 38. NVM Reliability Characteristics

Rating	Symbol	Min	Typ	Max	Unit
Data retention after 10,000 program/erase cycles for $T_{JAVG} \leq 85$ °C[45], [46]	t_{FLRET}	15	100[47]	-	Years
Data retention with <100 program/erase cycles for $T_{JAVG} \leq 85$ °C[45], [46]		20	100[47]	-	
Number of program/erase cycles[46] (-40 °C ≤ T_J ≤ 0 °C)	n_{FL}	10,000	-	-	Cycles
Number of program/erase cycles[46] (0 °C ≤ T_J ≤ 140 °C)		10,000	100,000[48]	-	

Note:
45. T_{JAVG} is the Average Junction Temperature
46. T_{JAVG} does not exceed 85 °C considering a typical temperature profile over the lifetime of a consumer, industrial, or automotive application.
47. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C, using the Arrhenius equation. For additional information on how Freescale defines Typical Data Retention, refer to Engineering Bulletin EB618.
48. Spec table quotes typical endurance evaluated at 25 °C for this product family, typical endurance at various temperature can be estimated using the graph in Figure 10. For additional information on how Freescale defines Typical Endurance, refer to Engineering Bulletin EB619.

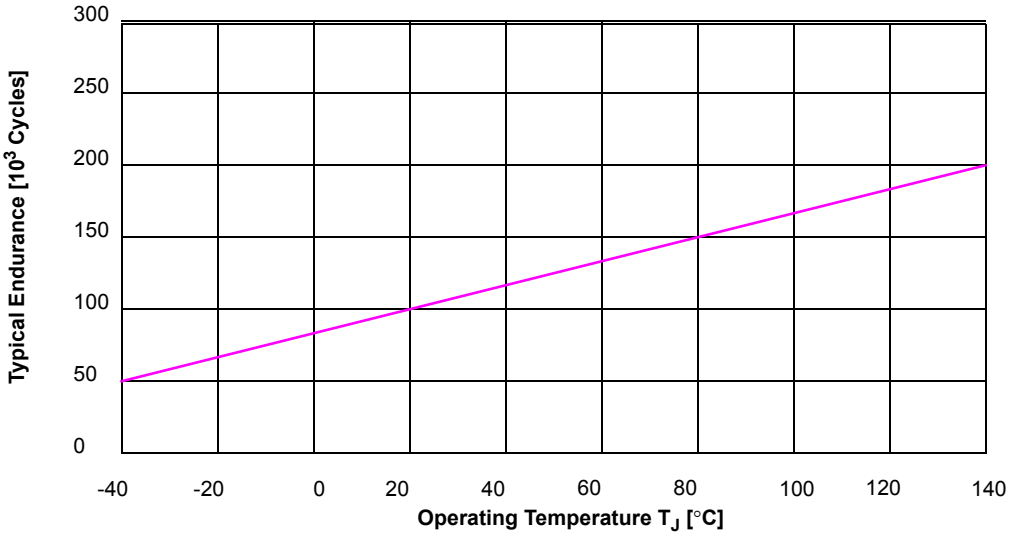


Figure 10. Typical Flash Cycling Endurance vs. Temperature

Table 77. VSR - Register Field Descriptions

Field	Description
4 VROVC	Voltage Regulator Overvoltage Condition - This status bit indicates an overvoltage warning is present for at least one of the main voltage regulators (VDD or VDDX). Reading the register clears the VROVI flag if present. See Section 4.6, “Interrupts" for details. Note: This feature requires the trimming of Section 4.25.2.3, “Trimming Register 2 (CTR2)" to be done to be effective. Untrimmed devices may issue the VROVC condition including the LS turn off at normal operation. 0 - No Voltage Regulator Overvoltage Condition present. 1 - Voltage Regulator Overvoltage Condition present.
3 HTC	High Temperature Condition - This status bit indicates a high temperature warning is present for the Voltage regulators (VDD/VDDX). Reading the register clears the HTI flag if present. See Section 4.6, “Interrupts" for details. 0 - No High Temperature Condition present. 1 - High Temperature Condition present.
2 HVC	High Voltage Condition - This status bit indicates a high voltage warning for VS2 is present. Reading the register clears the HVI flag if present. See Section 4.6, “Interrupts" for details. 0 - No High Voltage Condition present. 1 - High Voltage Condition present.
1 LVC	Low Voltage Condition - This status bit indicates a low voltage warning for VS1 is present. Reading the register clears the LVI flag if present. See Section 4.6, “Interrupts" for details. 0 - No Low Voltage Condition present. 1 - Low Voltage Condition present.
0 LBC	Low Battery Condition - This status bit indicates a low voltage warning for VSENSE is present. Reading the register clears the LBI flag if present. See Section 4.6, “Interrupts" for details. 0 - No Low Battery Condition present. 1 - Low Battery Condition present.

4.5 Die to Die Interface - Target

The D2D Interface is the bus interface to the Microcontroller. Access to the MM912F634 analog die is controlled by the D2D Interface module. This section describes the functionality of the die-to-die target block (D2D).

4.5.1 Overview

The D2D is the target for a data transfer from the target to the initiator (MCU). The initiator provides a set of configuration registers and two memory mapped 256 Byte address windows. When writing to a window, a transaction is initiated sending a write command, followed by an 8-bit address, and the data byte or word is received from the initiator. When reading from a window, a transaction is received with the read command, followed by an 8-bit address. The target then responds with the data. The basic idea is that a peripheral located on the MM912F634 analog die, can be addressed like an on-chip peripheral.

Features:

- software transparent register access to peripherals on the MM912F634 analog die
- 256 Byte address window
- supports blocking read or write, as well as non-blocking write transactions
- 4 bit physical bus width
- automatic synchronization of the target when initiator starts driving the interface clock
- generates transaction and error status as well as EOT acknowledge
- providing single interrupt interface to D2D Initiator

4.8.1 Wake-up Sources

4.8.1.1 Lx - Wake-up (Cyclic Sense Disabled)

Any state digital change on a Wake-up Enabled Lx input issues a wake-up. In order to select and activate a Wake-up Input (Lx), the Wake-up Control Register (WCR) must be configured with appropriate LxWE inputs enabled or disabled before entering low power mode. The Lx - Wake-up may be combined with the Forced Wake-up.

Note: Selecting a Lx Input for wake-up disables a selected analog input once entering low power mode.

4.8.1.2 Lx - Cyclic Sense Wake-up

NOTE

Once Cyclic Sense is configured (CSSEL!=0), the state change is only recognized from one cyclic sense event to the next.

The additional accuracy of the cyclic sense cycle by the WD clock trimming is only active during STOP mode. There is no trimmed clock available during SLEEP mode.

To reduce external power consumption during low power mode a cyclic wake-up has been implemented. Configuring the Timing Control Register (TCR) a specific cycle time can be selected to implement a periodic switching of the HS1 or HS2 output with the corresponding detection of an Lx state change. Any configuration of the HSx in the High-side Control Register (HSCR) is ignored when entering low power mode. The Lx - Cyclic Sense Wake-up may be combined with the Forced Wake-up. In case both (forced and Lx change) events are present at the same time, the Forced Wake-up is indicated as Wake-up source.

4.8.1.3 Forced Wake-up

Configuring the Forced Wake-up Multiplier (FWM) in the Timing Control Register (TCR) enables the forced wake-up based on the selected Cyclic Sense Timing (CST). Forced Wake-up can be combined with all other wake-up sources considering the timing dependencies.

4.8.1.4 LIN - Wake-up

While in Low-Power mode the MM912F634 analog die monitors the activity on the LIN bus. A dominant pulse longer than t_{PROPWL} followed by a dominant to recessive transition causes a LIN Wake-up. This behavior protects the system from a short-to-ground bus condition.

4.8.1.5 D2D - Wake-up (Stop Mode Only)

Receiving a Normal mode request via the D2D interface (MODE=0, Mode Control Register (MCR)) results in a wake-up from stop mode. As this condition is controlled by the MCU, no wake-up status bit does indicate this wake-up source.

4.8.1.6 Wake-up Due to Internal / External Reset (STOP Mode Only)

While in Stop mode, a Reset due to a VDD low voltage condition or an external Reset applied on the $\overline{\text{RESET\_A}}$ pin results in a Wake-up with immediate transition to Reset mode. In this case, the LVR or EXR bits in the Reset Status Register indicates the source of the event.

4.8.1.7 Wake-up Due to Loss of Supply Voltage (SLEEP Mode Only)

While in Sleep mode, a supply voltage VS1 < V_{POR} results in a transition to Power On mode.

4.10.1 Register Definition

4.10.1.1 Hall Supply Register (HSR)

Table 95. Hall Supply Register (HSR)

Offset[81] 0x38 Access: User read/write

	7	6	5	4	3	2	1	0
R	HOTIE	HOTC	0	0	0	0	0	HSUPON
W								
Reset	0	0	0	0	0	0	0	0

Note:
81. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 96. HSR - Register Field Descriptions

Field	Description
7 - HOTIE	Hall Supply Overtemperature Interrupt Enable
6 - HOTC	Hall Supply Overtemperature Condition present. During the event, the Hall Supply is shut down. Reading the register clears the HOT flag if present. See Section 4.6, “Interrupts" for details.
0 - HSUPON	Hall Supply On: 0 - Hall Supply Regulator disabled 1 - Hall Supply Regulator enabled

4.11 High-side Drivers - HS

These outputs are two High-side drivers, intended to drive small resistive loads or LEDs incorporating the following features:

- PWM capability via the PWM Module
- Open load detection
- Current limitation
- Overtemperature shutdown (with maskable interrupt)
- High voltage shutdown - HVI (software maskable)
- Cyclic-Sense, See Section 4.8, “Wake-up / Cyclic Sense"

4.11.1 Open Load Detection

Each high-side driver signals an Open Load condition if the current through the high-side is below the open load current threshold. The open load condition is indicated with the bits HS1OL and HS2OL in the High-side Status Register (HSSR).

When the High-side is in OFF state, the Open Load Detection function is not operating. When reading the HSSR register while the High-side is operating in PWM and is in the OFF state, the HS1OL and HS2OL bits does not indicate Open Load.

4.11.2 Current Limitation

Each high-side driver has an output current limitation. In combination with the overtemperature shutdown the high-side drivers are protected against overcurrent and short-circuit failures. The driver operating in the current limitation area is indicated with the bits HS1CL and HS2CL in the High-side Status Register (HSSR).

4.11.3 Overtemperature Protection (HS Interrupt)

Both high-side drivers are protected against overtemperature. In overtemperature conditions, both high-side drivers are shut down and the event is latched in the Interrupt Control Module. The shutdown is indicated as HS Interrupt in the Interrupt Source Register (ISR).

A thermal shutdown of the high-side drivers is indicated by setting the HSOT bit in the High-side Status Register (HSSR). A write to the High-side Control Register (HSCR), when the overtemperature condition is gone, re- enables the high-side drivers.

4.11.7.2 High-side Status Register (HSSR)

Table 99. High-side Status Register (HSSR)

Offset[83] 0x29 Access: User read

	7	6	5	4	3	2	1	0
R	HSOTC	0	0	0	HS2CL	HS1CL	HS2OL	HS1OL
W								
Reset	0	0	0	0	0	0	0	0

Note:
83. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 100. HSSR - Register Field Descriptions

Field	Description
7 - HSOTC	High-side Overtemperature Condition present. Both drivers are turned off. Reading the register clears the HSOT interrupt flag if present. See Section 4.6, "Interrupts" for details.
3 - HS2CL	High-side 2 Current Limitation
2 - HS1CL	High-side 1 Current Limitation
1 - HS2OL	High-side 2 Open Load [84]
0 - HS1OL	High-side 1 Open Load [84]

Note:
84. When the High-side is in OFF state, the Open Load Detection function is not operating. When reading the HSSR register while the High-side is operating in PWM and is in the OFF state, the HS1OL and HS2OL bits does not indicate Open Load.

4.12 Low-side Drivers - LSx

4.12.1 Introduction / Features

These outputs are two Low-side drivers intended to drive relays (inductive loads) incorporating the following features:

- PWM capability
- Open load detection
- Current limitation
- Overtemperature shutdown (with maskable interrupt)
- Active clamp
- Independent VREG - High Voltage Shutdown

4.12.5 PWM Capability

See Section 4.13, “PWM Control Module (PWM8B2C)".

4.12.6 Low-side Driver in Reverse Polarity

Freescale recommends the user implement their systems using an external diode to protect the low-side driver (LSx) from potential damage (see Figure 22) in the event of a reverse polarity condition. However, if the user chooses to implement their system without an external diode, and a reverse polarity condition were to occur, the current would flow through the body diode of the LSx driver and through the closing coil of the relay, as shown in Figure 23. The magnitude of current through this body diode is determined by the characteristics of this relay coil. Since this body diode is not specified to carry a sustained minimum amount of current, Freescale strongly recommends users implement their systems using an external reverse polarity protection diode.

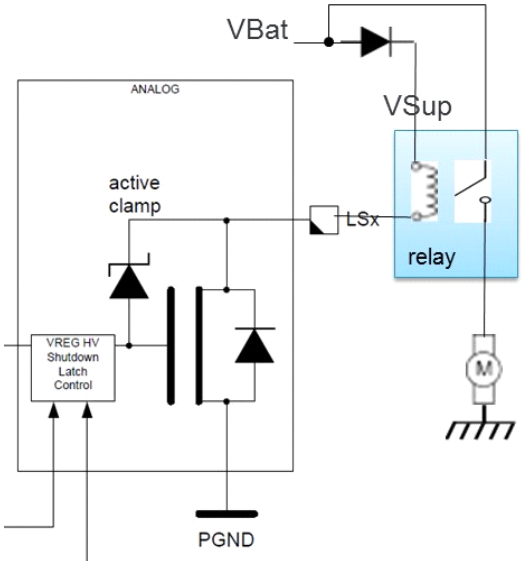


Figure 22. Low-side Driver Implemented With External Reverse Polarity Diode

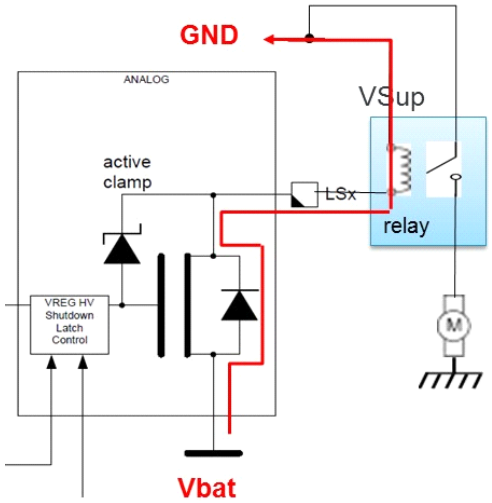


Figure 23. Current Flow in Low-side Driver Under Reverse Polarity Condition Without External Diode

- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Receiver wake-up by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

4.15.1.2 Modes of Operation

See Section 4.15.3, “Functional Description",” For details concerning SCI operation in these modes:

- 8- and 9-bit data modes
- Loop mode
- Single-wire mode

4.15.1.3 Block Diagram

Figure 32 shows the transmitter portion of the SCI.

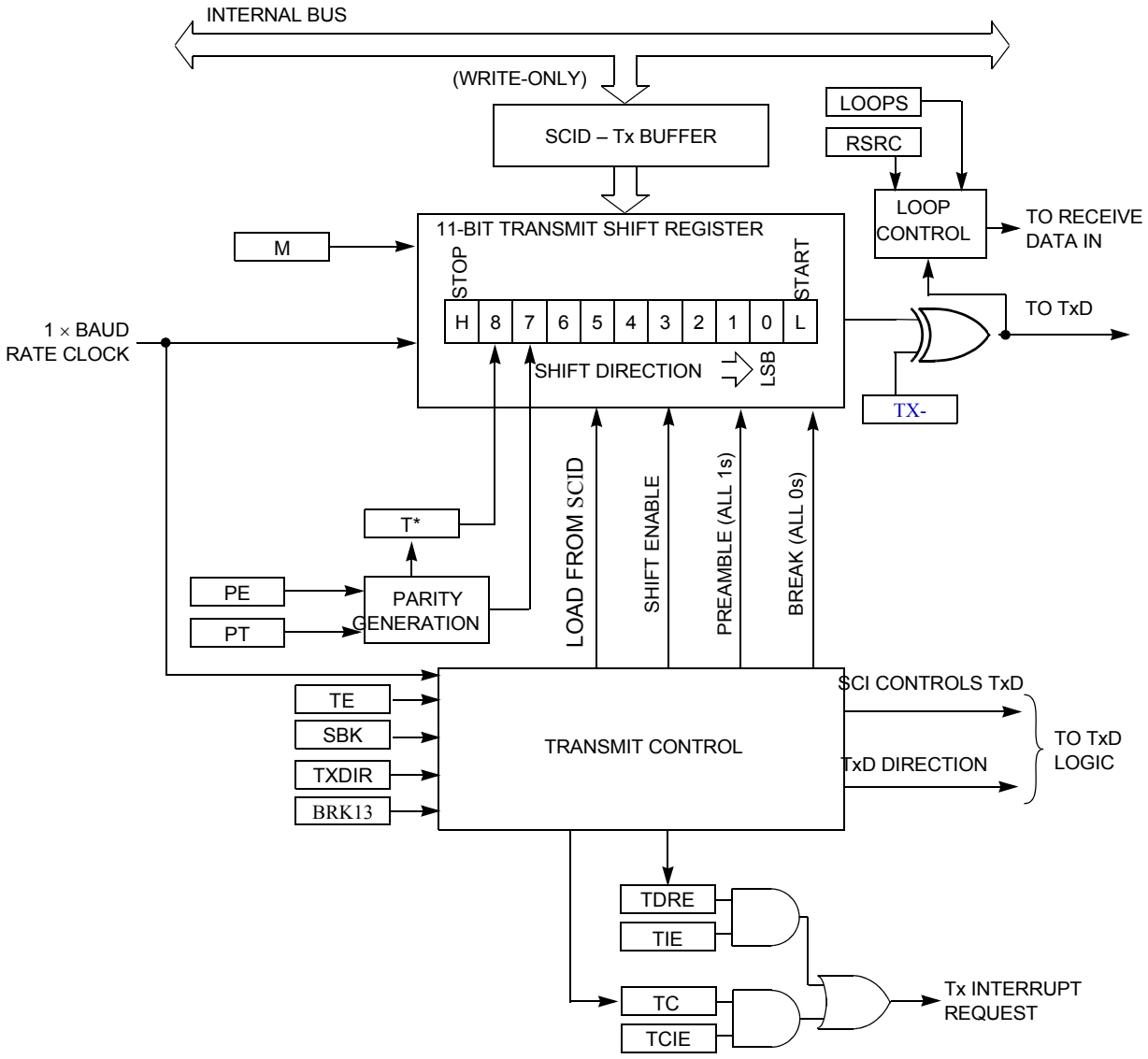


Figure 32. SCI Transmitter Block Diagram

Table 188. Analog Digital Converter Module - Memory Map (continued)

Register / Offset[135]		Bit 7	6	5	4	3	2	1	Bit 0
0x90 ADR5 (hi)	R	ADR5[9:2]							
	W								
0x91 ADR5 (lo)	R	ADR5[1:0]							
	W								
0x92 ADR6 (hi)	R	ADR6[9:2]							
	W								
0x93 ADR6 (lo)	R	ADR6[1:0]							
	W								
0x94 ADR7 (hi)	R	ADR7[9:2]							
	W								
0x95 ADR7 (lo)	R	ADR7[1:0]							
	W								
0x96 ADR8 (hi)	R	ADR8[9:2]							
	W								
0x97 ADR8 (lo)	R	ADR8[1:0]							
	W								
0x98 ADR9 (hi)	R	ADR9[9:2]							
	W								
0x99 ADR9 (lo)	R	ADR9[1:0]							
	W								
0x9A ADR10 (hi)	R	ADR10[9:2]							
	W								
0x9B ADR10 (lo)	R	ADR10[1:0]							
	W								
0x9C ADR11 (hi)	R	ADR11[9:2]							
	W								
0x9D ADR11 (lo)	R	ADR11[1:0]							
	W								
0x9E ADR12 (hi)	R	ADR12[9:2]							
	W								
0x9F ADR12 (lo)	R	ADR12[1:0]							
	W								
0xA0 Reserved	R								
	W								
0xA1 Reserved	R								
	W								
0xA2 ADR14 (hi)	R	ADR14[9:2]							
	W								

Table 218. Port A Data Register Description (continued)

Field	Description
2 PTA	**Port A general purpose input/output data**—Data Register Port A pin 2 is associated with the SCK signal of the SPI module. When not used with the alternative function, this pin can be used as general purpose I/O. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.
1 PTA	**Port A general purpose input/output data**—Data Register Port A pin 1 is associated with the MOSI signal of the SPI module. When not used with the alternative function, this pin can be used as general purpose I/O. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.
0 PTA	**Port A general purpose input/output data**—Data Register Port A pin 0 is associated with the MISO signal of the SPI module. When not used with the alternative function, this pin can be used as general purpose I/O. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.

4.27.3.2 PIM Reserved Register

Table 219. PIM Reserved Register

Address 0x0001 Access: User read(159)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Note:
159. Read: Anytime.
Write: Unimplemented. Writing to this register has no effect.

4.27.3.3 Port A Data Direction Register (DDRA)

Table 220. Port A Data Direction Register (DDRA)

Address 0x0002 Access: User read/write(160)

	7	6	5	4	3	2	1	0
R	0	0	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
W								
Reset	0	0	0	0	0	0	0	0

Note:
160. Read: Anytime.
Write: Anytime.

Table 221. DDRA Register Field Descriptions

Field	Description
5-0 DDRA	**Port A Data Direction**— This register controls the data direction of pins 5 through 0. The SPI function controls the data direction for the associated pins. In this case the data direction bits do not change. When operating a pin as a general purpose I/O, the associated data direction bit determines whether it is an input or output. 1 Associated pin is configured as output. 0 Associated pin is configured as high-impedance input.

The least significant word of line is read out first. This corresponds to the fields 1 and 0 of Table 315. The next word read returns field 2 in the least significant bits [3:0] and “0” for bits [15:4]. Reading the Trace Buffer while the DBG module is armed, returns invalid data, and no shifting of the RAM pointer occurs.

4.31.4.5.6 Trace Buffer Reset State

The Trace Buffer contents and DBGCNT bits are not initialized by a system reset. Thus should a system reset occur, the trace session information from immediately before the reset occurred, can be read out and the number of valid lines in the trace buffer is indicated by DBGCNT. The internal pointer to the current trace buffer address is initialized by unlocking the trace buffer and points to the oldest valid data, even if a reset occurred during the tracing session. To read the trace buffer after a reset, TSOURCE must be set, otherwise the trace buffer reads as all zeroes. Generally debugging occurrences of system resets is best handled using end trigger alignment, since the reset may occur before the trace trigger, which in the begin trigger alignment case means no information would be stored in the trace buffer. The Trace Buffer contents and DBGCNT bits are undefined following a POR

4.31.4.6 Tagging

A tag follows program information as it advances through the instruction queue. When a tagged instruction reaches the head of the queue, a tag hit occurs and can initiate a state sequencer transition.

Each comparator control register features a TAG bit, which controls whether the comparator match causes a state sequencer transition immediately or tags the opcode at the matched address. If a comparator is enabled for tagged comparisons, the address stored in the comparator match address registers must be an opcode address.

Using Begin trigger together with tagging, if the tagged instruction is about to be executed, then the transition to the next state sequencer state occurs. If the transition is to the Final State, tracing is started. Only upon completion of the tracing session can a breakpoint be generated. Using End alignment, when the tagged instruction is about to be executed and the next transition is to Final State, then a breakpoint is generated immediately before the tagged instruction is carried out.

R/W monitoring is not useful for tagged operations, since the taghit occurs based on the tagged opcode reaching the execution stage of the instruction queue. Similarly access size (SZ) monitoring and data bus monitoring is not useful if tagging is selected, since the tag is attached to the opcode at the matched address, and is not dependent on the data bus nor on the size of access. Thus these bits are ignored if tagging is selected.

When configured for range comparisons and tagging, the ranges are accurate only to word boundaries. Tagging is disabled when the BDM becomes active.

4.31.4.7 Breakpoints

It is possible to generate breakpoints from channel transitions to Final State or using software to write to the TRIG bit in the DBGC1 register.

4.31.4.7.1 Breakpoints From Comparator Channels

Breakpoints can be generated when the state sequencer transitions to the Final State. If configured for tagging, then the breakpoint is generated when the tagged opcode reaches the execution stage of the instruction queue.

If a tracing session is selected by the TSOURCE bit, breakpoints are requested when the tracing session has completed, thus if Begin aligned triggering is selected, the breakpoint is requested only on completion of the subsequent trace (see Table 320). If no tracing session is selected, breakpoints are requested immediately. If the BRK bit is set, then the associated breakpoint is generated immediately independent of tracing trigger alignment.

Table 320. Breakpoint Setup For CPU Breakpoints

BRK	TALIGN	DBGBRK	Breakpoint Alignment
0	0	0	Fill Trace Buffer until trigger, then disarm (no breakpoints)
0	0	1	Fill Trace Buffer until trigger, then breakpoint request occurs
0	1	0	Start Trace Buffer at trigger (no breakpoints)

Table 320. Breakpoint Setup For CPU Breakpoints (continued)

0	1	1	Start Trace Buffer at trigger, A breakpoint request occurs when Trace Buffer is full
1	x	1	Terminate tracing and generate breakpoint immediately on trigger
1	x	0	Terminate tracing immediately on trigger

4.31.4.7.2 Breakpoints Generated Via the TRIG Bit

If a TRIG triggers occur, the Final State is entered whereby tracing trigger alignment is defined by the TALIGN bit. If a tracing session is selected by the TSOURCE bit, breakpoints are requested when the tracing session has completed, thus if Begin aligned triggering is selected, the breakpoint is requested only on completion of the subsequent trace (see Table 320). If no tracing session is selected, breakpoints are requested immediately. TRIG breakpoints are possible even if the DBG module is disarmed.

4.31.4.7.3 Breakpoint Priorities

If a TRIG trigger occurs after Begin aligned tracing has already started, then the TRIG no longer has an effect. When the associated tracing session is complete, the breakpoint occurs. Similarly if a TRIG is followed by a subsequent comparator channel match, it has no effect, since tracing has already started.

If a forced SWI breakpoint coincides with a BGND in user code with BDM enabled, then the BDM is activated by the BGND and the breakpoint to SWI is suppressed.

4.31.4.7.3.1 DBG Breakpoint Priorities and BDM Interfacing

NOTE

When program control returns from a tagged breakpoint using an RTI or BDM GO command without program counter modification, it returns to the instruction whose tag generated the breakpoint. To avoid a repeated breakpoint at the same location, reconfigure the DBG module in the SWI routine, if configured for an SWI breakpoint, or over the BDM interface, by executing a TRACE command before the GO to increment the program flow past the tagged instruction.

Breakpoint operation is dependent on the state of the BDM module. If the BDM module is active, the CPU is executing out of BDM firmware, thus comparator matches and associated breakpoints are disabled. In addition, while executing a BDM TRACE command, tagging into BDM is disabled. If BDM is not active, the breakpoint gives priority to BDM requests over SWI requests, if the breakpoint happens to coincide with a SWI instruction in user code. On returning from BDM, the SWI from user code gets executed.

Table 321. Breakpoint Mapping Summary

DBGBRK	BDM Bit (DBGC1[4])	BDM Enabled	BDM Active	Breakpoint Mapping
0	X	X	X	No Breakpoint
1	0	X	0	Breakpoint to SWI
X	X	1	1	No Breakpoint
1	1	0	X	Breakpoint to SWI
1	1	1	0	Breakpoint to BDM

BDM cannot be entered from a breakpoint unless the ENABLE bit is set in the BDM. If entry to BDM via a BGND instruction is attempted and the ENABLE bit in the BDM is cleared, the CPU actually executes the BDM firmware code, checks the ENABLE, and returns if ENABLE is not set. If not serviced by the monitor, then the breakpoint is re-asserted when the BDM returns to normal CPU flow.

If the comparator register contents coincide with the SWI/BDM vector address, then an SWI in user code and DBG breakpoint could occur simultaneously. The CPU ensures BDM requests have a higher priority than SWI requests. Returning from the BDM/SWI service routine, care must be taken to avoid a repeated breakpoint at the same address.

Should a tagged or forced breakpoint coincide with a BGND in user code, then the instruction following the BGND instruction is the first instruction executed when normal program execution resumes.

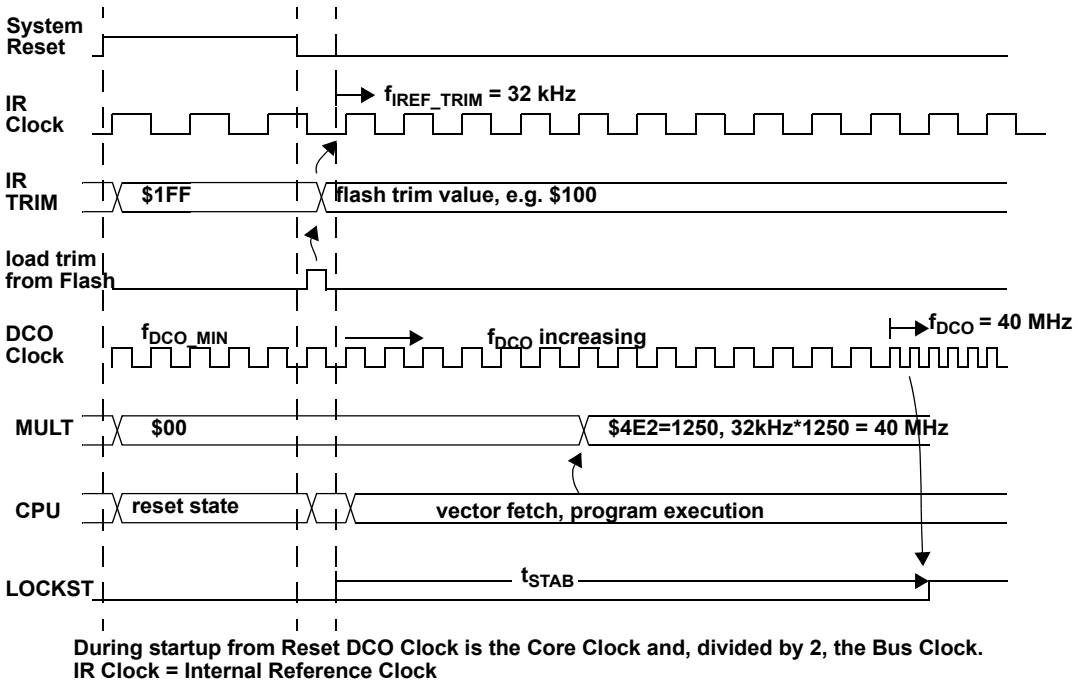


Figure 71. Example for Startup of Clock System After Reset

4.32.4.2 Stop Mode Using DCO Clock as a Bus Clock

An example of what happens going into stop mode and exiting stop mode after an interrupt is shown in Figure 72.

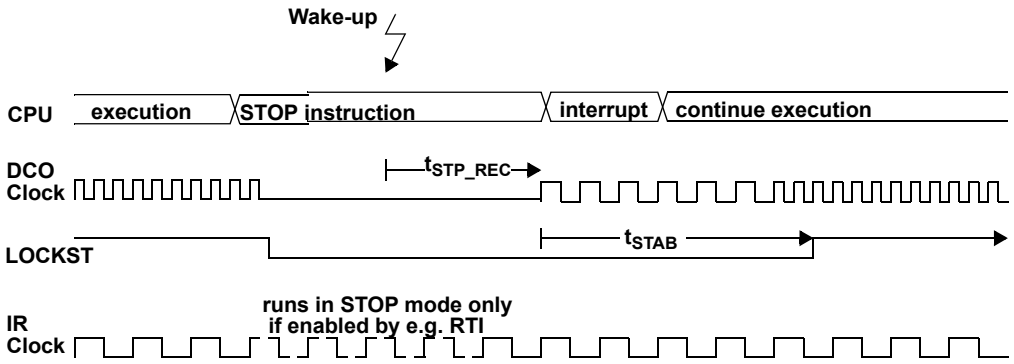


Figure 72. Example of STOP Mode Using DCO Clock as Bus Clock

4.32.4.3 Stop Mode Using Oscillator Clock as Bus Clock

An example of what happens going into stop mode and exiting stop mode after an interrupt is shown in Figure 73.

4.34.7.2 Modification of Prescaler rate (RTIRT bits)

Applications which modify the Frequency Divider Rate by modifying the RTIRT bits (Prescaler rate) in the RTICTL register should follow below recommendations.

If the Frequency Divider Rate is set lower or equal to three the RTI interrupt service routine accesses the RTICTL register with in a timing window which is less or equal the synchronization delay. Hence the interrupt service routine accessing the RTICTL register to clear the RTIF bit is executed with such frequency, the RTIRT bits are permanently locked. Therefore the following sequence is recommended if RTIRT bits should be changed for a current selected Frequency Divider Rate of two or three:

- Access the RTICTL register to clear the RTI interrupt flag (RTIF bit) and disable the RTI interrupt (clear RTIE bit) by a single write access.
- Execute a software loop in which the RTICTL register is written to modify the RTIRT bits until the new Frequency Divider Rate is taken (read back value of RTIRT bits equals new value)
- Access RTICTL register to enable RTI interrupts again.

If the actual Frequency Divider Rate of the RTI is set to a rate higher than three the write access to clear the interrupt flag (RTIF bit) in the RTICTL register can be used to modify the RTIRT bits of the RTICTL register.

4.34.7.3 Modification of Modulus Down Counter Rate (RTICNT register)

Applications which frequently access the RTICNT register should follow below recommendations. If the RTICNT register is accessed with in a timing window which is less or equal the synchronization delay the following sequence is recommended:

- Access the RTICTL register to clear the RTI interrupt flag (RTIF bit) and disable the RTI interrupt (clear RTIE bit) by a single write access.
- Execute a software loop in which the RTICNT register is written to modify the rate until the new Frequency Divider Rate is taken (read back value of RTICNT bits equals new value)
- Access RTICTL register to enable RTI interrupts again.

If the RTICNT register is accessed in a timing window which is higher than the synchronization delay, only the RTICNT register needs to be written and wait until next time-out occurs.

4.35 Computer Operating Properly (S12SCOPV1)

4.35.1 Introduction

This section describes the functionality of the Computer Operating Properly module (COP), a sub-block of the HCS12S core platform.The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. If the COP times out a system reset is initiated. Two types of COP operation are available: Window COP or Normal COP

When COP is enabled, sequential writes of $55 and $AA (in this order) are expected to the ARMCOP register during the selected timeout period. Once this is done, the COP timeout period restarts. If the program fails to do this the S12SCOP initiates a reset.

4.35.1.1 Overview

A block diagram of the COP is shown in Figure 79

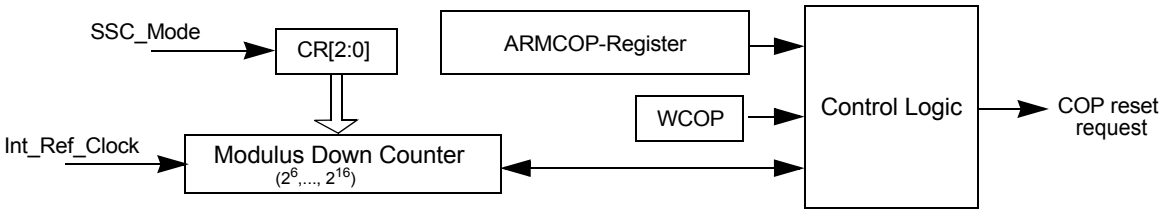


Figure 80. Block Diagram

4.36.3.3.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Table 356. Flash Security Register (FSEC)

0x0101

	7	6	5	4	3	2	1	0
R	KEYEN[1:0]		0	0	0	0	SEC[1:0]	
W								
Reset	F	F	0	0	0	0	F	F

All bits in the FSEC register are readable but are not writable.

The FSEC register is loaded from the Flash configuration field (see Section 4.36.3.1.1) during the reset sequence, indicated by F in Table 356.

Table 357. FSEC Field Descriptions

Field	Description
7:6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 358.
1:0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 359. If the Flash module is unsecured using backdoor key access, the SEC[1:0] bits are forced to the unsecured state.

Table 358. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01[193]	DISABLED
10	ENABLED
11	DISABLED

Note:
193. Preferred KEYEN state to disable Backdoor Key Access.

Table 359. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01[194]	SECURED
10	UNSECURED

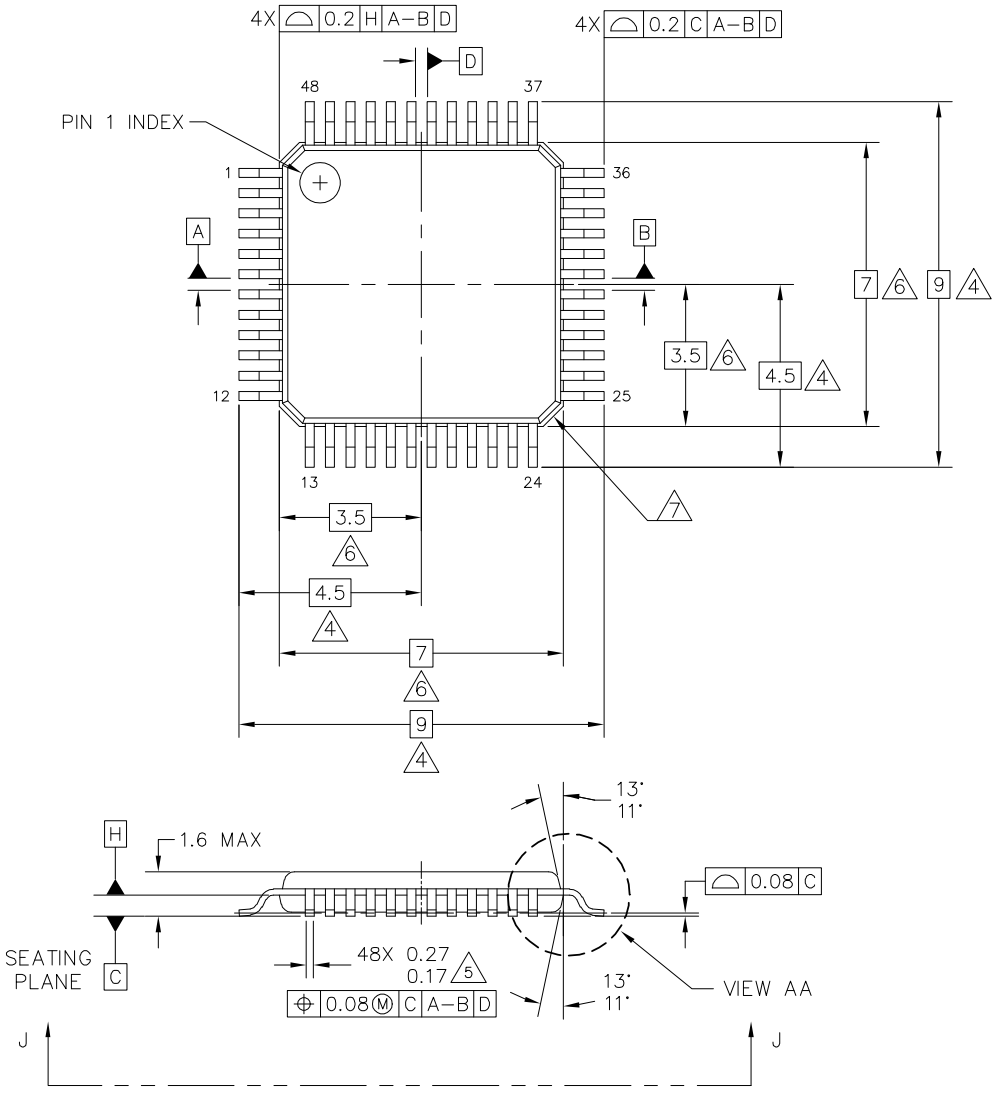
Note:
194. Preferred SEC state to set MCU to secured state.

The security feature in the Flash module is described in Section 4.36.6, “Flash Module Security".

5 Packaging

5.1 Package Dimensions

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: A
	CASE NUMBER: 2003-02	30 JUN 2011
	STANDARD: JEDEC MS-026 BBC	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.

6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.

9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA00173D	REV: A
48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	CASE NUMBER: 2003–02	30 JUN 2011
	STANDARD: JEDEC MS–026 BBC	

Revision	Date	Description
8.0	5/2015	• Changed Low-side frequency + added condition + added note guaranteed by design • Corrected typo V_{LVR} and V_{ROV} • Added Section 4.12.6, “Low-side Driver in Reverse Polarity" • Added the sentence in the general description to Section 4.25, “MM912F634 - Analog Die Trimming" • Removed the Note at beginning of 4.25.1.1 • Added explanation on SLPBG_Lock bit (4.25.1.2.3) + note to refer to errata • Added comment regarding D2D not bonded in Section 4.37.2.2, “D2DDAT[7:4]" • Added note (199) • Updated case outline • Removed the C part numbers in 1 Ordering Information (obsolete) • Reformatted document to new form and style
9.0	6/2015	• Updated the max. value for Output Drain-to-Source On resistance in Table 15 • Corrected references in Revision History • Updated module names.