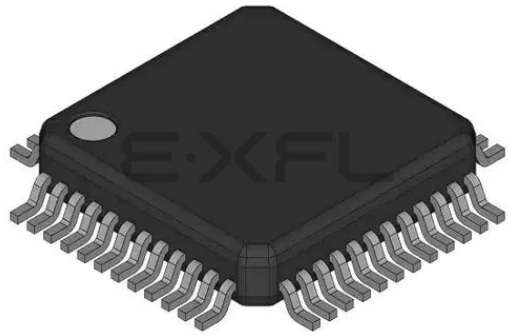

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Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (32KB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mm912f634cv1ae

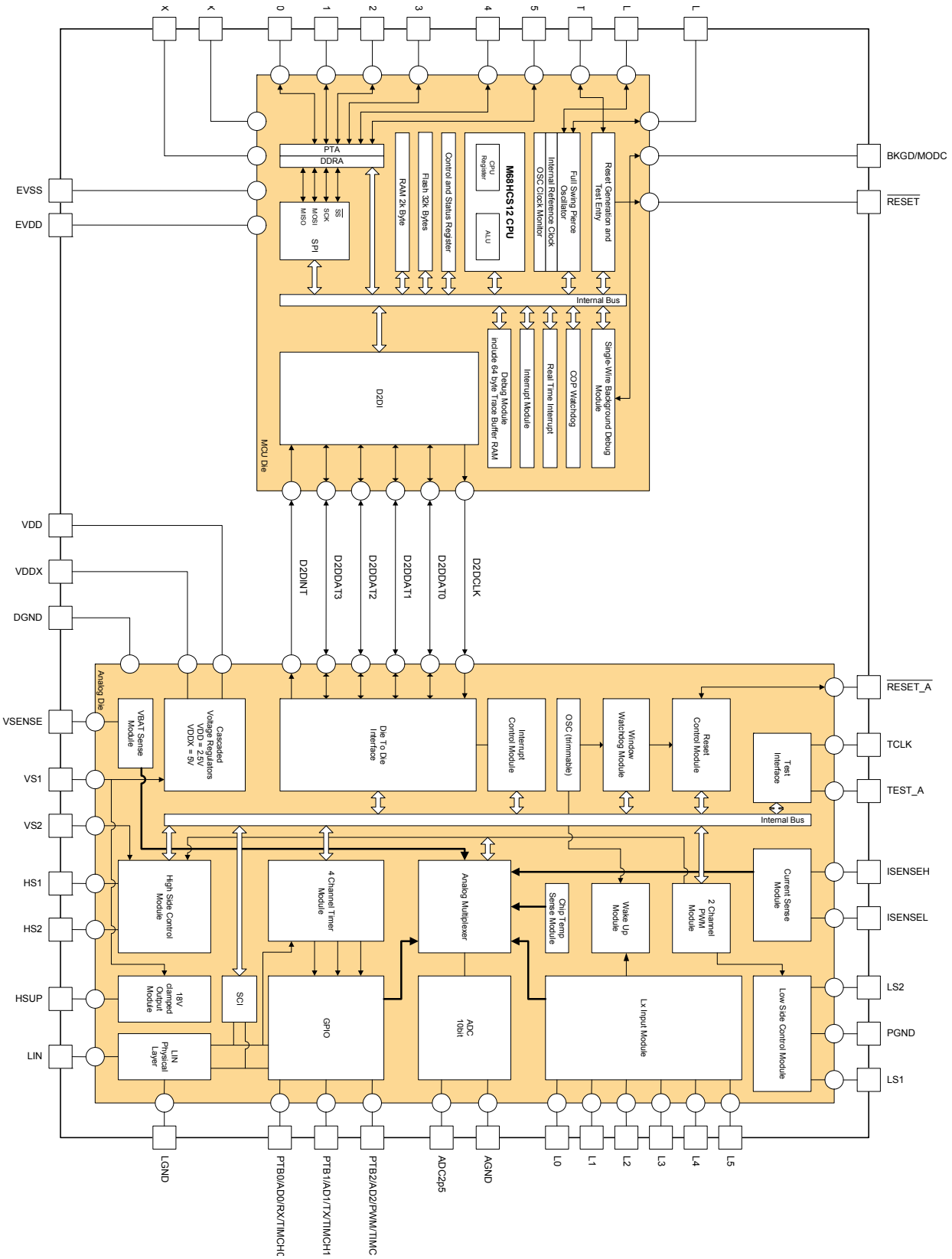


Figure 3. Device Block Diagram

Table 3. MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
36	L5	High Voltage Input 5	This pins is the High Voltage Input 5 with the following shared functions: • L5 - Digital High Voltage Input 5. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD8 - Analog Input 8 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU5 - Selectable Wake-up input 5 for wake-up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
37	LS1	Low-side Output 1	Low-side output 1 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, “Low-side Drivers - LSx".
38	PGND	Power Ground Pin	This pin is the device Low-side Ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.
39	LS2	Low-side Output 2	Low-side output 2 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, “Low-side Drivers - LSx".
40	ISENSEL	Current Sense Pins L	Current Sense differential input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 4.20, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
41	ISENSEH	Current Sense Pins H	Current Sense differential input “High”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. Section 4.20, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
42	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating.
43	TEST_A	Test Mode Pin	Analog die Test Mode pin for Test Mode only. This pin must be grounded in user mode.
44	TCLK	Test Clock Input	Test Mode Clock Input pin for Test Mode only. The pin can be used to disable the internal watchdog for development purpose in user mode. See Section 4.9, “Window Watchdog". The pin is recommended to be grounded in user mode.
45	$\overline{\text{RESET\_A}}$	Reset I/O	Bidirectional Reset I/O pin of the analog die. Active low signal. Internal pull-up. V_{DDX} based. See Section 4.7, “Resets". To be externally connected to the $\overline{\text{RESET}}$ pin.
46	$\overline{\text{RESET}}$	MCU Reset Pin	The $\overline{\text{RESET}}$ pin is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device to EVDDX.
47	BKGD	MCU Background Debug and Mode Pin	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device.
48	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating or connected to GND.

Note:
4. An optional filter capacitor C_{VSENSE} is recommended to be placed between the board connector and R_{VSENSE} to GND for increased ESD performance.
5. An optional filter capacitor C_{Lx} is recommended to be placed between the board connector and R_{Lx} to GND for increased ESD performance.

2.2 MCU Die Signal Properties

This section describes the external MCU signals. It includes a table of signal properties.

Table 4. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
EXTAL	—	V_{DD}	NA	NA	Oscillator pins
XTAL	—	V_{DD}	NA	NA	
$\overline{\text{RESET}}$	—	V_{DDX}	Pull-up		External reset

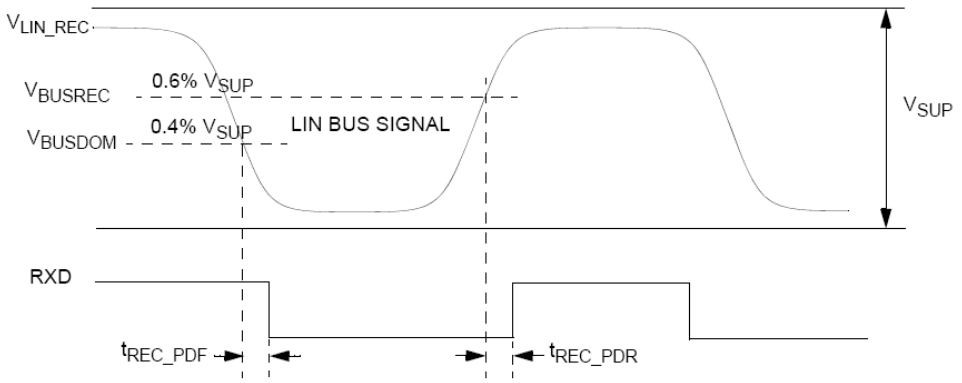


Figure 8. LIN Receiver Timing

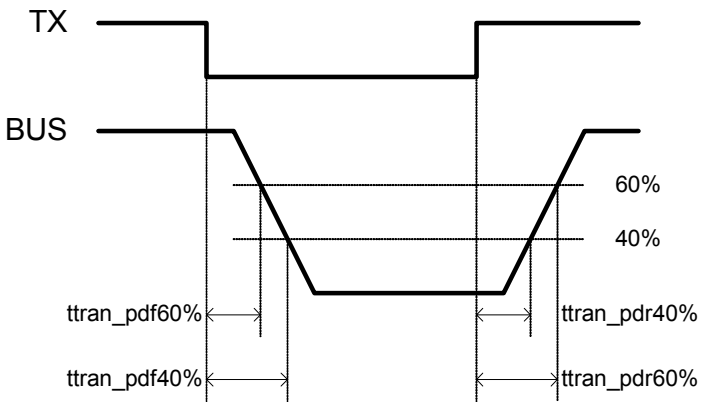


Figure 9. LIN Transmitter Timing

Table 35. Dynamic Electrical Characteristics - General Purpose I/O - PTB[0…2]

Ratings	Symbol	Min	Typ	Max	Unit
GPIO Digital Frequency[37]	f_{PTB}	-	-	10	MHz
Propagation Delay - Rising Edge[37], [38]	t_{PDR}	-	-	20	ns
Rise Time - Rising Edge[37]	t_{RISE}	-	-	17.5	ns
Propagation Delay - Falling Edge[37]	t_{PDF}	-	-	20	ns
Rise Time - Falling Edge[37]	t_{FALL}	-	-	17.5	ns

Note:
37. Guaranteed by design.
38. Load PTBx = 100 pF.

Table 51. 0x0020–0x002F Debug Module (S12XDBG) (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x002E	DBGADHM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002F	DBGADLM	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

Note:
60. This bit is visible at DBGCNT[7] and DBGSR[7]
61. This represents the contents if the Comparator A control register is blended into this address.
62. This represents the contents if the Comparator B control register is blended into this address.
63. This represents the contents if the Comparator C control register is blended into this address.

Table 52. 0x0030–0x0033 Module Mapping Control (S12SMMC)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0030	PPAGE	R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
		W								
0x0031	DIRECT	R	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
		W								
0x0032	MODE	R	MODC	0	0	0	0	0	0	0
		W								
0x0033	MMCCTL1	R	0	0	0	0	0	0	0	IFRON
		W								

Table 53. 0x0034–0x003B Clock and Reset Generator (CRG)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0034	CRGCTL0	R	OSCEN	RDIV[2:0]			BCLKS	REFS	OSC4MHZ	0
		W								
0x0035	CRGCTL1	R	BDIV[3:0]				0	0	LOCKIE	
		W								
0x0036	CRGMULT	R		MULT[6:0]						
		W								
0x0037	CRGFLG	R	0	PORF	0	LOCKIF	LOCKST	ILAF	UPOSC	0
		W								
0x0038	CRGTRIMH	R	0	0	0	0	0	0	0	TRIM[8]
		W								
0x0039	CRGTRIML	R	TRIM[7:0]							
		W								
0x003A	Reserved	R	0	0	0	0	0	0	0	0
		W								

4.11.7.2 High-side Status Register (HSSR)

Table 99. High-side Status Register (HSSR)

Offset[83] 0x29 Access: User read

	7	6	5	4	3	2	1	0
R	HSOTC	0	0	0	HS2CL	HS1CL	HS2OL	HS1OL
W								
Reset	0	0	0	0	0	0	0	0

Note:
83. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 100. HSSR - Register Field Descriptions

Field	Description
7 - HSOTC	High-side Overtemperature Condition present. Both drivers are turned off. Reading the register clears the HSOT interrupt flag if present. See Section 4.6, "Interrupts" for details.
3 - HS2CL	High-side 2 Current Limitation
2 - HS1CL	High-side 1 Current Limitation
1 - HS2OL	High-side 2 Open Load [84]
0 - HS1OL	High-side 1 Open Load [84]

Note:
84. When the High-side is in OFF state, the Open Load Detection function is not operating. When reading the HSSR register while the High-side is operating in PWM and is in the OFF state, the HS1OL and HS2OL bits does not indicate Open Load.

4.12 Low-side Drivers - LSx

4.12.1 Introduction / Features

These outputs are two Low-side drivers intended to drive relays (inductive loads) incorporating the following features:

- PWM capability
- Open load detection
- Current limitation
- Overtemperature shutdown (with maskable interrupt)
- Active clamp
- Independent VREG - High Voltage Shutdown

The starting polarity of each PWM channel waveform is determined by the associated PPOLx bit. If the polarity bit is one, the PWM channel output is high at the beginning of the cycle and then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

4.13.3.1.3 PWM Clock Select (PCLKx)

NOTE

Register bits PCLK0 and PCLK1 can be written anytime. If a clock select changes while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Each PWM channel has a choice of two clocks to use as the clock source for their channel, as described by the following.

4.13.3.1.4 PWM Center Align Enable (CAEx)

NOTE

Write these bits only when the corresponding channel is disabled.

The CAEx bits select either center aligned outputs or left aligned output for both PWM channels. If the CAEx bit is set to a one, the corresponding PWM output is center aligned. If the CAEx bit is cleared, the corresponding PWM output is left aligned. See Section 4.13.4.2.5, “Left Aligned Outputs" and Section 4.13.4.2.6, “Center Aligned Outputs" for a more detailed description of the PWM output modes.

4.13.3.2 PWM Prescale Clock Select Register (PWMPRCLK)

NOTE

PCKB2–0 and PCKA2–0 register bits can be written anytime. If the clock pre-scale is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

This register selects the prescale clock source for clocks A and B independently.

Table 112. PWM Prescale Clock Select Register (PWMPRCLK)

Offset[91] 0x61 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
W								
Reset	0	0	0	0	0	0	0	0

Note:
91. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 113. PWMPRCLK - Register Field Descriptions

Field	Description
6–4 PCKB[2:0]	Prescaler Select for Clock B — Clock B is one of two clock sources which can be used for channel 1. These three bits determine the rate of clock B, as shown in Table 114.
2–0 PCKA[2:0]	Prescaler Select for Clock A — Clock A is one of two clock sources which can be used for channel 0. These three bits determine the rate of clock A, as shown in Table 115.

Table 114. Clock B Prescaler Selects

PCKB2	PCKB1	PCKB0	Value of Clock B
0	0	0	D2D clock
0	0	1	D2D clock / 2
0	1	0	D2D clock / 4
0	1	1	D2D clock / 8
1	0	0	D2D clock / 16

Table 114. Clock B Prescaler Selects (continued)

PCKB2	PCKB1	PCKB0	Value of Clock B
1	0	1	D2D clock / 32
1	1	0	D2D clock / 64
1	1	1	D2D clock / 128

Table 115. Clock A Prescaler Selects

PCKA2	PCKA1	PCKA0	Value of Clock A
0	0	0	D2D clock
0	0	1	D2D clock / 2
0	1	0	D2D clock / 4
0	1	1	D2D clock / 8
1	0	0	D2D clock / 16
1	0	1	D2D clock / 32
1	1	0	D2D clock / 64
1	1	1	D2D clock / 128

4.13.3.3 PWM Scale A Register (PWMSCLA)

NOTE

When PWMSCLA = $00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

PWMSCLA is the programmable scale value used in scaling clock A to generate clock SA. Clock SA is generated by taking clock A, dividing it by the value in the PWMSCLA register and dividing it by two.

Clock SA = Clock A / (2 * PWMSCLA)

Any value written to this register causes the scale counter to load the new scale value (PWMSCLA).

Table 116. PWM Scale A Register (PWMSCLA)

Offset[92] 0x62 Access: User read/write

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Note:
92. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

4.13.3.4 PWM Scale B Register (PWMSCLB)

NOTE

When PWMSCLB = $00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

PWMSCLB is the programmable scale value used in scaling clock B to generate clock SB. Clock SB is generated by taking clock B, dividing it by the value in the PWMSCLB register and dividing it by two.

Clock SB = Clock B / (2 * PWMSCLB)

Any value written to this register causes the scale counter to load the new scale value (PWMSCLB).

4.15.3.3.2.2 Address-Mark Wake-up

When WAKE = 1, the receiver is configured for address-mark wake-up. In this mode, RWU is cleared automatically when the receiver detects a logic 1 in the most significant bit of a received character (eighth bit in M = 0 mode and ninth bit in M = 1 mode).

Address-mark wake-up allows messages to contain idle characters but requires the MSB be reserved for use in address frames. The logic 1 MSB of an address frame clears the RWU bit before the stop bit is received and sets the RDRF flag. In this case the character with the MSB set is received even though the receiver was sleeping during most of this character time.

4.15.3.4 Interrupts and Status Flags

The SCI system has three separate interrupt vectors to reduce the amount of software needed to isolate the cause of the interrupt. One interrupt vector is associated with the transmitter for TDRE and TC events. Another interrupt vector is associated with the receiver for RDRF, IDLE, RXEDGIF and LBKDIF events, and a third vector is used for OR, NF, FE, and PF error conditions. Each of these ten interrupt sources can be separately masked by local interrupt enable masks. The flags can still be polled by software when the local masks are cleared to disable generation of hardware interrupt requests.

The SCI transmitter has two status flags which optionally can generate hardware interrupt requests. Transmit data register empty (TDRE) indicates when there is room in the transmit data buffer to write another transmit character to SCID. If the transmit interrupt enable (TIE) bit is set, a hardware interrupt is requested whenever TDRE = 1. Transmit complete (TC) indicates the transmitter is finished transmitting all data, preamble, and break characters and is idle with TxD at the inactive level. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (TCIE) bit is set, a hardware interrupt is requested whenever TC = 1. Instead of hardware interrupts, software polling may be used to monitor the TDRE and TC status flags if the corresponding TIE or TCIE local interrupt masks are 0s.

When a program detects the receive data register is full (RDRF = 1), it gets the data from the receive data register by reading SCID. The RDRF flag is cleared by reading SCIS1 while RDRF = 1 and then reading SCID.

When polling is used, this sequence is naturally satisfied in the normal course of the user program. If hardware interrupts are used, SCIS1 must be read in the interrupt service routine (ISR). Normally, this is done in the ISR anyway to check for receive errors, so the sequence is automatically satisfied.

The IDLE status flag includes logic preventing it from getting set repeatedly when the RxD line remains idle for an extended period of time. IDLE is cleared by reading SCIS1 while IDLE = 1 and then reading SCID. After IDLE has been cleared, it cannot become set again until the receiver has received at least one new character and has set RDRF.

If the associated error was detected in the received character causing RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases. If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead the data along with any associated NF, FE, or PF condition is lost.

At any time, an active edge on the RxD serial data input pin causes the RXEDGIF flag to set. The RXEDGIF flag is cleared by writing a “1” to it. This function does depend on the receiver being enabled (RE = 1).

4.15.3.5 Additional SCI Functions

The following sections describe additional SCI functions.

4.15.3.5.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCIC1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCIC3. For the receiver, the ninth bit is held in R8 in SCIC3.

For coherent writes to the transmit data buffer, write to the T8 bit before writing to SCID.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to T8 again. When data is transferred from the transmit data buffer to the transmit shifter, the value in T8 is copied at the same time data is transferred from SCID to the shifter.

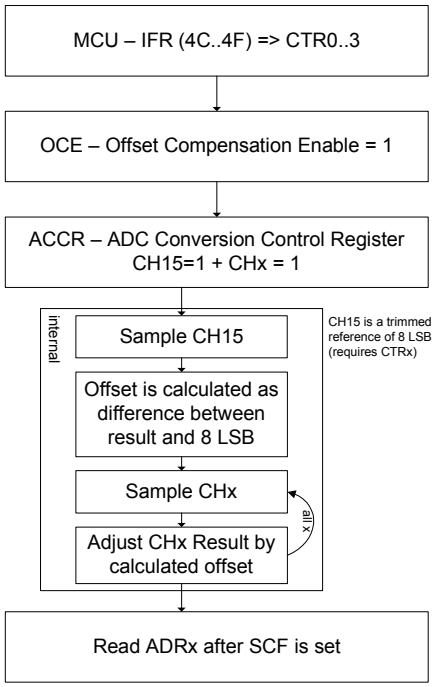


Figure 39. Automatic Offset Compensation

4.19.5.3 Conversion Timing

The conversion timing is based on the ADCCLK generated by the ADC prescaler (PS) out of the D2DCLK signal. The prescaler needs to be configured to have the ADCCLK match the specified f_{ADC} clock limits. A conversion is divided into the following 27+ clock cycles:

- 9 cycle sampling time
- 18 cycle remaining conversion time
- A worst case (only channel 14) of 15 clock cycles to count up to the selected channel (15, 0, 1,....14)
- 4 cycles between two channels

Example 1. Single Conversion Channel 10 (VSENSE)

12c (count up to Ch10) + 9c (sample) + 18c (conversion) = 39 cycles from start to end of conversion.

Example 2. Sequence of Channel 10 (VSENSE) + Channel 15 (Offset Compensation)

1c (count) + 9c (sample Ch15) + 18c (conversion Ch15) + 4c (in between) + 0c (count further to Ch10 is performed while converting ch15) + 9c (sample) + 18c (conversion) = 59 cycles from start to end of both conversions.

4.20 Current Sense Module - ISENSE

The Current Sense Module is implemented to amplify the voltage drop across an external shunt resistor to measure the actual application current using the internal Analog Digital Converter Channel 9. Typical application is the motor current in a window lift control module

4.27.3.4 PIM Reserved Register

Table 222. PIM Reserved Register

Address 0x0003 Access: User read(161)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Note:
161. Read: Anytime.
Write: Unimplemented. Writing to this register has no effect.

4.27.3.5 Port C Data Register (PTC)

Table 223. Port C Data Register (PTC)

Address 0x0004 Access: User read/write(162)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PTC1	PTC0
W								
D2DI Function	—	—	—	—	—	—	D2DINT	D2DCLK
Reset	0	0	0	0	0	0	0	0

Note:
162. Read: Anytime.
Write: Anytime.

Table 224. PTC Register Field Descriptions

Field	Description
1 PTC	**Port C general purpose input/output data**—Data Register Port C pin 1 is associated with the D2DINT signal of the D2DI module. When not used with the alternative function, this pin can be used as general purpose I/O. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.
0 PTC	**Port C general purpose input/output data**—Data Register Port C pin 0 is associated with the D2DCLK signal of the D2DI module. When not used with the alternative function, this pin can be used as general purpose I/O. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.

4.30.3.2.3 BDM Program Page Index Register (BDMPPR)

Table 257. BDM Program Page Register (BDMPPR)

Register Global Address 0x3_FF08	7	6	5	4	3	2	1	0
R	BPAE	0	0	0	BPP3	BPP2	BPP1	BPP0
W								
Reset	0	0	0	0	0	0	0	0

Read: All modes through BDM operation when not secured
Write: All modes through BDM operation when not secured

Table 258. BDMPPR Field Descriptions

Field	Description
7 BPAE	**BDM Program Page Access Enable Bit** — BPAE enables program page access for BDM hardware and firmware read/write instructions. The BDM hardware commands used to access the BDM registers (READ_BD and WRITE_BD), and cannot be used for global accesses even if the BGAE bit is set. 0 BDM Program Paging disabled 1 BDM Program Paging enabled
3–0 BPP[3:0]	**BDM Program Page Index Bits 3–0** — These bits define the selected program page. For more detailed information regarding the program page window scheme, refer to the S12S_MMC Block Guide.

4.30.3.3 Family ID Assignment

The family ID is a 8-bit value located in the firmware ROM (at global address: 0x3_FF0F). The read-only value is a unique family ID which is 0xC2 for devices with HCS12S core.

4.30.4 Functional Description

The BDM receives and executes commands from a host via a single wire serial interface. There are two types of BDM commands: hardware and firmware commands.

Hardware commands are used to read and write target system memory locations and to enter active background debug mode, see Section 4.30.4.3, “BDM Hardware Commands". Target system memory includes all memory accessible by the CPU.

Firmware commands are used to read and write CPU resources and to exit from active background debug mode, see Section 4.30.4.4, “Standard BDM Firmware Commands". The CPU resources referred to are the accumulator (D), X index register (X), Y index register (Y), stack pointer (SP), and program counter (PC).

Hardware commands can be executed at any time and in any mode excluding a few exceptions as highlighted (see Section 4.30.4.3, “BDM Hardware Commands"), and in secure mode (see Section 4.30.4.1, “Security"). Firmware commands can only be executed when the system is not secure and is in active background debug mode (BDM).

4.30.4.1 Security

If the user resets into special single-chip mode with the system secured, a secured mode BDM firmware lookup table is brought into the map overlapping a portion of the standard BDM firmware lookup table. The secure BDM firmware verifies the on-chip EEPROM and Flash EEPROM are erased. This being the case, the UNSEC and ENBDM bit gets set. The BDM program jumps to the start of the standard BDM firmware and the secured mode BDM firmware is turned off and all BDM commands are allowed. If the EEPROM or Flash do not verify as erased, the BDM firmware sets the ENBDM bit, without asserting UNSEC, and the firmware enters a loop. This causes the BDM hardware commands to become enabled, but does not enable the firmware commands. This allows the BDM hardware to be used to erase the EEPROM and Flash.

This register is visible at 0x0027 only with COMRV[1:0] = 10. The state control register three selects the targeted next state whilst in State3. The matches refer to the match channels of the comparator match control logic as depicted in Figure 67 and described in Section 4.31.3.2.8.1, "Debug Comparator Control Register (DBGXCTL)". Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 288. DBGSCR3 Field Descriptions

Field	Description
2–0 SC[2:0]	These bits select the targeted next state whilst in State3, based upon the match event.

Table 289. State3 — Sequencer Next State Selection

SC[2:0]	Description
000	Match0 to State1
001	Match2 to State2..... Match1 to Final State
010	Match0 to Final State.....Match1 to State1
011	Match1 to Final State..... Match2 to State1
100	Match1 to State2
101	Match1 to Final State
110	Match2 to State2..... Match0 to Final State
111	Match0 to Final State

The priorities described in Table 314 dictate in the case of simultaneous matches, the match on the lower channel number (0,1,2) has priority. The SC[2:0] encoding ensures a match leading to final state has priority over all other matches.

4.31.3.2.7.4 Debug Match Flag Register (DBGMFR)

Table 290. Debug Match Flag Register (DBGMFR)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	MC2	MC1	MC0
W								
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 11
Write: Never

DBGMFR is visible at 0x0027 only with COMRV[1:0] = 11. It features 3 flag bits each mapped directly to a channel. Should a match occur on the channel during the debug session, then the corresponding flag is set and remains set until the next time the module is armed by writing to the ARM bit. Thus the contents are retained after a debug session for evaluation purposes. These flags cannot be cleared by software, they are cleared only when arming the module. A set flag does not inhibit the setting of other flags. Once a flag is set, further comparator matches on the same channel in the same session have no affect on that flag.

4.31.3.2.8 Comparator Register Descriptions

Each comparator has a bank of registers visible through an 8-byte window in the DBG module register address map. Comparator A consists of 8 register bytes (3 address bus compare registers, two data bus compare registers, two data bus mask registers and a control register). Comparator B consists of four register bytes (three address bus compare registers and a control register). Comparator C consists of four register bytes (three address bus compare registers and a control register).

Table 330. CRGFLG Field Descriptions (continued)

Field	Description
2 ILAF	**Illegal Address Reset Flag** — ILAF is set to 1 when an illegal address access occurs. Refer to MMC Block Guide for details. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Illegal address access has not occurred. 1 Illegal address access has occurred.
1 UPOSC	**Oscillator Startup Status Bit** — UPOSC is set when startup of the oscillator has finished successfully. The oscillator requires a startup time t_{UPOSC}. See Electrical Characteristics for a value. Note that the Oscillator Clock can only be selected as Bus Clock source (BCLKS bit) or FLL Reference Clock (REFS bit) if UPOSC = 1. If despite enabling the Oscillator (OSCEN = 1), the UPOSC flag is not set within t_{UPOSC}, this indicates e.g. a crystal failure. Note that the Oscillator Monitor becomes active **after** initial oscillator startup, is only for UPOSC=1. UPOSC is cleared with disabling the Oscillator, which is either OSCEN = 0 or entering Stop mode. Writes have no effect. 0 Oscillator has not started up. Oscillator Monitor is inactive. 1 Oscillator has started up. Oscillator Monitor is active.

4.32.3.2.5 9S12I32PIMV1TRIM register (CRGTRIMH, CRGTRIML)

This registers contains the trimmed value for the Internal Reference Clock

Table 331. 9S12I32PIMV1 TRIM Register High Byte (CRGTRIMH)

0x0038

	15	14	13	12	11	10	9	8
R	0	0	0	0	0	0	0	TRIM[8]
W								
Reset	0	0	0	0	0	0	0	F

After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference Frequency f_{IREF_TRIM}.

Table 332. 9S12I32PIMV1 Trim Register Low Byte (CRGTRIML)

0x0039

	7	6	5	4	3	2	1	0
R W	TRIM[7:0]							
Reset	F	F	F	F	F	F	F	F

After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference frequency f_{IREF_TRIM}.

Read: Anytime
Write: Anytime

Writing the CRGTRIMH or CRGTRIML register clears the LOCKST bit, but does not set the LOCKIF bit in the CRGFLG register.

Table 333. CRGTRIMH and CRGTRIML Field Descriptions

Field	Description
8, 7, 6, 5, 4, 3, 2, 1, 0 TRIM[8:0]	Trim Bits for Internal Reference Clock After System Reset, the factory programmed trim value is automatically loaded into this register, resulting in a Internal Reference Frequency f_{IREF_TRIM}. See Electrical Characteristics for value of f_{IREF_TRIM}. The TRIM[8:0] bits are binary weighted (i.e., bit 1 adjusts twice as much as bit 0). Decreasing the binary value in TRIM[8:0] increases the frequency, increasing the value decreases the frequency. Trimmed frequency must be in the allowed range for f_{FLLREF}. See device electrical characteristics for details.

4.33.3 Modes of Operation

The OSCFSP contains the registers and associated bits for controlling and monitoring the oscillator module. Two modes of operation exist:

1. Off (OSCEN=0)
2. Full swing Pierce oscillator (OSCEN=1)

4.33.4 Block Diagram

Figure 76 shows a block diagram of the OSCFSP module.

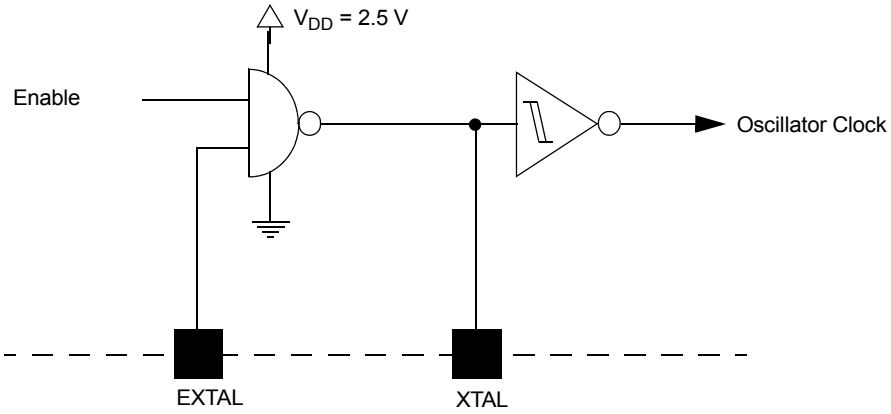


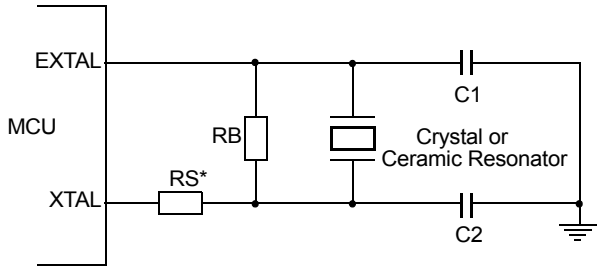
Figure 76. OSCFSP Block Diagram

4.33.5 External Signals EXTAL and XTAL — Input and Output Pins

NOTE

Freescale recommends an evaluation of the application board, and chosen resonator or crystal, by the resonator or crystal supplier. The oscillator circuit is not suited for overtone resonators and crystals.

EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier.



* R_S can be zero (shorted) when use with higher frequency crystals. Refer to manufacturer's data.

Figure 77. Full Swing Pierce Oscillator Connections

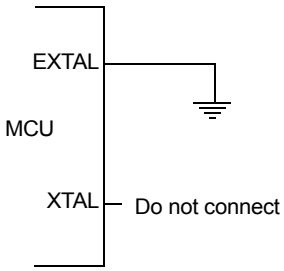


Figure 78. External Connections, if OSCFSP is Unused

The circuit shown in Figure 77 is recommended when using either a crystal or a ceramic resonator. If OSCFSP is not used, it is recommended to pull the EXTAL input pin to GND, as shown in Figure 78. In Off mode the XTAL output is forced to V_{DD} by the MCU.

4.34 Real Time Interrupt (S12SRTIV1)

4.34.1 Introduction

This section describes the functionality of the Real Time Interrupt module (RTI), a sub-block of the HCS12S core platform. The RTI (free running real time interrupt) enables the user to generate a hardware interrupt at a fixed periodic rate. If RTI is enabled, the interrupt occurs at the rate selected by the RTICTL and RTICNT register.

The RTI counter is clocked by the internal reference clock. At the end of the RTI timeout period the RTIF flag is set to one and a new RTI timeout period starts immediately.

The RTI contains two asynchronous clock domains (one for the Modulus Down Counter/Prescaler and one for the register bank). Information exchange between both clock domains is fully synchronized. Therefore modification of the RTI timeout period must be done in appliance to the write protection rules.

4.34.2 Overview

A block diagram of the RTI is shown in Figure 79

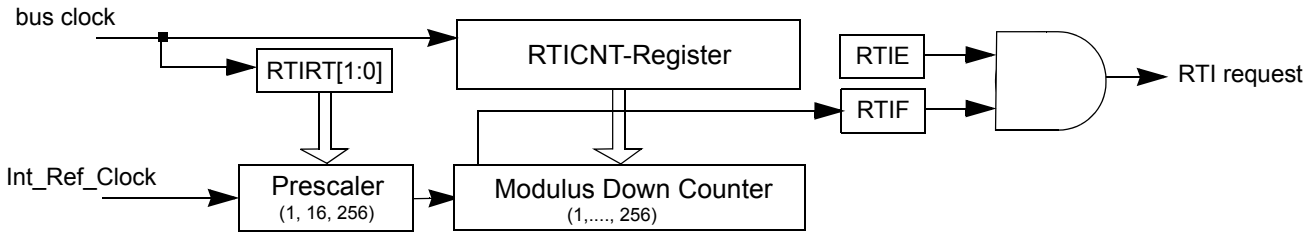


Figure 79. Block Diagram

4.34.3 Features

The RTI includes these distinctive features:

- Generate hardware interrupt at a fixed periodic rate
- Software selectable RTI operation in WAIT and STOP mode
- Software selectable RTI freeze during BDM active mode

Table 350. Initial WCOP Configuration

NV[3] in FCTL Register	WCOP in COPCTL Register
1	0
0	1

4.36 32 kbyte Flash Module (S12SFTSR32KV1)

4.36.1 Introduction

This document describes the S12SFTSR32K module, which includes a 32 kbyte Flash (nonvolatile) memory.

CAUTION

A Flash block address must be in the erased state before being programmed. Cumulative programming of bits within a Flash block address is not allowed, except for status field updates required in EEPROM emulation applications.

The Flash memory is ideal for single-supply applications, allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller which executes commands to modify Flash memory contents.

Array read access time is one bus cycle for bytes and aligned words, and two bus cycles for misaligned words. For Flash memory, an erased bit reads 1 and a programmed bit reads 0. It is not possible to read from a Flash block while any command is executing on a specific Flash block.

4.36.1.1 Glossary

Command Write Sequence — A three step MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

Flash Array — The Flash array constitutes the main memory portion of a Flash block.

Flash Block — An analog block consisting of the Flash array and Flash IFR with supporting high voltage and parametric test circuitry.

Flash IFR — Nonvolatile information memory, consisting of 128 bytes, located in the Flash block outside of Flash main memory. Refer to the SoC Guide on how to make the Flash IFR visible in the global memory map.

4.36.1.2 Features

- 32 kbytes of Flash memory comprised of one 32 kbyte block divided into 64 sectors of 512 bytes
- Nonvolatile information memory (Flash IFR) comprised of one 128 byte block
- Automated program and erase algorithm
- Interrupt on Flash command completion, command buffer empty
- Fast program and sector erase operation
- Burst program command for faster Flash array program times
- Flexible protection scheme to prevent accidental program or erase
- Single power supply for all Flash operations including program and erase
- Security feature to prevent unauthorized access to the Flash memory

4. Wait for the CCIF flag in the FSTAT register to set signifying completion of the sector erase operation.
5. Repeat steps 1 through 4 until all 16 sector erase pulses have been executed. Address must be in the same Flash sector.

If a Flash sector to be erased is in a protected area of the Flash block, the PVIOL flag in the FSTAT register sets and the sector erase command does not launch. Once the sector erase command has successfully launched, the CCIF flag in the FSTAT register sets after the sector erase operation has completed.

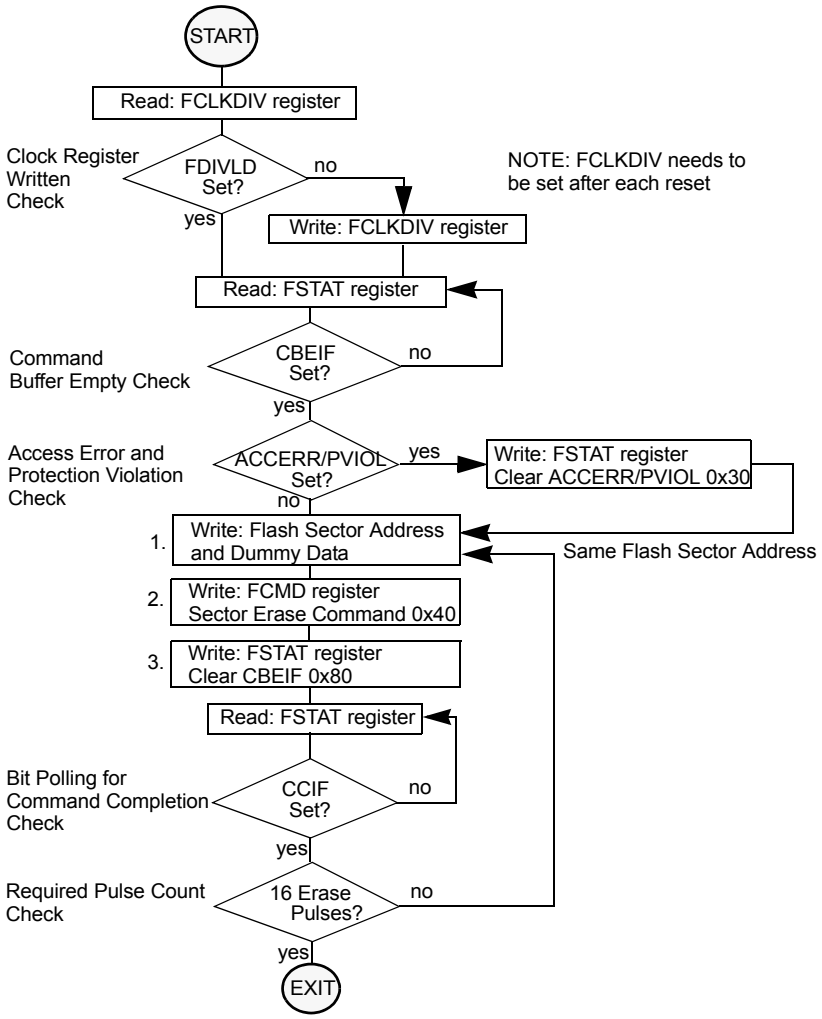


Figure 87. Example Sector Erase Command Flow

4.36.4.2.5 Mass Erase Command

The mass erase operation erases the entire Flash array memory using an embedded algorithm. An example flow to execute the mass erase operation is shown in Figure 88. The mass erase command write sequence is as follows:

1. Write to an aligned Flash block address to start the command write sequence for the mass erase command. The address and data written are ignored.
2. Write the mass erase command, 0x41, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the mass erase command.

If the Flash array memory to be mass erased contains any protected area, the PVIOL flag in the FSTAT register sets and the mass erase command does not launch. Once the mass erase command has successfully launched, the CCIF flag in the FSTAT register sets after the mass erase operation has completed.

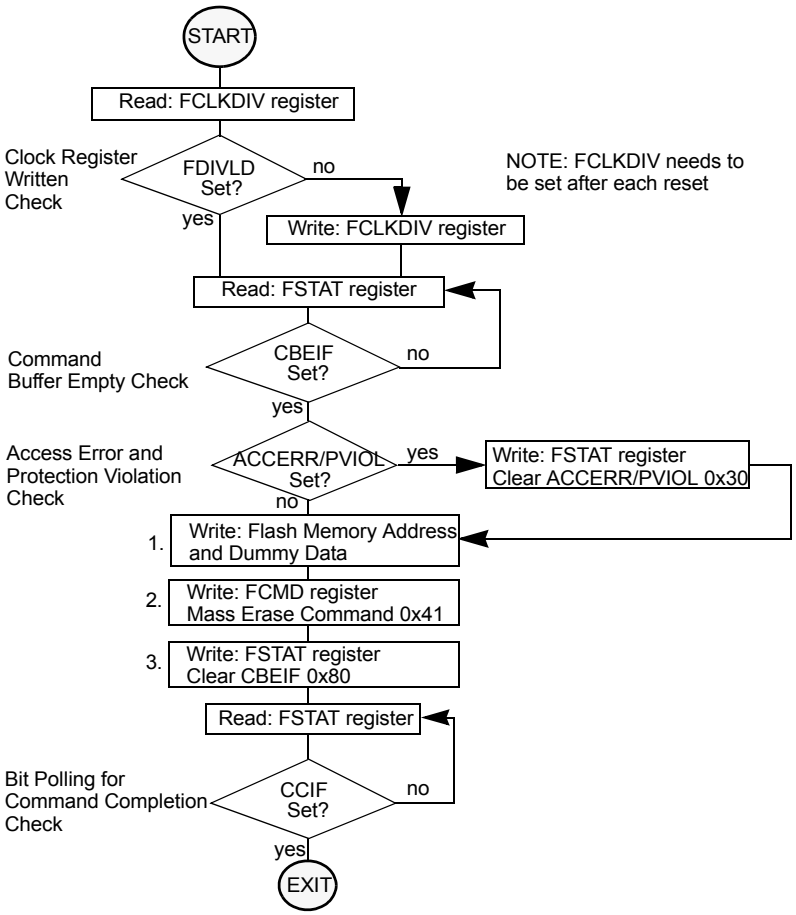


Figure 88. Example Mass Erase Command Flow

4.36.4.2.6 Set Verify Margin Level Command

The set verify margin level operation, available only in special mode, sets the margin level in the Flash array sense-amps to allow content validation with margin to the normal level for subsequent Flash array reads. The set verify margin level command should only be used to validate initial programming of the Flash array.

An example flow to execute the set verify margin level operation is shown in Figure 89. The set verify margin level command write sequence is as follows:

1. Write to an aligned Flash block address to start the command write sequence for the set verify margin level command. The address is ignored while the data written sets the margin level as shown in Table 389.
2. Write the set verify margin level command, 0x75, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the set verify margin level command.

Once the set verify margin level command has successfully launched, the CCIF flag in the FSTAT register sets after the set verify margin level operation has completed.

Table 389. Flash Array Margin Level Settings

Command Data Field	Margin Level Setting	Description
0x0000	Normal	Sets normal level for Flash array reads
0x0005	Margin 0	Sets test level to validate margin to reading 0's
0x0024	Margin 1	Sets test level to validate margin to reading 1's

Table 407. SPICR1 Field Descriptions

Field	Description
7 SPIE	**SPI Interrupt Enable Bit** — This bit enables SPI interrupt requests, if the SPIF or MODF status flag is set. 0 SPI interrupts disabled. 1 SPI interrupts enabled.
6 SPE	**SPI System Enable Bit** — This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, SPI is disabled and forced into idle state, status bits in SPISR register are reset. 0 SPI disabled (lower power consumption). 1 SPI enabled, port pins are dedicated to SPI functions.
5 SPTIE	**SPI Transmit Interrupt Enable** — This bit enables SPI interrupt requests, if the SPTEF flag is set. 0 SPTEF interrupt disabled. 1 SPTEF interrupt enabled.
4 MSTR	**SPI Master/Slave Mode Select Bit** — This bit selects whether the SPI operates in master or slave mode. Switching the SPI from master to slave or vice versa forces the SPI system into idle state. 0 SPI is in slave mode. 1 SPI is in master mode.
3 CPOL	**SPI Clock Polarity Bit** — This bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. In master mode, a change of this bit aborts a transmission in progress and force the SPI system into idle state. 0 Active-high clocks selected. In idle state SCK is low. 1 Active-low clocks selected. In idle state SCK is high.
2 CPHA	**SPI Clock Phase Bit** — This bit is used to select the SPI clock format. In master mode, a change of this bit aborts a transmission in progress and force the SPI system into idle state. 0 Sampling of data occurs at odd edges (1,3,5,...,15) of the SCK clock. 1 Sampling of data occurs at even edges (2,4,6,...,16) of the SCK clock.
1 SSOE	**Slave Select Output Enable** — The $\overline{SS}$ output feature is enabled only in master mode, if MODFEN is set, by asserting the SSOE as shown in Table 408. In master mode, a change of this bit aborts a transmission in progress and force the SPI system into idle state.
0 LSBFE	**LSB-First Enable** — This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in bit 7. In master mode, a change of this bit aborts a transmission in progress and force the SPI system into idle state. 0 Data is transferred most significant bit first. 1 Data is transferred least significant bit first.

Table 408. $\overline{SS}$ Input / Output Selection

MODFEN	SSOE	Master Mode	Slave Mode
0	0	$\overline{SS}$ not used by the SPI	$\overline{SS}$ input
0	1	$\overline{SS}$ not used by the SPI	$\overline{SS}$ input
1	0	$\overline{SS}$ input with MODF feature	$\overline{SS}$ input
1	1	$\overline{SS}$ is slave select output	$\overline{SS}$ input

4.38.3.2.2 SPI Control Register 2 (SPICR2)

Table 409. SPI Control Register 2 (SPICR2)

0x00E9

	7	6	5	4	3	2	1	0
R	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime
Write: Anytime; writes to the reserved bits have no effect

If SPIF is set and a valid byte is in the receive shift register, and SPIF is serviced before the start of a third transmission, the byte in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 98). If SPIF is set and a valid byte is in the receive shift register, and SPIF is serviced after the start of a third transmission, the byte in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 99).

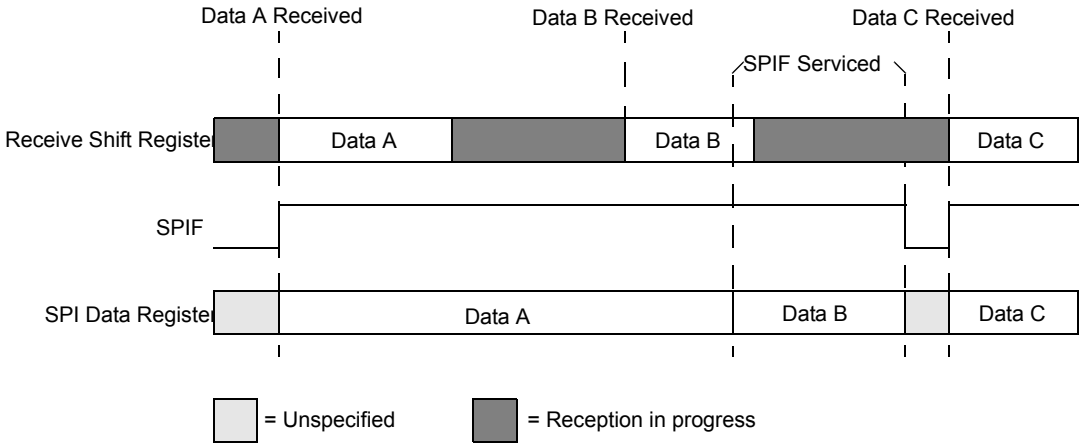


Figure 98. Reception with SPIF Serviced in Time

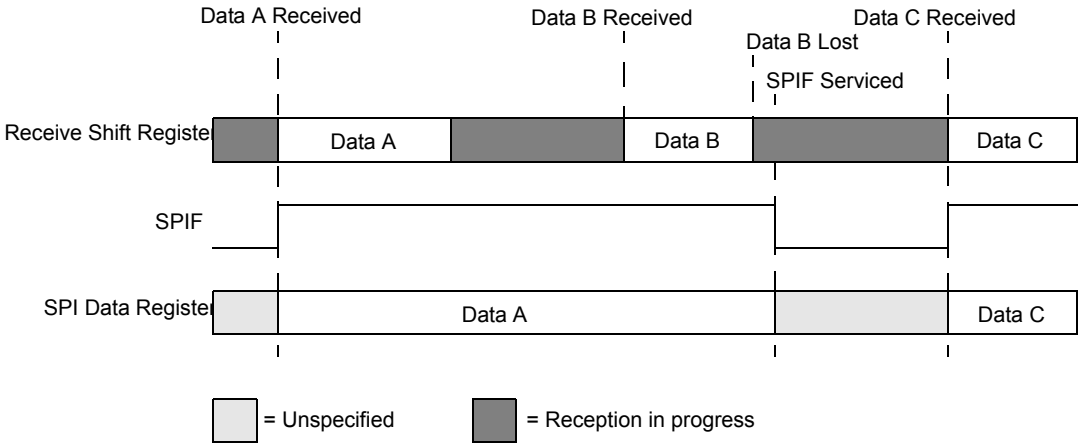


Figure 99. Reception with SPIF Serviced Too Late

4.38.4 Functional Description

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or SPI operation can be interrupt driven.

The SPI system is enabled by setting the SPI enable (SPE) bit in SPI control register 1. While SPE is set, the four associated SPI port pins are dedicated to the SPI function as:

- Slave select ($\overline{SS}$)
- Serial clock (SCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

The main element of the SPI system is the SPI data register. The 8-bit data register in the master and the 8-bit data register in the slave are linked by the MOSI and MISO pins to form a distributed 16-bit register. When a data transfer operation is performed, this 16-bit register is serially shifted eight bit positions by the S-clock from the master, so data is exchanged between the master and the slave. Data written to the master SPI data register becomes the output data for the slave, and data read from the master SPI data register after a transfer operation is the input data from the slave.