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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (32KB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912f634cv1aer2

1 Ordering Information

Table 1. Ordering Information

Device [2]	Temperature Range (T_A)	Package	Max. Bus Frequency (MHz) (f_{BUSMAX})	Flash (kB)	RAM (kB)	Analog Option [1]
MM912F634DV1AE	-40 to 105 °C	98ASA00173D, 48-PIN LQFP-EP	20	32	2	1
MM912F634DV2AE						2
MM912F634DV2AP		98ASH00962A, 48-PIN LQFP	16	32		

Note:
1. See Table 2.
2. For Tape and Reel orders add R2 to the part suffix

Table 2. Analog Options[3]

Feature	Option 1	Option 2
Current Sense Module	YES	NO
Wake-up Inputs (Lx)	L0…L5	L0…L3

Note:
3. This table only highlights the analog die differences between the derivatives. See Section 4.2.3, “Analog Die Options" for detailed information.

The device part number follows the standard scheme below:

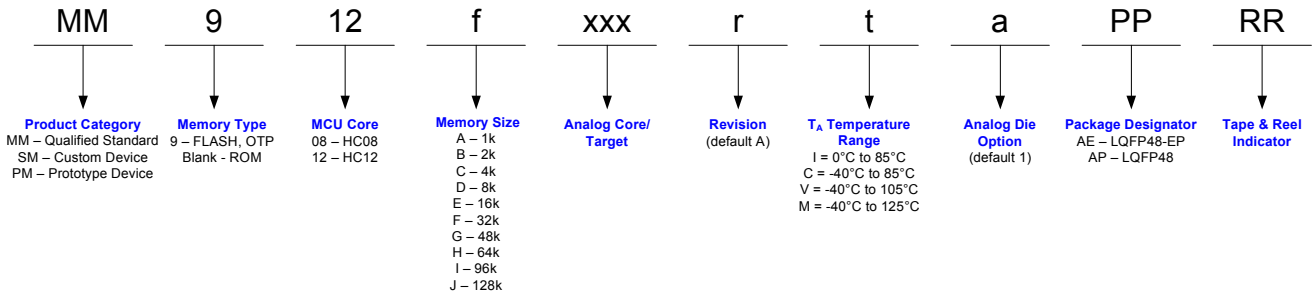

Figure 2. Part Number Scheme

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Table 3. MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
36	L5	High Voltage Input 5	This pins is the High Voltage Input 5 with the following shared functions: • L5 - Digital High Voltage Input 5. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD8 - Analog Input 8 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU5 - Selectable Wake-up input 5 for wake-up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
37	LS1	Low-side Output 1	Low-side output 1 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, “Low-side Drivers - LSx".
38	PGND	Power Ground Pin	This pin is the device Low-side Ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.
39	LS2	Low-side Output 2	Low-side output 2 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, “Low-side Drivers - LSx".
40	ISENSEL	Current Sense Pins L	Current Sense differential input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 4.20, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
41	ISENSEH	Current Sense Pins H	Current Sense differential input “High”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. Section 4.20, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
42	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating.
43	TEST_A	Test Mode Pin	Analog die Test Mode pin for Test Mode only. This pin must be grounded in user mode.
44	TCLK	Test Clock Input	Test Mode Clock Input pin for Test Mode only. The pin can be used to disable the internal watchdog for development purpose in user mode. See Section 4.9, “Window Watchdog". The pin is recommended to be grounded in user mode.
45	$\overline{\text{RESET\_A}}$	Reset I/O	Bidirectional Reset I/O pin of the analog die. Active low signal. Internal pull-up. V_{DDX} based. See Section 4.7, “Resets". To be externally connected to the $\overline{\text{RESET}}$ pin.
46	$\overline{\text{RESET}}$	MCU Reset Pin	The $\overline{\text{RESET}}$ pin is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device to EVDDX.
47	BKGD	MCU Background Debug and Mode Pin	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device.
48	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating or connected to GND.

Note:
4. An optional filter capacitor C_{VSENSE} is recommended to be placed between the board connector and R_{VSENSE} to GND for increased ESD performance.
5. An optional filter capacitor C_{Lx} is recommended to be placed between the board connector and R_{Lx} to GND for increased ESD performance.

2.2 MCU Die Signal Properties

This section describes the external MCU signals. It includes a table of signal properties.

Table 4. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
EXTAL	—	V_{DD}	NA	NA	Oscillator pins
XTAL	—	V_{DD}	NA	NA	
$\overline{\text{RESET}}$	—	V_{DDX}	Pull-up		External reset

Table 33. Dynamic Electrical Characteristics - Low-side Drivers - LS

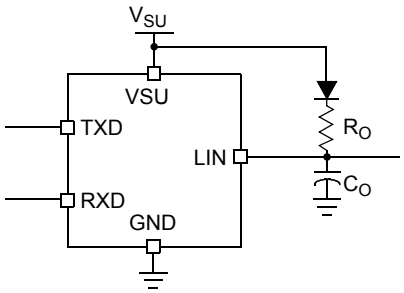
Ratings	Symbol	Min	Typ	Max	Unit
Low-side Operating Frequency[34], Load Condition: $C_{LOAD} \leq 2.2$ nF; $R_{LOAD} \geq 500\ \Omega$	f_{HS}	-	-	50	kHz

Note:
34. Guaranteed by design.

Table 34. Dynamic Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Bus Wake-up Deglitcher (Sleep and Stop Mode)	t_{PROPWL}	60	80	100	µs
Fast Bit Rate (Programming Mode)	BR_{FAST}	-	-	100	kBit/s
Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})[35]	t_{REC_PD}	-	-	6.0	µs
Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	t_{REC_SYM}	-2.0	-	2.0	µs
LIN Driver - 20.0 kBit/s; Bus load conditions (C_{BUS}; R_{BUS}): 1.0 nF; 1.0 kΩ / 6,8 nF;660 Ω / 10 nF;500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 6.					
Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, 7.0 V ≤ V_{SUP} ≤ 18 V; t_{Bit} = 50 µs;, D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{Bit})	D1	0.396	-	-	
Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, 7.6 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 50 µs, D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT})	D2	-	-	0.581	
LIN Driver - 10.0 kBit/s; Bus load conditions (C_{BUS}; R_{BUS}): 1.0 nF; 1.0 kΩ / 6,8 nF;660 Ω / 10 nF;500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 7.					
Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, 7.0 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 96 µs, D3 = $T_{BUS\_REC(MIN)}$/(2 x t_{BIT})	D3	0.417	-	-	
Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, 7.6 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 96 µs, D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT})	D4	-	-	0.590	
Transmitter Symmetry t_{TRAN_SYM} < MAX(t_{TRAN_SYM}60%, t_{TRAN_SYM}40%) tran_sym60% = ttran_pdf60% - ttran_pdr60% tran_sym40% = ttran_pdf40% - ttran_pdr40%	t_{TRAN_SYM}	-7.25	0	7.25	µs

Note:
35. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 8.
36. LIN Transmitter Timing, (V_{SUP} from 7.0 to 18 V) - See Figure 9



Note: Rn and Cn: 1.0kΩ/1.0nF, 660Ω/6.8

Figure 5. Test Circuit for Timing Measurements

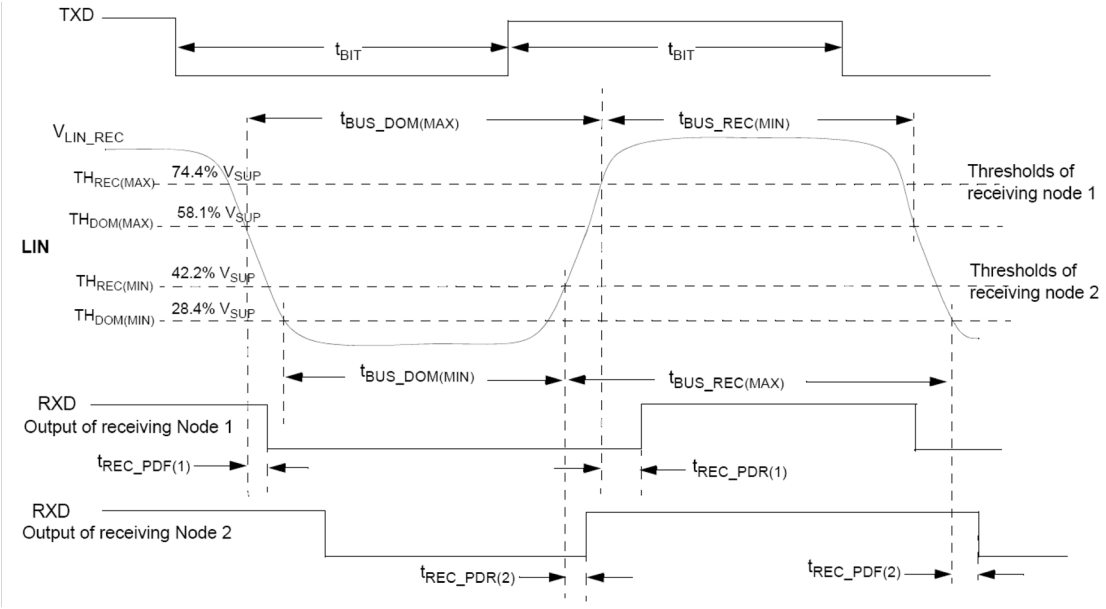


Figure 6. LIN Timing Measurements for Normal Baud Rate

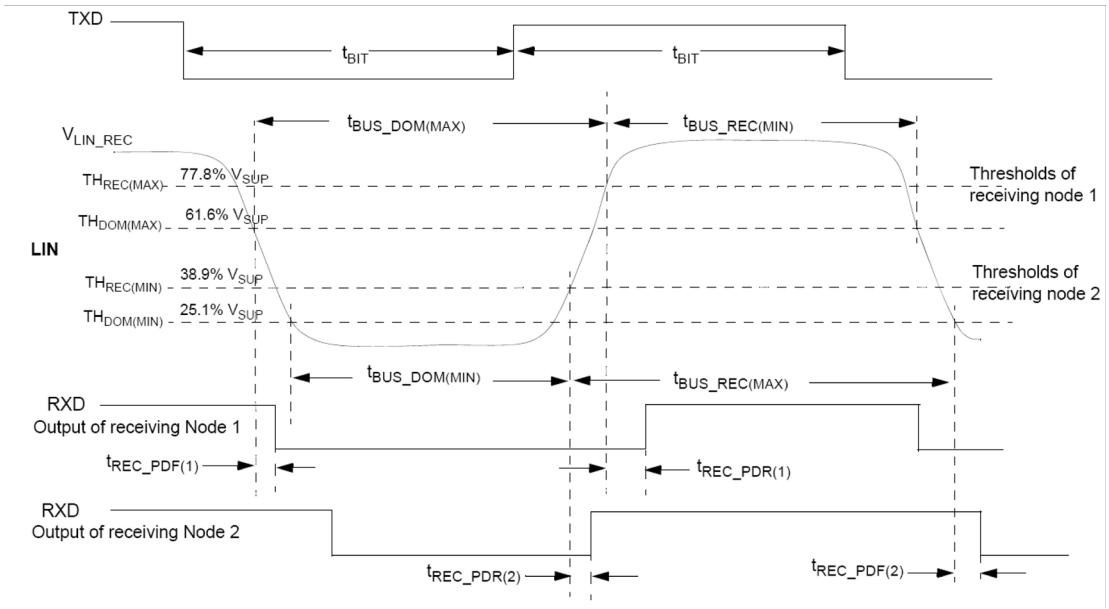


Figure 7. LIN Timing Measurements for Slow Baud Rate

Table 63. 0x0120–0x0123 Port Integration Module (PIM) 2 of 2 (continued)

0x0122	RDRA	R	0	0	RDRA5	RDRA4	RDRA3	RDRA2	RDRA1	RDRA0
		W								
0x0123	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 64. 0x0124–0x01FF Reserved Register Space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0124-0x01FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 65 shows the detailed module maps of the MM912F634 analog die.

Table 65. Analog die Registers[64] - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3

Offset	Name		7	6	5	4	3	2	1	0
0x00	ISR (hi)	R	0	0	HOT	LSOT	HSOT	LINOT	SCI	RX
	Interrupt Source Register	W								
0x01	ISR (lo)	R	TX	ERR	TOV	CH3	CH2	CH1	CH0	VSI
	Interrupt Source Register	W								
0x02	IVR	R	0	0	IRQ					
	Interrupt Vector Register	W								
0x04	VCR	R	0	0	0	VROVIE	HTIE	HVIE	LVIE	LBIE
	Voltage Control Register	W								
0x05	VSR	R	0	0	0	VROVC	HTC	HVC	LVC	LBC
	Voltage Status Register	W								
0x08	LXR	R	0	0	L5	L4	L3	L2	L1	L0
	Lx Status Register	W								
0x09	LXCR	R	0	0	L5DS	L4DS	L3DS	L2DS	L1DS	L0DS
	Lx Control Register	W								
0x10	WDR	R	WDOFF	WDWO	0	0	0	WDTO		
	Watchdog Register	W								
0x11	WDSR	R	WDSR							
	Watchdog Service Register	W								
0x12	WCR	R	CSSEL		L5WE	L4WE	L3WE	L2WE	L1WE	L0WE
	Wake Up Control Register	W								
0x13	TCR	R	FWM				CST			
	Timing Control Register	W								
0x14	WSR	R	FWU	LINWU	L5WU	L4WU	L3WU	L2WU	L1WU	L0WU
	Wake Up Source Register	W								

4.6.2.6 TIM Channel 1 Interrupt (CH1)

See Section 4.18, “Basic Timer Module - TIM (TIM16B4C)".

4.6.2.7 TIM Channel 2 Interrupt (CH2)

See Section 4.18, “Basic Timer Module - TIM (TIM16B4C)".

4.6.2.8 TIM Channel 3 Interrupt (CH3)

See Section 4.18, “Basic Timer Module - TIM (TIM16B4C)".

4.6.2.9 TIM Timer Overflow Interrupt (TOV)

See Section 4.18, “Basic Timer Module - TIM (TIM16B4C)".

4.6.2.10 SCI Error Interrupt (ERR)

See Section 4.15, “Serial Communication Interface (S08SCIV4)".

4.6.2.11 SCI Transmit Interrupt (TX)

See Section 4.15, “Serial Communication Interface (S08SCIV4)".

4.6.2.12 SCI Receive Interrupt (RX)

See Section 4.15, “Serial Communication Interface (S08SCIV4)".

4.6.2.13 LIN Driver Overtemperature Interrupt (LINOT)

Acknowledge the interrupt by reading the LIN Register - LINR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.14, “LIN Physical Layer Interface - LIN" for details on the LIN Register including masking information.

4.6.2.14 High-side Overtemperature Interrupt (HSOT)

Acknowledge the interrupt by reading the High-side Status Register - HSSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.11, “High-side Drivers - HS" for details on the High-side Status Register including masking information.

4.6.2.15 Low-side Overtemperature Interrupt (LSOT)

Acknowledge the interrupt by reading the Low-side Status Register - LSSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.12, “Low-side Drivers - LSx" for details on the Low-side Status Register including masking information.

4.6.2.16 HSUP Overtemperature Interrupt (HOT)

Acknowledge the interrupt by reading the Hall Supply Register - HSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.10, “Hall Sensor Supply Output - HSUP" for details on the Hall Supply Register including masking information.

4.6.2.17 High Voltage Interrupt (HVI)

Acknowledge the interrupt by reading the Voltage Status Register - VSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.4, “Power Supply" for details on the Voltage Status Register including masking information.

4.6.2.18 Voltage Regulator Overvoltage Interrupt (VROVI)

Acknowledge the interrupt by reading the Voltage Status Register - VSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.4, “Power Supply" for details on the Voltage Status Register including masking information.

4.7 Resets

To protect the system during critical events, the MM912F634 analog die drives the $\overline{\text{RESET\_A}}$ pin low during the presence of the reset condition. In addition, the $\overline{\text{RESET\_A}}$ pin is monitored for external reset events. To match the MCU, the $\overline{\text{RESET\_A}}$ pin is based on the VDDX voltage level.

After an internal reset condition has gone, the $\overline{\text{RESET\_A}}$ stays low for an additional time t_{RST} before being released. Entering reset mode causes all MM912F634 analog die registers to be initialized to their RESET default. The only registers with valid information are the Reset Status Register (RSR) and the Wake-up Source Register (WUS).

4.7.1 Reset Sources

In the MM912F634 six reset sources exist.

4.7.1.1 POR - Analog Die Power On Reset

To indicate the device power supply (VS1) was below V_{POR} or the MM912F634 analog die was powered up, the POR condition is set. See Section 4.3, “Modes of Operation".

4.7.1.2 LVR - Low Voltage Reset - VDD

With the VDD voltage regulator output voltage falling below V_{LVR}, the Low Voltage Reset condition becomes present. As the VDD Regulator is shutdown once a LVRX condition is detected, The actual cause could be also a low voltage condition at the VDDX regulator. See Section 4.4, “Power Supply".

4.7.1.3 LVRX - Low Voltage Reset - VDDX

With the VDDX voltage regulator output voltage falling below V_{LVRX}, the Low Voltage Reset condition becomes present. See Section 4.4, “Power Supply".

4.7.1.4 WUR - Wake-up Reset

While in Sleep mode, any active wake-up event causes a MM912F634 analog die transition from Sleep to Reset Mode. To determine the wake-up source, refer to Section 4.8, “Wake-up / Cyclic Sense".

4.7.1.5 EXR - External Reset

Any low level voltage at the $\overline{\text{RESET\_A}}$ pin with a duration > t_{RSTDF} issues an External Reset event. This reset source is also active in Stop mode.

4.7.1.6 WDR - Watchdog Reset

Any incorrect serving if the MM912F634 analog die Watchdog results in a Watchdog Reset. Refer to the Section 4.9, “Window Watchdog" for details.

4.7.2 Register Definition

4.7.2.1 Reset Status Register (RSR)

Table 83. Reset Status Register (RSR)

Offset[73] 0x15 — Access: User read

	7	6	5	4	3	2	1	0
R	0	0	WDR	EXR	WUR	LVRX	LVR	POR
W								

Note:
73. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

4.9.1 Register Definition

4.9.1.1 Watchdog Register (WDR)

Table 91. Watchdog Register (WDR)

Offset[79] 0x10 Access: User read/write

	7	6	5	4	3	2	1	0
R	WDOFF	WDWO	0	0	0	WDTO		
W								
Reset	0	0	0	0	0	0	0	0

Note:
79. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 92. WDR - Register Field Descriptions

Field	Description
7 - WDOFF	watchdog Off - Indicating the Watchdog module is being disabled externally.
6 - WDWO	Watchdog Window Open - Indicating the Watchdog Window is currently open for counter reset.
2-0 WDTO[2:0]	Watchdog Timeout Configuration - configuring the Watchdog timeout duration t_{WDTO}. 000 - 10 ms 001 - 20 ms 010 - 40 ms 011 - 80 ms 100 - 160 ms 101 - 320 ms 110 - 640 ms 111 - 1280 ms

4.9.1.2 Watchdog Service Register (WDSR)

Table 93. Watchdog Service Register (WDSR)

Offset[80] 0x11 Access: User read/write

	7	6	5	4	3	2	1	0
R	WDSR							
W								
Reset	0	1	0	1	0	1	0	1

Note:
80. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 94. WDSR - Register Field Descriptions

Field	Description
7-0 WDSR	Watchdog Service Register - Writing this register with the correct value (0xAA alternating 0x55) while the window is open resets the watchdog counter. Writing the register while the watchdog is disabled has no effect.

4.10 Hall Sensor Supply Output - HSUP

To supply Hall Effect Sensors or similar external loads, the HSUP output is implemented. To reduce power dissipation inside the device, the output is implemented as a switchable Voltage Regulator, internally connected to the VS1 supply input. For protection, an Overtemperature Shutdown and a Current Limitation is implemented. A write to the Hall Supply Register (HSR), when the overtemperature condition is gone, re-enables the Hall Supply Output. The HSUP output is active only during Normal mode. A capacitor C_{HSUP} is recommended for operation.

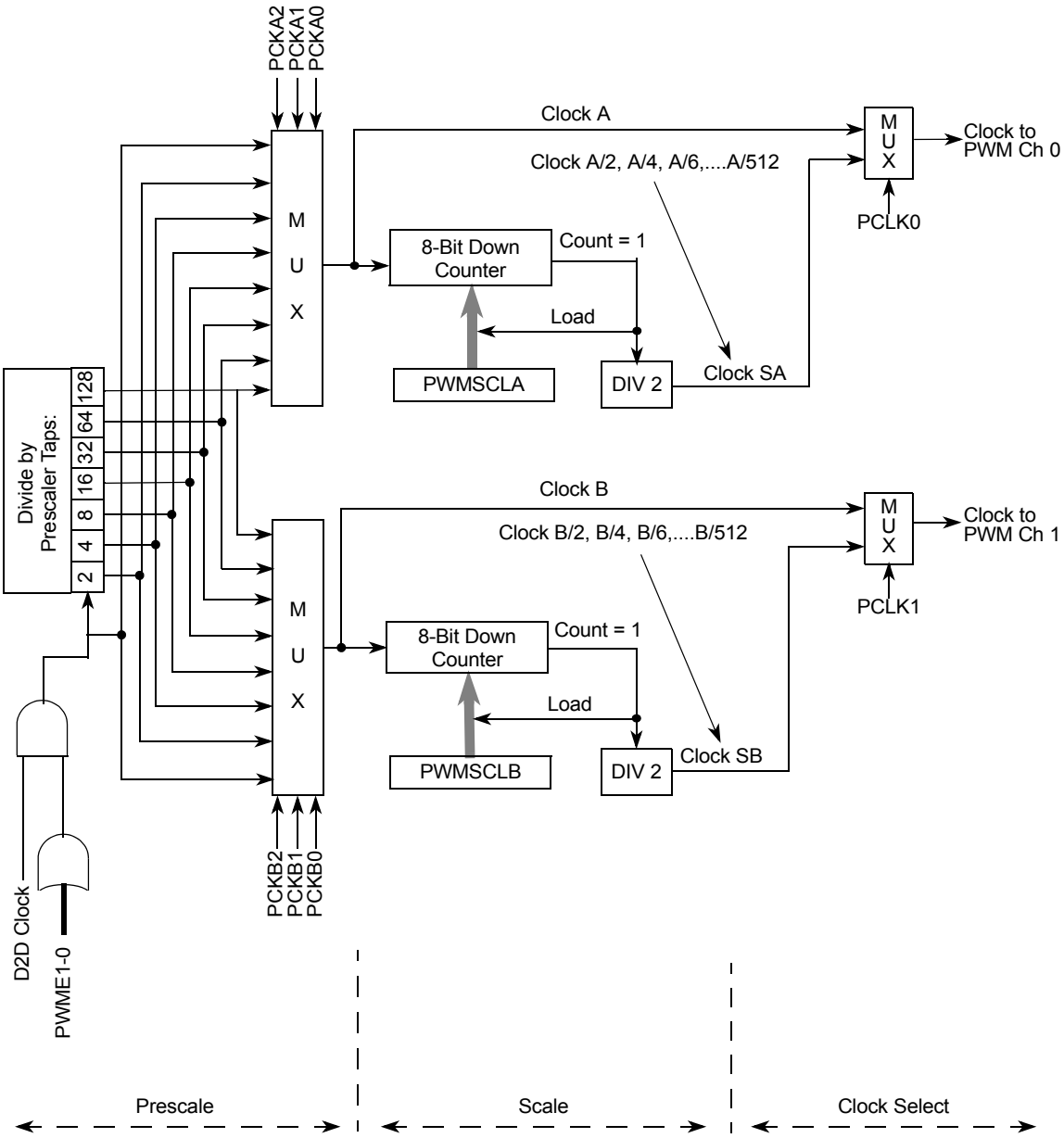


Figure 26. PWM Clock Select Block Diagram

NOTE

Clock SA = Clock A / (2 * PWMSCLA)

When PWMSCLA = $00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Clock A is used as an input to an 8-bit down counter. This down counter loads a user programmable scale value from the scale register (PWMSCLA). When the down counter reaches one, a pulse is output and the 8-bit counter is re-loaded. The output signal from this circuit is further divided by two. This gives a greater range with only a slight reduction in granularity. Clock SA equals clock A divided by two times the value in the PWMSCLA register.

NOTE

Clock SB = Clock B / (2 * PWMSCLB)

When PWMSCLB = $00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

Table 205. CTR0 - Register Field Descriptions (continued)

Field	Description
3 CTR0_3	Spare Trim bit 3
2-0 WDCTR2…0	Watchdog clock trim (Trim effect to the 100 kHz Watch dog base clock) 000: 0% 001: +5% 010: +10% 011: +15% 100: -20% 101: -15% 110: -10% 111: -5%

4.25.2.2 Trimming Register 1 (CTR1)

Table 206. Trimming Register 1 (CTR1)

Offset[148] 0xF1 Access: User read/write

	7	6	5	4	3	2	1	0
R W	BGTRE	CTR1_6	BGTRIMUP	BGTRIMDN	IREFTRE	IREFTR2	IREFTR1	IREFTR0
Reset	0	0	0	0	0	0	0	0

Note:
148. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 207. CTR1 - Register Field Descriptions

Field	Description
7 BGTRE	Bandgap trim enable 0 - no trim can be done 1 - trim can be done by setting BGTRIMUP and BGTRIMDN bits
6 CTR1_6	Spare Trim Bit
5 BGTRIMUP	Bandgap trim up bit 0 - default slope 1 - increase bandgap slope
4 BGTRIMDN	Bandgap trim down bit 0 - default slope 1 - decrease bandgap slope
3 IREFTRE	Iref trim enable bit 0 - no trim can be done 1 - trim can be done by setting IREFTR[2:0] bits
2-0 IREFTR2…0	Iref trim - This trim is used to adjust the internal zero TC current reference 000: 0% 001: +7.6% 010: +16.43% 011: +26.83% 100: -8.54% 101: -15.75% 110: -21.79% 111: 0%

4.28.1.1 Terminology

Table 238. Acronyms and Abbreviations

Logic level “1”	Voltage corresponding to the Boolean true state
Logic level “0”	Voltage corresponding to the Boolean false state
0x	Represents hexadecimal number
x	Represents logic level ’don’t care’
byte	8-bit data
word	16-bit data
local address	based on the 64 Kilobytes Memory Space (16-bit address)
global address	based on the 256 Kilobytes Memory Space (18-bit address)
Aligned address	Address on even boundary
Mis-aligned address	Address on odd boundary
Bus Clock	System Clock. Refer to CRG Block Guide.
single-chip modes	Normal Single-chip mode Special Single-chip mode
normal modes	Normal Single-chip mode
special modes	Special Single-chip mode
NS	Normal Single-chip mode
SS	Special Single-chip mode
Unimplemented areas	Areas which are accessible by the PPAGE, and not implemented
MCU	Micro-Controller Unit
NVM	Non-volatile Memory; Flash EEPROM or ROM
IFR	NVM Information Row. Refer to FTSR Block Guide

4.28.1.2 Features

The main features of this block are:

- Paging capability to support a global 256 Kilobytes memory address space
- Bus arbitration between the masters CPU, BDM to different resources (internal and peripherals). Note: resources are also called targets.
- MCU operation mode control
- MCU security control
- Separate memory map schemes for each master CPU, BDM
- Generation of system reset when CPU accesses an unimplemented address (i.e., an address which does not belong to any of the on-chip modules) in single-chip modes

4.28.1.3 S12S Memory Mapping

The S12S architecture implements one memory mapping scheme including:

- A (CPU or BDM) 64 kByte local map, defined using specific resource page (PPAGE) register and the default instruction set. The 64 Kilobytes visible at any instant can be considered as the local map accessed by the 16-bit (CPU or BDM) address.

4.28.3.2 Memory Map Scheme

4.28.3.2.1 CPU and BDM Memory Map Scheme

The BDM firmware lookup tables and BDM register memory locations share addresses with other modules. However, they are not visible in the memory map during user's code execution. The BDM memory resources are enabled only during the READ_BD and WRITE_BD access cycles to distinguish between accesses to the BDM memory area and accesses to the other modules. (Refer to BDM Block Guide for further details).

When the MCU enters active BDM mode, the BDM firmware lookup tables and the BDM registers become visible in the local memory map in the range 0xFF00-0xFFFF (global address 0x3_FF00 - 0x3_FFFF) and the CPU begins execution of firmware commands or the BDM begins execution of hardware commands. The resources which share memory space with the BDM module are not be visible in the memory map during active BDM mode.

Note that after the MCU enters active BDM mode the BDM firmware lookup tables and the BDM registers are also visible between addresses 0xBF00 and 0xBFFF if the PPAGE register contains value of 0xFF.

4.28.3.2.2 Expansion of the Local Address Map

4.28.3.2.2.1 Expansion of the CPU Local Address Map

The program page index register in MMC allows accessing up to 256 kbyte of FLASH or ROM in the global memory map by using the four page index bits to page 16x16 kbyte blocks into the program page window located from address 0x8000 to address 0xBFFF in the local CPU memory map.

The page value for the program page window is stored in the PPAGE register. The value of the PPAGE register can be read or written by normal memory accesses as well as by the CALL and RTC instructions (see Section 4.28.4.1, "CALL and RTC Instructions"). Control registers, vector space and parts of the on-chip memories are located in unpaged portions of the 64 kilobyte local CPU address space.

The starting address of an interrupt service routine must be located in unpaged memory unless the user is certain the PPAGE register is set to the appropriate value when the service routine is called. However an interrupt service routine can call other routines in paged memory. The upper 16 kilobyte block of the local CPU memory space (0xC000–0xFFFF) is unpaged. It is recommended all reset and interrupt vectors point to locations in this area or to the other unmapped pages sections of the local CPU memory map.

4.28.3.2.2.2 Expansion of the BDM Local Address Map

PPAGE and BDMPPR register is also used for the expansion of the BDM local address to the global address. These registers can be read and written by the BDM. The BDM expansion scheme is the same as the CPU expansion scheme. The four BDMPPR Program Page index bits allow access to the full 256 kbyte address map which can be accessed with 17 address bits.

The BDM program page index register (BDMPPR) is used only when the feature is enabled in BDM and, in the case the CPU is executing a firmware command which uses CPU instructions, or by a BDM hardware commands. See the BDM Block Guide for further details. (see Figure 53).

Table 265. COMRV Encoding

COMRV	Visible Comparator	Visible Register at 0x0027
00	Comparator A	DBGSCR1
01	Comparator B	DBGSCR2
10	Comparator C	DBGSCR3
11	None	DBGMFR

4.31.3.2.2 Debug Status Register (DBGSR)

Table 266. Debug Status Register (DBGSR)

Address: 0x0021

	7	6	5	4	3	2	1	0
R	TBF	0	0	0	0	SSF2	SSF1	SSF0
W								
Reset	—	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0

Read: Anytime
Write: Never

Table 267. DBGSR Field Descriptions

Field	Description
7 TBF	**Trace Buffer Full** — The TBF bit indicates the trace buffer has stored 64 or more lines of data since it was last armed. If this bit is set, then all 64 lines are valid data, regardless of the value of DBGCNT bits. The TBF bit is cleared when ARM in DBGC1 is written to a one. The TBF is cleared by the power on reset initialization. Other system generated resets have no affect on this bit. This bit is also visible at DBGCNT[7].
2–0 SSF[2:0]	**State Sequencer Flag Bits** — The SSF bits indicate in which state the State Sequencer is in currently. During a debug session on each transition to a new state these bits are updated. If the debug session is ended by software clearing the ARM bit, then these bits retain their value to reflect the last state of the state sequencer before disarming. If a debug session is ended by an internal event, then the state sequencer returns to state 0 and these bits are cleared to indicate state0 was entered during the session. On arming the module the state sequencer enters state1 and these bits are forced to SSF[2:0] = 001. See Table 268.

Table 268. SSF[2:0] — State Sequence Flag Bit Encoding

SSF[2:0]	Current State
000	State0 (disarmed)
001	State1
010	State2
011	State3
100	Final State
101,110,111	Reserved

Write: DBGACTL if COMRV[1:0] = 00 and DBG not armed
DBGBCTL if COMRV[1:0] = 01 and DBG not armed
DBGCCTL if COMRV[1:0] = 10 and DBG not armed

Table 295. DBGXCTL Field Descriptions

Field	Description
7 SZE (Comparator B)	**Size Comparator Enable Bit** — The SZE bit controls whether access size comparison is enabled for the associated comparator. This bit is ignored if the TAG bit in the same register is set. 0 Word/Byte access size is not used in comparison 1 Word/Byte access size is used in comparison
6 NDB (Comparator A)	**Not Data Bus** — The NDB bit controls whether the match occurs when the data bus matches the comparator register value or when the data bus differs from the register value. This bit is ignored if the TAG bit in the same register is set. This bit is only available for comparator A. 0 Match on data bus equivalence to comparator register contents 1 Match on data bus difference to comparator register contents
6 SZ (Comparator B)	**Size Comparator Value Bit** — The SZ bit selects either word or byte access size in comparison for the associated comparator. This bit is ignored if the SZE bit is cleared or if the TAG bit in the same register is set. This bit is only featured in comparator B. 0 Word access size is compared 1 Byte access size is compared
5 TAG	**Tag Select**— This bit controls whether the comparator match has immediate effect, causing an immediate state sequencer transition or tag the opcode at the matched address. Tagged opcodes trigger only if they reach the execution stage of the instruction queue. 0 Allow state sequencer transition immediately on match 1 On match, tag the opcode. If the opcode is about to be executed allow a state sequencer transition
4 BRK	**Break**— This bit controls whether a comparator match terminates a debug session immediately, independent of state sequencer state. To generate an immediate breakpoint the module breakpoints must be enabled using the DBGC1 bit DBGBRK. 0 The debug session termination is dependent upon the state sequencer and trigger conditions. 1 A match on this channel terminates the debug session immediately; breakpoints if active are generated, tracing, if active, is terminated and the module disarmed.
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is not used if RWE = 0. This bit is ignored if the TAG bit in the same register is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator.This bit is ignored if the TAG bit in the same register is set 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

Table 296 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if the corresponding TAG bit is set since the match occurs based on the tagged opcode reaching the execution stage of the instruction queue.

Table 296. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write data bus
1	0	1	No match
1	1	0	No match
1	1	1	Read data bus

4.31.4.2.1 Exact Address Comparator Match (Comparators A and C)

With range comparisons disabled, the match condition is an exact equivalence of address/data bus with the value stored in the comparator address/data registers. Further qualification of the type of access (R/W, word/byte) is possible.

Comparators A and C do not feature SZE or SZ control bits, thus the access size is not compared. The exact address is compared, thus with the comparator address register loaded with address (n) a word access of address (n–1) also accesses (n) but does not cause a match. Table 313 lists access considerations without data bus compare. Table 312 lists access considerations with data bus comparison. To compare byte accesses DBGADH must be loaded with the data byte and the low byte must be masked out using the DBGADLM mask register. On word accesses the data byte of the lower address is mapped to DBGADH.

Table 312. Comparator A Data Bus Considerations

Access	Address	DBGADH	DBGADL	DBGADHM	DBGADLM	Example Valid Match
Word	ADDR[n]	Data[n]	Data[n+1]	$FF	$FF	MOVW #$WORD ADDR[n]
Byte	ADDR[n]	Data[n]	x	$FF	$00	MOVB #$BYTE ADDR[n]
Word	ADDR[n]	Data[n]	x	$FF	$00	MOVW #$WORD ADDR[n]
Word	ADDR[n]	x	Data[n+1]	$00	$FF	MOVW #$WORD ADDR[n]

Comparator A features an NDB control bit to determine if a match occurs when the data bus differs to comparator register contents, or when the data bus is equivalent to the comparator register contents.

4.31.4.2.2 Exact Address Comparator Match (Comparator B)

Comparator B features SZ and SZE control bits. If SZE is clear, then the comparator address match qualification functions the same as for comparators A and C.

If the SZE bit is set the access size (word or byte) is compared with the SZ bit value such that only the specified type of access causes a match. Thus if configured for a byte access of a particular address, a word access covering the same address does not lead to match.

Table 313. Comparator Access Size Considerations

Comparator	Address	SZE	SZ8	Condition For Valid Match
Comparators A and C	ADDR[n]	—	—	Word and byte accesses of ADDR[n](186) MOVB #$BYTE ADDR[n] MOVW #$WORD ADDR[n]
Comparator B	ADDR[n]	0	X	Word and byte accesses of ADDR[n](186) MOVB #$BYTE ADDR[n] MOVW #$WORD ADDR[n]
Comparator B	ADDR[n]	1	0	Word accesses of ADDR[n](186) MOVW #$WORD ADDR[n]
Comparator B	ADDR[n]	1	1	Byte accesses of ADDR[n] MOVB #$BYTE ADDR[n]

Note:
186. A word access of ADDR[n-1] also accesses ADDR[n] but does not generate a match. The comparator address register must contain the exact address used in the code.

4.31.4.2.3 Range Comparisons

Using the AB comparator pair for a range comparison, the data bus can also be used for qualification by using the comparator A data registers. Furthermore the DBGACTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access. The corresponding DBGBCTL bits are ignored. The SZE and SZ control bits are ignored in range mode. The comparator A TAG bit is used to tag range comparisons. The comparator B TAG bit is ignored in range modes. In order for a range comparison using comparators A

The least significant word of line is read out first. This corresponds to the fields 1 and 0 of Table 315. The next word read returns field 2 in the least significant bits [3:0] and “0” for bits [15:4]. Reading the Trace Buffer while the DBG module is armed, returns invalid data, and no shifting of the RAM pointer occurs.

4.31.4.5.6 Trace Buffer Reset State

The Trace Buffer contents and DBGCNT bits are not initialized by a system reset. Thus should a system reset occur, the trace session information from immediately before the reset occurred, can be read out and the number of valid lines in the trace buffer is indicated by DBGCNT. The internal pointer to the current trace buffer address is initialized by unlocking the trace buffer and points to the oldest valid data, even if a reset occurred during the tracing session. To read the trace buffer after a reset, TSOURCE must be set, otherwise the trace buffer reads as all zeroes. Generally debugging occurrences of system resets is best handled using end trigger alignment, since the reset may occur before the trace trigger, which in the begin trigger alignment case means no information would be stored in the trace buffer. The Trace Buffer contents and DBGCNT bits are undefined following a POR

4.31.4.6 Tagging

A tag follows program information as it advances through the instruction queue. When a tagged instruction reaches the head of the queue, a tag hit occurs and can initiate a state sequencer transition.

Each comparator control register features a TAG bit, which controls whether the comparator match causes a state sequencer transition immediately or tags the opcode at the matched address. If a comparator is enabled for tagged comparisons, the address stored in the comparator match address registers must be an opcode address.

Using Begin trigger together with tagging, if the tagged instruction is about to be executed, then the transition to the next state sequencer state occurs. If the transition is to the Final State, tracing is started. Only upon completion of the tracing session can a breakpoint be generated. Using End alignment, when the tagged instruction is about to be executed and the next transition is to Final State, then a breakpoint is generated immediately before the tagged instruction is carried out.

R/W monitoring is not useful for tagged operations, since the taghit occurs based on the tagged opcode reaching the execution stage of the instruction queue. Similarly access size (SZ) monitoring and data bus monitoring is not useful if tagging is selected, since the tag is attached to the opcode at the matched address, and is not dependent on the data bus nor on the size of access. Thus these bits are ignored if tagging is selected.

When configured for range comparisons and tagging, the ranges are accurate only to word boundaries. Tagging is disabled when the BDM becomes active.

4.31.4.7 Breakpoints

It is possible to generate breakpoints from channel transitions to Final State or using software to write to the TRIG bit in the DBGC1 register.

4.31.4.7.1 Breakpoints From Comparator Channels

Breakpoints can be generated when the state sequencer transitions to the Final State. If configured for tagging, then the breakpoint is generated when the tagged opcode reaches the execution stage of the instruction queue.

If a tracing session is selected by the TSOURCE bit, breakpoints are requested when the tracing session has completed, thus if Begin aligned triggering is selected, the breakpoint is requested only on completion of the subsequent trace (see Table 320). If no tracing session is selected, breakpoints are requested immediately. If the BRK bit is set, then the associated breakpoint is generated immediately independent of tracing trigger alignment.

Table 320. Breakpoint Setup For CPU Breakpoints

BRK	TALIGN	DBGBRK	Breakpoint Alignment
0	0	0	Fill Trace Buffer until trigger, then disarm (no breakpoints)
0	0	1	Fill Trace Buffer until trigger, then breakpoint request occurs
0	1	0	Start Trace Buffer at trigger (no breakpoints)

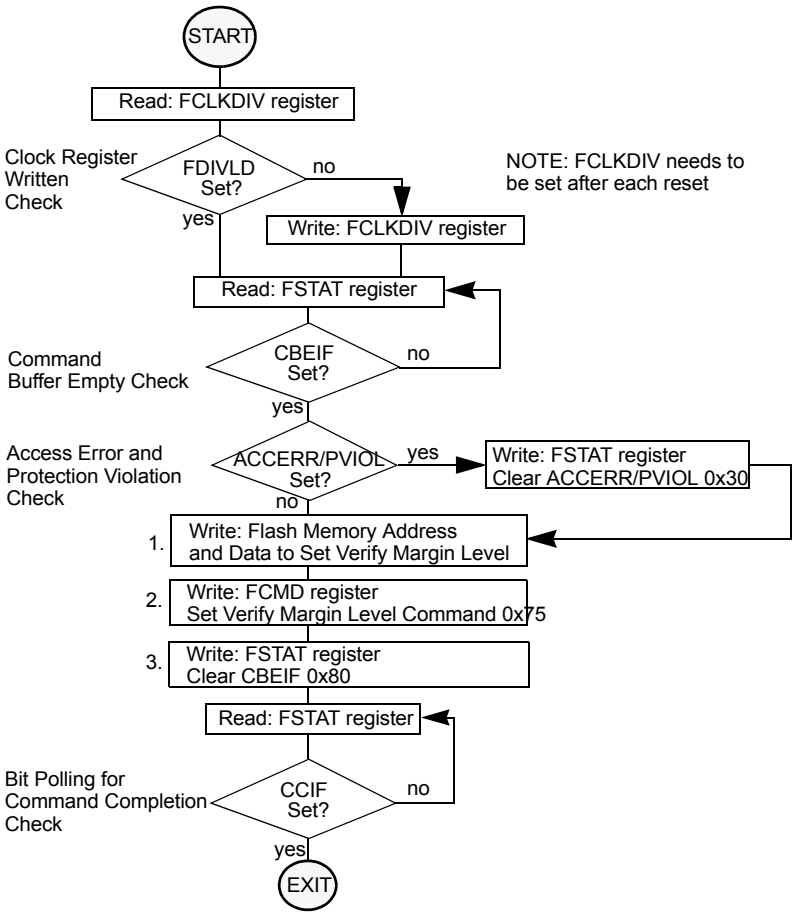


Figure 89. Example Set Verify Margin Level Command Flow (Special Mode only)

4.36.4.3 Illegal Flash Operations

4.36.4.3.1 Flash Access Violations

The ACCERR flag is set during the command write sequence if any of the following illegal steps are performed, causing the command write sequence to immediately abort:

1. Writing to a Flash address before initializing the FCLKDIV register.
2. Writing a byte or misaligned word to a valid Flash address.Writing to any Flash register other than FCMD after writing to a Flash address.
3. Writing to a second Flash address in the same command write sequence.
4. Writing an invalid command to the FCMD register, unless the address written was in a protected area of the Flash array.
5. Writing a command other than burst program, while CBEIF is set and CCIF is clear.
6. When security is enabled, writing a command other than erase verify or mass erase to the FCMD register, when the write originates from a non-secure memory location or from the background debug mode.
7. Writing to a Flash address after writing to the FCMD register.
8. Writing to any Flash register other than FSTAT (to clear CBEIF) after writing to the FCMD register.
9. Writing a 0 to the CBEIF flag in the FSTAT register to abort a command write sequence.

The ACCERR flag also sets if the MCU enters stop mode while any command is active (CCIF=0). The operation is aborted immediately and, if burst programming, any pending burst program command is purged (see Section 4.36.5.2, “Stop Mode").

The ACCERR flag does not set if any Flash register is read during a valid command write sequence. If the Flash memory is read during execution of an algorithm (CCIF = 0), the read operation returns invalid data and the ACCERR flag does not set.

- Configurable timeout period
- Non-maskable interrupt on transaction errors
- Transaction Status and Error Flags
- Interrupt enable for receiving interrupt (from D2D target)

4.37.1.3 Modes of Operation

4.37.1.3.1 D2DI in STOP/WAIT Mode

The D2DI stops working in STOP/WAIT mode. The D2DCLK signal as well as the data signals used are driven low (only after the end of the current high phase, as defined by D2DCLKDIV). Waking from STOP/WAIT mode, the D2DCLK line starts clocking again and the data lines are driven low until the first transaction starts.

STOP and WAIT mode are entered by different CPU instructions. In the WAIT mode, the behavior of the D2DI can be configured (D2DSWAI). Every (enabled) interrupt can be used to leave the STOP and WAIT mode.

4.37.1.3.2 D2DI in special modes

The MCU can enter a special mode (used for test and debugging purposes as well as programming the FLASH). In the D2DI the “write-once” feature is disabled. See the MCU description for details.

4.37.2 External Signal Description

The D2DI optionally uses 6 or 10 port pins. The functions of those pins depends on the settings in the D2DCTL0 register, when the D2DI module is enabled.

4.37.2.1 D2DCLK

NOTE

The maximum allowed D2D target frequency (f_{D2D}) might be lower than the maximum initiator frequency.

When the D2DI is enabled this pin is the clock output. This signal is low if the initiator is disabled, in STOP mode or in WAIT mode (with D2DSWAI asserted), otherwise it is a continuos clock. This pin may be shared with general purpose functionality if the D2DI is disabled.

4.37.2.2 D2DDAT[7:4]

When the D2DI is enabled and the interface connection width D2DCW is set to be 8-bit wide, those lines carry the data bits 7:4 acting as outputs or inputs. When they act as inputs pull-down elements are enabled. If the D2DI is disabled or if the interface connection width is set as 4-bit wide, the pins may be shared with general purpose pin functionality. In the MM912F634 configuration, D2DDAT [7:4] are not bonded, and act as GPIO inputs. These pads are in high-impedance mode. To avoid any leakage in Stop mode, D2DDAT [7:0] should be configured as an output by writing 0xF0 on DDRD register (0x007).

4.37.2.3 D2DDAT[3:0]

When the D2DI is enabled those lines carry the data bits 3:0 acting as outputs or inputs. When they act as inputs pull-down elements are enabled. If the D2DI is disabled the pins and may be shared with general purpose pin functionality.

4.37.2.4 D2DINT

The D2DINT is an active input interrupt input driven by the target device. The pin has an active pull-down device. If the D2DI is disabled, the pin may be shared with general purpose pin functionality.

Table 402. D2DI Address Buffer Register Bit Descriptions (continued)

Field	Description
11:8	Reserved, should be masked to ensure compatibility with future versions of this interface.
7:0 ADR[7:0]	**Transaction Address** — Those read-only bits contain the address of the transaction

4.37.3.2.6 D2DI Data Buffer Register (D2DDATA)

This read-only register contains information about the ongoing D2D interface transaction. For a write transaction, the data becomes valid at the begin of the transaction. For a read transaction, the data is updated during the transaction, and is finalized when the transaction is acknowledged by the target. In error cases, the user can track back what has happened.

Table 403. D2DI Data Buffer Register (D2DDATA)

0x00DE / 0x00DF — Access: User read

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DATA15:0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 404. D2DI Data Buffer Register Bit Descriptions

Field	Description
15:0 DATA	**Transaction Data** — Those read-only bits contain the data of the transaction

Both D2DDATA and D2DADR can be read with byte accesses.

4.37.4 Functional Description

4.37.4.1 Initialization

Out of reset the interface is disabled. The interface must be initialized by setting the interface clock speed, the timeout value, the transfer width, and finally enabling the interface. This should be done using a 16-bit write, or if using 8-bit write, D2DCTL1 must be written before D2D2CTL0.D2DEN = 1 is written. Once it is enabled in normal modes, only a reset can disable it again (write once feature).

4.37.4.2 Transactions

A transaction on the D2D Interface is triggered by writing to either the 256 byte address window or reading from the address window (see STAA/LDAA 0/1 in the next figure). Depending on which address window is used, a blocking or a non-blocking transaction is performed. The address for the transaction is the 8-bit wide window relative address. The data width of the CPU read or write instructions determines if 8-bit or 16-bit wide data are transferred. There is always only one transaction active. Figure 94 shows the various types of transactions explained in more detail below.

For all 16-bit read/write accesses of the CPU, the addresses are assigned according the big-endian model:
word [15:8]: addr word[7:0]: addr+1
addr: byte-address (8 bit wide) inside the blocking or non-blocking window, as provided by the CPU and transferred to the D2D target
word: CPU data, to be transferred from/to the D2D target

The application must care for the stretched CPU cycles (limited by the TIMOUT value, caused by blocking or consecutive accesses), which could affect time limits, including COP (computer operates properly) supervision. The stretched CPU cycles cause the “CPU halted” phases (see Figure 94).