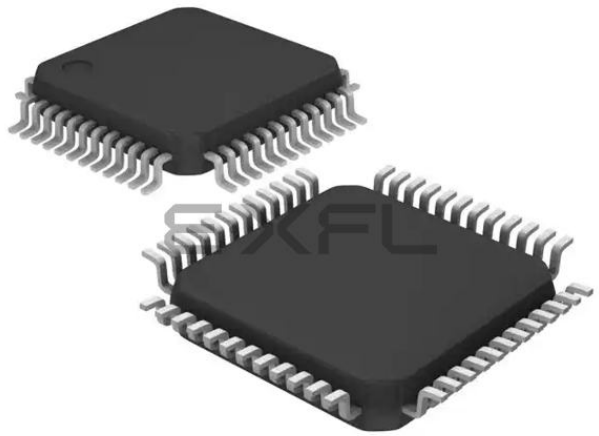

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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (32KB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912f634cv2ap

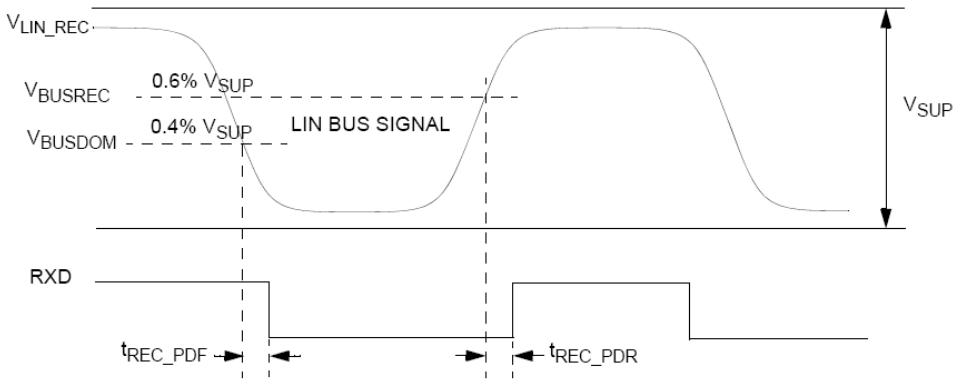


Figure 8. LIN Receiver Timing

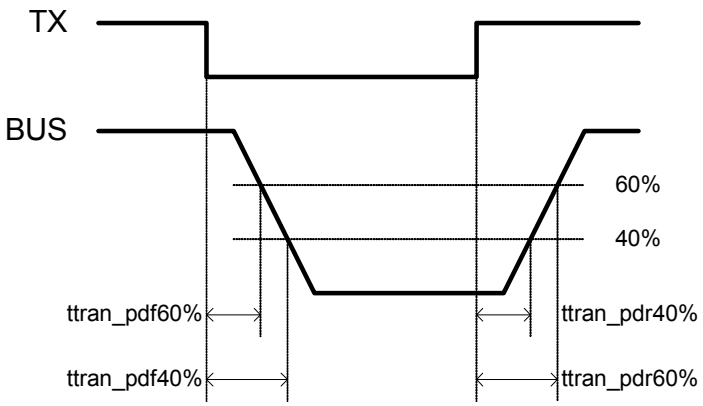


Figure 9. LIN Transmitter Timing

Table 35. Dynamic Electrical Characteristics - General Purpose I/O - PTB[0…2]

Ratings	Symbol	Min	Typ	Max	Unit
GPIO Digital Frequency[37]	f_{PTB}	-	-	10	MHz
Propagation Delay - Rising Edge[37], [38]	t_{PDR}	-	-	20	ns
Rise Time - Rising Edge[37]	t_{RISE}	-	-	17.5	ns
Propagation Delay - Falling Edge[37]	t_{PDF}	-	-	20	ns
Rise Time - Falling Edge[37]	t_{FALL}	-	-	17.5	ns

Note:
37. Guaranteed by design.
38. Load PTBx = 100 pF.

3.6.2.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress tests during qualification, constant process monitors, and burn-in to screen early life failures. The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table 38. NVM Reliability Characteristics

Rating	Symbol	Min	Typ	Max	Unit
Data retention after 10,000 program/erase cycles for $T_{JAVG} \leq 85$ °C[45], [46]	t_{FLRET}	15	100[47]	-	Years
Data retention with <100 program/erase cycles for $T_{JAVG} \leq 85$ °C[45], [46]		20	100[47]	-	
Number of program/erase cycles[46] (-40 °C ≤ T_J ≤ 0 °C)	n_{FL}	10,000	-	-	Cycles
Number of program/erase cycles[46] (0 °C ≤ T_J ≤ 140 °C)		10,000	100,000[48]	-	

Note:
45. T_{JAVG} is the Average Junction Temperature
46. T_{JAVG} does not exceed 85 °C considering a typical temperature profile over the lifetime of a consumer, industrial, or automotive application.
47. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C, using the Arrhenius equation. For additional information on how Freescale defines Typical Data Retention, refer to Engineering Bulletin EB618.
48. Spec table quotes typical endurance evaluated at 25 °C for this product family, typical endurance at various temperature can be estimated using the graph in Figure 10. For additional information on how Freescale defines Typical Endurance, refer to Engineering Bulletin EB619.

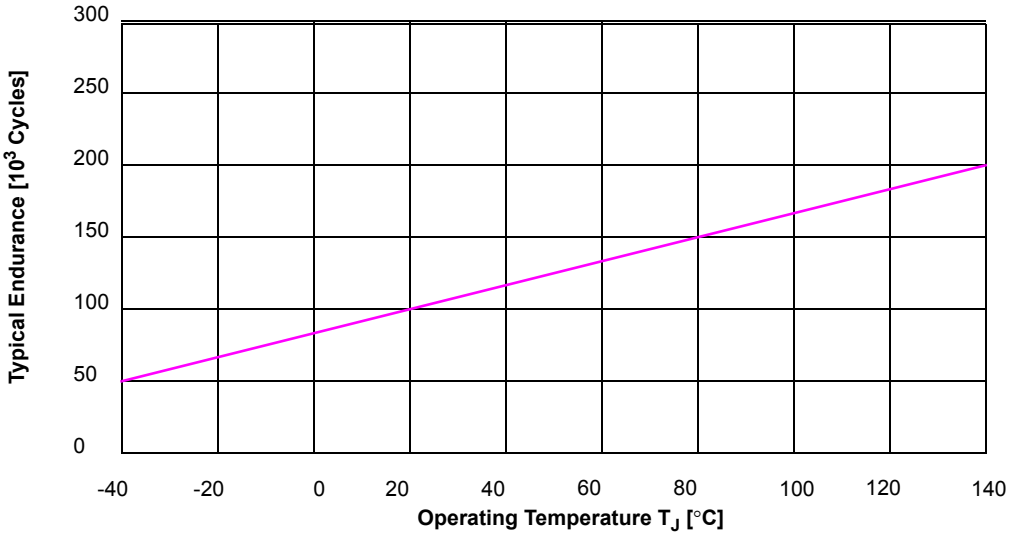


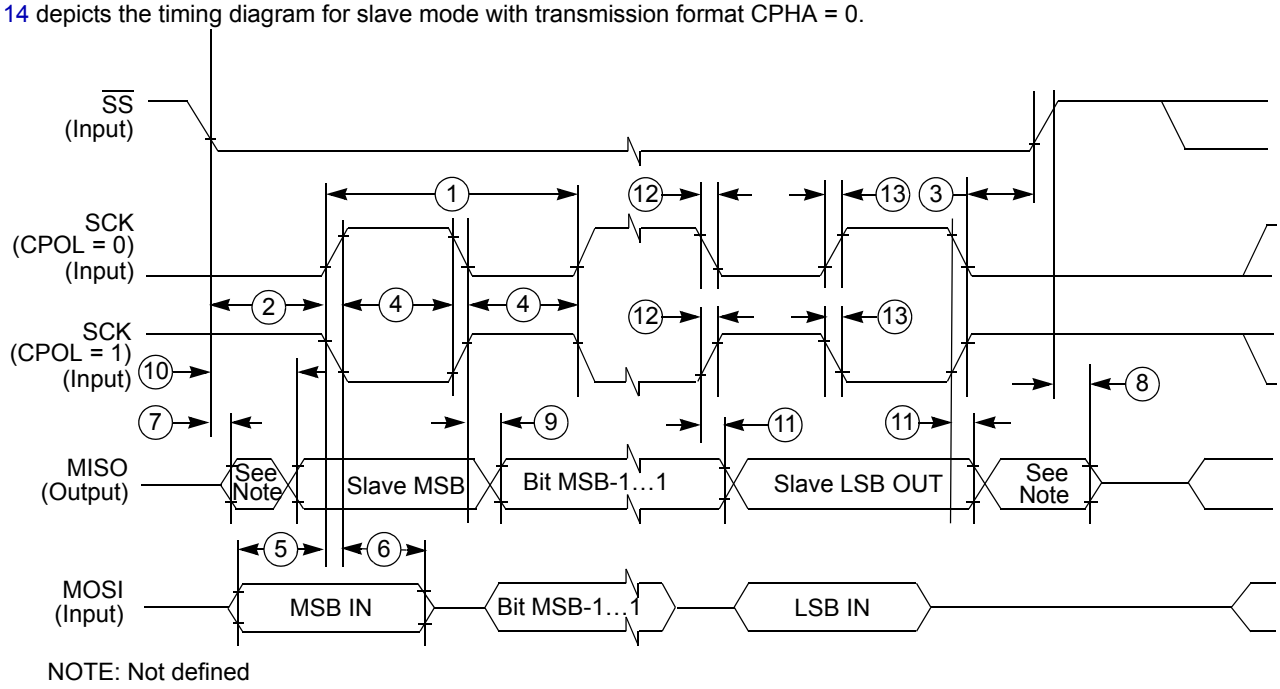
Figure 10. Typical Flash Cycling Endurance vs. Temperature

Table 43. SPI Master Mode Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
SCK frequency	f_{SCK}	1/2048	-	1/2	f_{BUS}
SCK period	t_{SCK}	2.0	-	2048	t_{BUS}
Enable lead time	t_{LEAD}	-	1/2	-	t_{SCK}
Enable lag time	t_{LAG}	-	1/2	-	t_{SCK}
Clock (SCK) high or low time	t_{WSCK}	-	1/2	-	t_{SCK}
Data setup time (inputs)	t_{SU}	8.0	-	-	ns
Data hold time (inputs)	t_{HI}	8.0	-	-	ns
Data valid after SCK edge	t_{VSCK}	-	-	29	ns
Data valid after $\overline{SS}$ fall (CPHA = 0)	t_{VSS}	-	-	15	ns
Data hold time (outputs)	t_{HO}	20	-	-	ns
Rise and fall time inputs	t_{RFI}	-	-	8.0	ns
Rise and fall time outputs	t_{RFO}	-	-	8.0	ns

3.6.2.4.2 Slave Mode

Figure 14 depicts the timing diagram for slave mode with transmission format CPHA = 0.



NOTE: Not defined

Figure 14. SPI Slave Timing (CPHA = 0)

4.2.3.1 Current Sense Module

For device options with the current sense module not available, the following considerations are to be made.

4.2.3.1.1 Pinout considerations

Table 69. ISENSE - Pin Considerations

PIN	PIN name for option 1	New PIN name	Comment
40	ISENSEL	NC	ISENSE feature not bonded and/or not tested. Connect PINs 40 and 41 (NC) to GND.
41	ISENSEH	NC	

4.2.3.1.2 Register Considerations

The Current Sense Register must remain in default (0x00) state.

Offset	Name		7	6	5	4	3	2	1	0
0x3C	CSR	R	CSE	0	0	0	CCD	CSGS		
	Current Sense Register	W								

The Conversion Control Register - Bit 9 must always be written 0.

0x82	ACCR (hi)	R	CH15	CH14	0	CH12	CH11	CH10	CH9	CH8
	ADC Conversion Ctrl Reg	W								

The Conversion Complete Register - Bit 9 must be ignored.

0x84	ACCSR (hi)	R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8
	ADC Conv Complete Reg	W								

The ADC Data Result Reg 9 must be ignored.

0x98	ADR9 (hi)	R	adr9 9	adr9 8	adr9 7	adr9 6	adr9 5	adr9 4	adr9 3	adr9 2
	ADC Data Result Register 9	W								
0x99	ADR9 (lo)	R	adr9 1	adr9 0	0	0	0	0	0	0
	ADC Data Result Register 9	W								

4.2.3.1.3 Functional Considerations

- The complete Current Sense Module is not available.
- The ADC Channel 9 is not available.

4.4 Power Supply

The MM912F634 analog die supplies VDD (2.5 V), VDDX (5.0 V), and HSUP, based on the supply voltage applied to the VS1 pin. VDD is cascaded of the VDDX regulator. To separate the High-side outputs from the main power supply, the VS2 pin does only power the High-side drivers. Both supply pins have to be externally protected against reverse battery conditions. To supply external Hall Effect Sensors, the HSUP pin supplies a switchable regulated supply. See Section 4.10, “Hall Sensor Supply Output - HSUP".

A reverse battery protected input (VSENSE) is implemented to measure the Battery Voltage directly. A serial resistor (RVSENSE) is required on this pin. See Section 4.22, “Supply Voltage Sense - VSENSE". In addition, the VS1 supply can be routed to the ADC (VS1SENSE) to measure the VS1 pin voltage directly. See Section 4.23, “Internal Supply Voltage Sense - VS1SENSE".

To have an independent ADC verification, the internal sleep mode bandgap voltage can be routed to the ADC (BANDGAP). As this node is independent from the ADC reference, any out of range result would indicate malfunctioning ADC or Bandgap reference. See Section 4.24, “Internal Bandgap Reference Voltage Sense - BANDGAP".

To stabilize the internal ADC reference voltage for higher precision measurements, the current limited ADC2p5 pin needs to be connected to an external filter capacitor (C_{ADC2p5}). It is not recommended to connect additional loads to this pin. See Section 4.19, “Analog Digital Converter - ADC".

The following safety features are implemented:

- LBI - Low Battery Interrupt, internally measured at VSENSE
- LVI - Low Voltage Interrupt, internally measured at VS1
- HVI - High Voltage Interrupt, internally measured at VS2
- VROVI - Voltage Regulator Overvoltage Interrupt internally measured at VDD and VDDX
- LVR - Low Voltage Reset, internally measured at VDD
- LVRX - Low Voltage Reset, internally measured at VDDX
- HTI - High Temperature Interrupt measured between the VDD and VDDX regulators
- Overtemperature Shutdown measured between the VDD and VDDX regulators

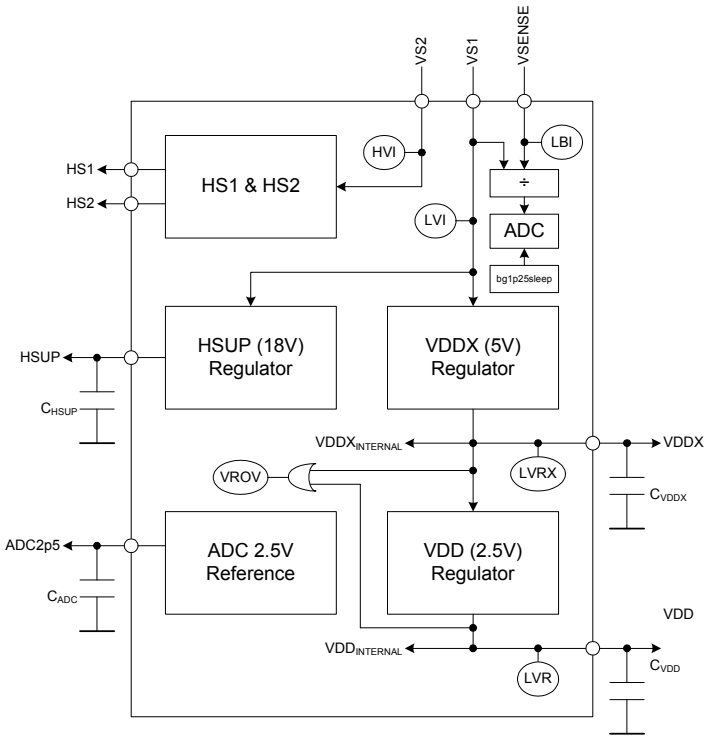


Figure 17. MM912F634 Power Supply

4.5.2 Low Power Mode Operation

The D2D module is disabled in SLEEP mode. In Stop mode, the D2DINT signal is used to wake-up a powered down MCU. As the MCU could wake up without the MM912F634 analog die, a special command is recognized as a wake-up event during Stop mode. See Section 4.3, “Modes of Operation".

4.5.2.1 Normal Mode / Stop Mode

NOTE

The maximum allowed clock speed of the interface is limited to f_{D2D}.

While in Normal or Stop mode, D2DCLK acts as input only with pull present. D2D[3:0] operates as an input/output with pull-down always present. D2DINT acts as output only.

4.5.2.2 Sleep Mode

While in Sleep mode, all Interface data pins are pulled down to DGND to reduce power consumption.

4.6 Interrupts

Interrupts are used to signal a microcontroller that a peripheral needs to be serviced. While in Stop mode, the interrupt signal is used to signal Wake-up events. The interrupts are signaled by an active high level of the D2DINT pin, which remains high until the interrupt is acknowledged via the D2D-Interface. Interrupts are only asserted while in Normal mode.

4.6.1 Interrupt Source Identification

Once an Interrupt is signalized, there are two options to identify the corresponding source(s).

4.6.1.1 Interrupt Source Mirror

NOTE

The VSI - Voltage Status Interrupt combines the five status flags for the Low Battery Interrupt, Low Voltage Interrupt, High Voltage Interrupt, Voltage Regulator Overvoltage Interrupt, and the Voltage Regulator High Temperature Interrupt. The specific source can be identified by reading the Voltage Status Register - VSR.

All Interrupt sources in MM912F634 analog die are mirrored to a special Interrupt Source Register (ISR). This register is read only and indicates all currently pending Interrupts. Reading this register does not acknowledge any interrupt. An additional D2D access is necessary to serve the specific module.

4.6.1.1.1 Interrupt Source Register (ISR)

Table 78. Interrupt Source Register (ISR)

Offset[71] 0x00 (0x00 and 0x01 for 8Bit access) — Access: User read

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	HOT	LSOT	HSOT	LINOT	SCI	RX	TX	ERR	TOV	CH3	CH2	CH1	CH0	VSI
W																

Note:
71. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for this channel:

- Left aligned output (CAEx = 0)
- PWMx Period = Channel Clock Period * PWMPERx Center Aligned Output (CAEx = 1)
- PWMx Period = Channel Clock Period * (2 * PWMPERx)

For boundary case programming values, refer to Section 4.13.4.2.7, “PWM Boundary Cases".

Table 119. PWM Channel Period Registers (PWMPERx)

Offset[95] 0x66/0x67 — Access: User read/write

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Note:
95. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

4.13.3.7 PWM Channel Duty Registers (PWMDTYx)

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active duty due to the double buffering scheme.

There is a dedicated duty register for each channel. The value in this register determines the duty of the associated PWM channel. The duty value is compared to the counter and if it is equal to the counter value a match occurs and the output changes state. The duty registers for each channel are double buffered, so if they change while the channel is enabled, the change does NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM is always either the old duty waveform or the new duty waveform, not some variation in between. If the channel is not enabled, then writes to the duty register goes directly to the latches as well as the buffer. See Section 4.13.4.2.3, “PWM Period and Duty" for more information.

NOTE

Depending on the polarity bit, the duty registers contains the count of either the high time or the low time. If the polarity bit is one, the output starts high and then goes low when the duty count is reached, so the duty registers contain a count of the high time. If the polarity bit is zero, the output starts low and then goes high when the duty count is reached, so the duty registers contain a count of the low time.

To calculate the output duty cycle (high time as a% of period) for a particular channel:

- Polarity = 0 (PPOL x =0)
  - Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
- Polarity = 1 (PPOLx = 1)
  - Duty Cycle = [PWMDTYx / PWMPERx] * 100%

For boundary case programming values, refer to Section 4.13.4.2.7, “PWM Boundary Cases".

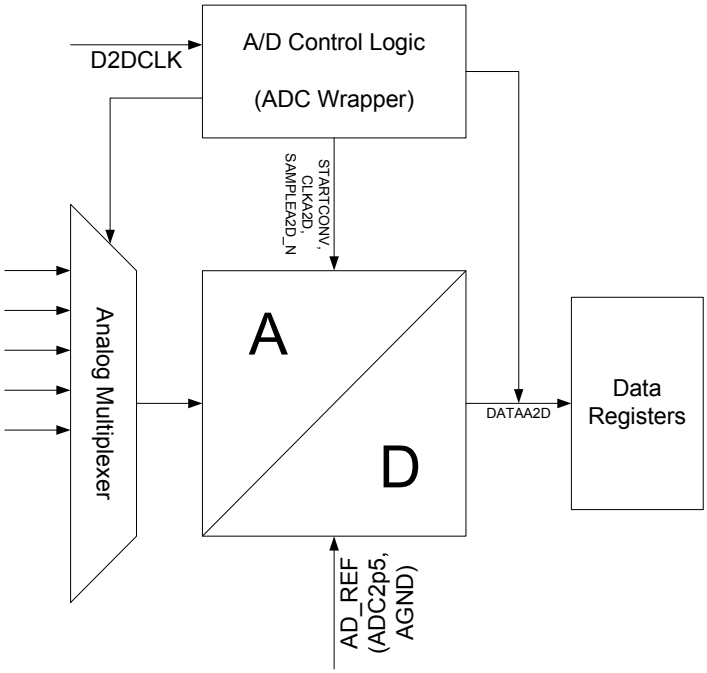


Figure 38. Analog Digital Converter Block Diagram

4.19.1.2 Features

- 10-bit resolution
- 13 µs (typ.), 10-bit Single Sample + Conversion Time
- External ADC2p5 pin with overcurrent protection to filter the analog reference voltage
- Total Error (TE) of ± 5 LSB without offset calibration active
- Integrated selectable offset compensation
- 14 + 1 analog channels (AD0…8; ISENSE, TSENSE and VSENSE, VS1SENSE, BANDGAP, plus calibration channel)
- Sequence- and Continuous Conversion Mode with IRQ for Sequence Complete indication
- Dedicated Result register for each channel

4.19.2 Modes of Operation

The Analog Digital Converter Module is active only in normal mode; it is disabled in Sleep and Stop mode.

4.19.3 External Signal Description

This section lists and describes the signals connected off-chip. Table 187 shows all the pins and their functions controlled by the Analog Digital Converter Module.

Table 187. ADC - Pin Functions and Priorities

Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
AGND	Analog Ground	-	Analog Ground Connection	-
ADC2p5	Analog Regulator	-	Analog Digital Converter Regulator Filter Terminal. A capacitor C_{ADC2p5} is required for operation.	-

Table 190. ACR - Register Field Descriptions (continued)

Field	Description
4 - ADCRST	Analog Digital Converter RESET 0 - Analog Digital Converter in Normal Operation 1 - Analog Digital Converter in Reset Mode, all ADC registers resets to initial values. The bit has to be cleared to allow ADC operation.
2-0 PS2…0	ADC Clock Prescaler Select (D2DCLK to ADCCLK divider) 000 - 10 001 - 8 010 - 6 011 - 4 100 - 2 101 - 1 110 - 1 111 - 1

4.19.4.2.2 ADC Status Register (ASR)

Table 191. ADC Status Register (ASR)

Offset[137] 0x81 Access: User read/write

	7	6	5	4	3	2	1	0
R	SCF	2p5CLF	0	0	CCNT3	CCNT2	CCNT1	CCNT0
W								
Reset	0	0	0	0	1	1	1	1

Note:
137. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 192. ACR - Register Field Descriptions

Field	Description
7 - SCF	Sequence Complete Flag. Reading the ADC Status Register (ASR) clears the Flag.
6 - 2p5CLF	ADC Reference Voltage Current Limitation Flag
3-0 CCNT3…0	Conversion Counter Status. The content of CCNT reflects the current channel in conversion and the conversion of CCNT-1 being complete. The conversion order is CH15, CH0, CH1,..., CH14.

ADC Conversion Control Register (ACCR)

Table 193. ADC Conversion Control Register (ACCR)

Offset[138] 0x82 (0x82 and 0x83 for 8-Bit access) Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CH15	CH14	0	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
138. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

4.26.2 Block Diagrams

Figure 44 shows a block diagram of the MC9S12I32device

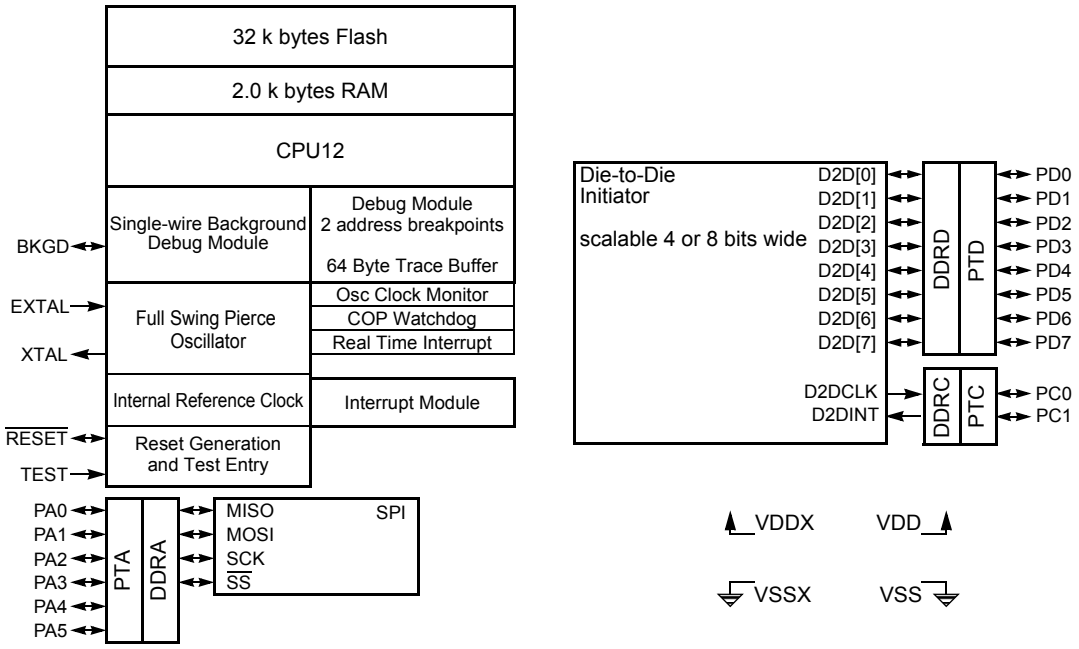


Figure 44. MC9S12I32 Block Diagram

4.26.3 Device Memory Map

4.26.3.1 Address Mapping

Figure 45 shows S12S CPU & BDM local address translation to the global memory map. It also indicates the location of the internal resources in the memory map.

Table 212. Device Internal Resources

Internal Resource	Bottom Address	Top Address
Registers	0x0_0000	0x0_03FF
IFR (if MMCCTL1. IFRON == 1'b1)	0x0_0400	0x0_047F
Reserved[152] (if MMCCTL1.IFRON == 1'b0)		
RAM	0x0_0800	RAM_HIGH = 0x0_07FF plus RAMSIZE[153]
FLASH[154]	FLASH_LOW = 0x4_0000 minus FLASHSIZE[155]	0x3_FFFF

Note:
152. Write access to Reserved has no effect. Read access returns always 0x0000.
153. RAMSIZE is the hexadecimal value of RAM SIZE in bytes.
154. Accessing unimplemented FLASH pages causes an illegal address reset.
155. FLASHSIZE is the hexadecimal value of FLASH SIZE in bytes.

4.26.7 Security

4.26.7.1 MC9S12I32

The MCU security feature allows the protection of the on chip Flash. For a detailed description of the security features refer to the 4.36.6, “Flash Module Security“ description.

4.26.8 Resets and Interrupts

Consult the S12SCPU manual and the 4.27, “Port Integration Module (9S12I32PIMV1)“ description for information on exception processing.

4.26.8.1 Resets

Resets are explained in detail in the 4.27, “Port Integration Module (9S12I32PIMV1)“ description.

4.26.8.2 Vectors

Table 215 lists all interrupt sources and vectors in the order of priority. The interrupt module (4.27, “Port Integration Module (9S12I32PIMV1)“) provides an interrupt vector base register (IVBR) to relocate the vectors.

Table 215. Interrupt Vector Locations

Vector Address[157]	Interrupt Source	CCR Mask	Local Enable
$FFFE	System reset or illegal access reset	None	None
$FFFC	Oscillator monitor reset	None	CRGCTL0 (CME)
$FFFA	COP watchdog reset	None	COP rate select
Vector base + $F8	Unimplemented instruction trap	None	None
Vector base+ $F6	SWI	None	None
Vector base+ $F4	$\overline{\text{D2DI Error Interrupt}}$	X Bit	None
Vector base+ $F2	$\overline{\text{D2DI External Error Interrupt}}$	I bit	D2DIE (D2DCTL1)
Vector base+ $F0	Real time interrupt	I bit	(RTIE)
Vector base + $D8	SPI	I bit	SPICR1 (SPIE, SPTIE)
Vector base + $C6	CRG FLL lock	I bit	CRGCTL1(LOCKIE)
Vector base + $B8	FLASH	I bit	FCNFG (CBEIE, CCIE)
Vector base + $80	Spurious Interrupt	-	None

Note:
157. 16 bits vector address based

4.26.8.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective block descriptions for register reset states.

4.26.8.3.1 I/O Pins

Refer to the 4.27, “Port Integration Module (9S12I32PIMV1)“ description for reset configurations of all peripheral module ports.

4.26.8.3.2 Memory

The RAM array is not initialized out of reset.

Table 218. Port A Data Register Description (continued)

Field	Description
2 PTA	**Port A general purpose input/output data**—Data Register Port A pin 2 is associated with the SCK signal of the SPI module. When not used with the alternative function, this pin can be used as general purpose I/O. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.
1 PTA	**Port A general purpose input/output data**—Data Register Port A pin 1 is associated with the MOSI signal of the SPI module. When not used with the alternative function, this pin can be used as general purpose I/O. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.
0 PTA	**Port A general purpose input/output data**—Data Register Port A pin 0 is associated with the MISO signal of the SPI module. When not used with the alternative function, this pin can be used as general purpose I/O. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.

4.27.3.2 PIM Reserved Register

Table 219. PIM Reserved Register

Address 0x0001 Access: User read(159)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Note:
159. Read: Anytime.
Write: Unimplemented. Writing to this register has no effect.

4.27.3.3 Port A Data Direction Register (DDRA)

Table 220. Port A Data Direction Register (DDRA)

Address 0x0002 Access: User read/write(160)

	7	6	5	4	3	2	1	0
R	0	0	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
W								
Reset	0	0	0	0	0	0	0	0

Note:
160. Read: Anytime.
Write: Anytime.

Table 221. DDRA Register Field Descriptions

Field	Description
5-0 DDRA	**Port A Data Direction**— This register controls the data direction of pins 5 through 0. The SPI function controls the data direction for the associated pins. In this case the data direction bits do not change. When operating a pin as a general purpose I/O, the associated data direction bit determines whether it is an input or output. 1 Associated pin is configured as output. 0 Associated pin is configured as high-impedance input.

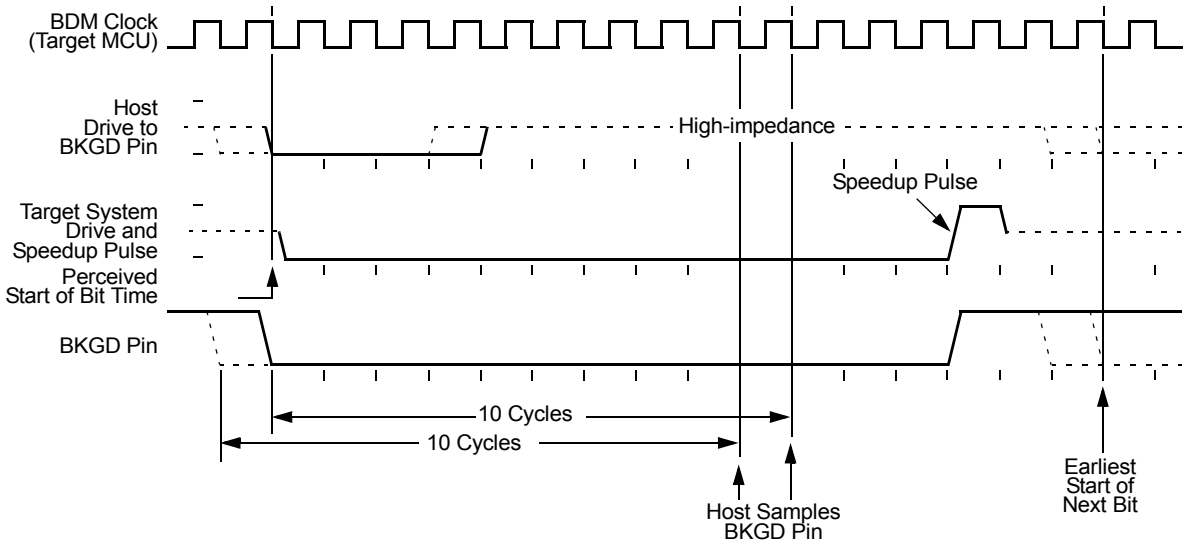


Figure 62. BDM Target-to-Host Serial Bit Timing (Logic 0)

4.30.4.7 Serial Interface Hardware Handshake Protocol

NOTE

If the ACK pulse was issued by the target, the host assumes the previous command was executed. If the CPU enters wait or stop prior to executing a hardware command, the ACK pulse is not issued meaning the BDM command was not executed. After entering wait or stop mode, the BDM command is no longer pending.

BDM commands which require CPU execution are ultimately treated at the MCU bus rate. Since the BDM clock source can be modified relative to the bus clock, when modifying DCO clock or the bus clock divider, it is very helpful to provide a handshake protocol in which the host could determine when an issued command is executed by the CPU. The alternative is to always wait the amount of time equal to the appropriate number of cycles at the slowest possible rate the clock could be running. This sub-section describes the hardware handshake protocol.

The hardware handshake protocol signals to the host controller when an issued command was successfully executed by the target. This protocol is implemented by a 16 serial clock cycle low pulse followed by a brief speedup pulse in the BKGD pin. This pulse is generated by the target MCU when a command, issued by the host, has been successfully executed (see Figure 63). This pulse is referred to as the ACK pulse. After the ACK pulse has finished: the host can start the bit retrieval if the last issued command was a read command, or start a new command if the last command was a write command or a control command (BACKGROUND, GO, GO_UNTIL or TRACE1). The ACK pulse is not issued earlier than 32 serial clock cycles after the BDM command was issued. The end of the BDM command is assumed to be the 16th tick of the last bit. This minimum delay assures enough time for the host to perceive the ACK pulse. Note also that, there is no upper limit for the delay between the command and the related ACK pulse, since the command execution depends upon the CPU bus, which in some cases could be very slow due to long accesses taking place.This protocol allows a great flexibility for the POD designers, since it does not rely on any accurate time measurement or short response time to any event in the serial communication.

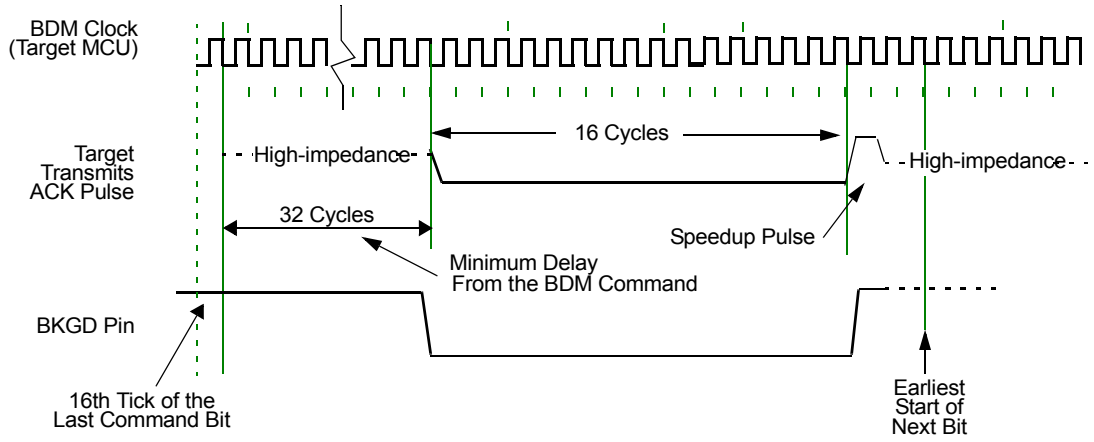


Figure 63. Target Acknowledge Pulse (ACK)

Figure 64 shows the ACK handshake protocol in a command level timing diagram. The READ_BYTE instruction is used as an example. First, the 8-bit instruction opcode is sent by the host, followed by the address of the memory location to be read. The target BDM decodes the instruction. A bus cycle is grabbed (free or stolen) by the BDM and it executes the READ_BYTE operation. Having retrieved the data, the BDM issues an ACK pulse to the host controller, indicating the addressed byte is ready to be retrieved. After detecting the ACK pulse, the host initiates the byte retrieval process. Note that data is sent in the form of a word and the host needs to determine which is the appropriate byte based on whether the address was odd or even.

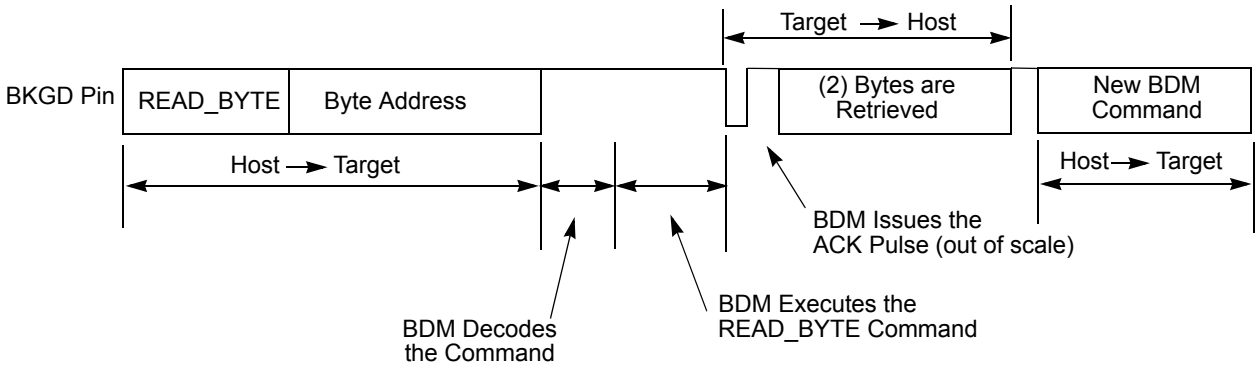


Figure 64. Handshake Protocol at Command Level

NOTE

The only place the BKGD pin can have an electrical conflict is when one side is driving low and the other side is issuing a speedup pulse (high). Other “highs” are pulled rather than driven. However, at low rates the time of the speedup pulse can become lengthy and so the potential conflict time becomes longer as well.

Differently from the normal bit transfer (where the host initiates the transmission), the serial interface ACK handshake pulse is initiated by the target MCU by issuing a negative edge in the BKGD pin. The hardware handshake protocol in Figure 63 specifies the timing when the BKGD pin is being driven, so the host should follow this timing constraint in order to avoid the risk of an electrical conflict in the BKGD pin.

NOTE

The ACK pulse does not provide a timeout. This means for the GO_UNTIL command, it can not be distinguished if a stop or wait has been executed (command discarded and ACK not issued) or if the “UNTIL” condition (BDM active) is just not reached yet. Hence in any case where the ACK pulse of a command is not issued the possible pending command should be aborted before issuing a new command. See the handshake abort procedure described in Section 4.30.4.8, “Hardware Handshake Abort Procedure".

4.31.3.2.8.2 Debug Comparator Address High Register (DBGXAH)

Table 297. Debug Comparator Address High Register (DBGXAH)

Address: 0x0029

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	Bit 17	Bit 16
W								
Reset	0	0	0	0	0	0	0	0

The DBGC1_COMRV bits determine which comparator address registers are visible in the 8-byte window from 0x0028 to 0x002F.

Table 298. Comparator Address Register Visibility

COMRV	Visible Comparator
00	DBGAAH, DBGAAM, DBGAAL
01	DBGBAH, DBGBAM, DBGBAL
10	DBGCAH, DBGCAM, DBGCAL
11	None

Read: Anytime. See Table 299 for visible register encoding.
Write: If DBG not armed. See Table 299 for visible register encoding.

Table 299. DBGXAH Field Descriptions

Field	Description
1–0 Bit[17:16]	**Comparator Address High Compare Bits** — The Comparator address high compare bits control whether the selected comparator compares the address bus bits [17:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

4.31.3.2.8.3 Debug Comparator Address Mid Register (DBGXAM)

Table 300. Debug Comparator Address Mid Register (DBGXAM)

Address: 0x002A

	7	6	5	4	3	2	1	0
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime. See Table 300 for visible register encoding.
Write: If DBG not armed. See Table 300 for visible register encoding.

Table 301. DBGXAM Field Descriptions

Field	Description
7–0 Bit[15:8]	**Comparator Address Mid Compare Bits** — The Comparator address mid compare bits control whether the selected comparator compares the address bus bits [15:8] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

4.31.3.2.8.8 Debug Comparator Data Low Mask Register (DBGADLM)

Table 310. Debug Comparator Data Low Mask Register (DBGADLM)

Address: 0x002F

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 00
Write: If COMRV[1:0] = 00 and DBG not armed.

Table 311. DBGADLM Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Mask Bits** — The Comparator data low mask bits control whether the selected comparator compares the data bus bits [7:0] to the corresponding comparator data compare bits. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Do not compare corresponding data bit. Any value of corresponding data bit allows match 1 Compare corresponding data bit

4.31.4 Functional Description

This section provides a complete functional description of the DBG module. If the part is in secure mode, the DBG module can generate breakpoints, but tracing is not possible.

4.31.4.1 S12SDBGV1 Operation

Arming the DBG module by setting ARM in DBGC1 allows triggering the state sequencer, storing of data in the trace buffer, and generation of breakpoints to the CPU. The DBG module is made up of four main blocks, the comparators, control logic, the state sequencer, and the trace buffer.

The comparators monitor the bus activity of the CPU. All comparators can be configured to monitor address bus activity. Comparator A can also be configured to monitor databus activity and mask out individual data bus bits during a compare. Comparators can be configured to use R/W and word/byte access qualification in the comparison. A match with a comparator register value can initiate a state sequencer transition to another state (see Figure 69). Either forced or tagged matches are possible. Using a forced match, a state sequencer transition can occur immediately on a successful match of system busses and comparator registers. Whilst tagging, at a comparator match, the instruction opcode is tagged and only if the instruction reaches the execution stage of the instruction queue, can a state sequencer transition occur. In the case of a transition to Final State, bus tracing is triggered and/or a breakpoint can be generated.

A state sequencer transition to Final State (with associated breakpoint, if enabled) can be initiated by writing to the TRIG bit in the DBGC1 control register. The trace buffer is visible through a 2-byte window in the register address map, and must be read out using standard 16-bit word reads.

4.33.3 Modes of Operation

The OSCFSP contains the registers and associated bits for controlling and monitoring the oscillator module. Two modes of operation exist:

1. Off (OSCEN=0)
2. Full swing Pierce oscillator (OSCEN=1)

4.33.4 Block Diagram

Figure 76 shows a block diagram of the OSCFSP module.

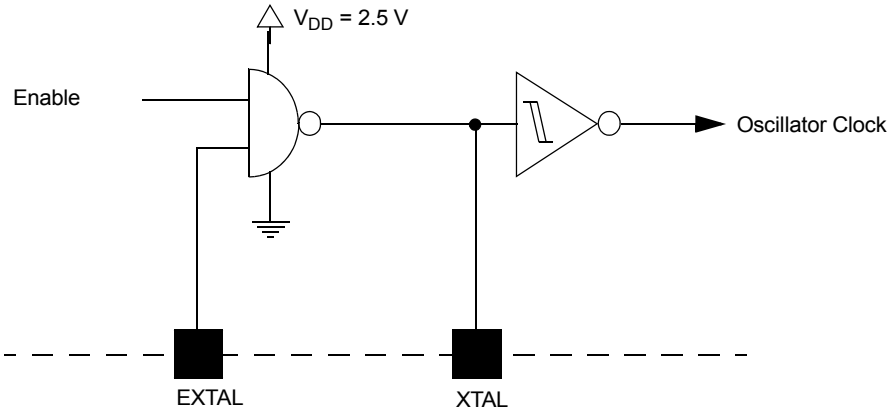


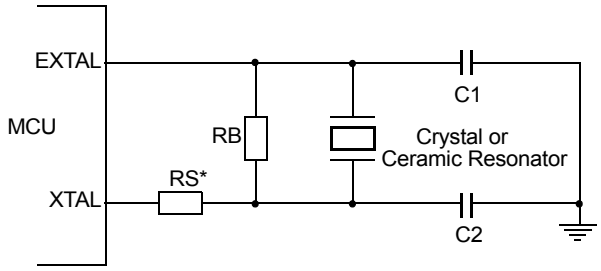
Figure 76. OSCFSP Block Diagram

4.33.5 External Signals EXTAL and XTAL — Input and Output Pins

NOTE

Freescale recommends an evaluation of the application board, and chosen resonator or crystal, by the resonator or crystal supplier. The oscillator circuit is not suited for overtone resonators and crystals.

EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier.



* R_S can be zero (shorted) when use with higher frequency crystals. Refer to manufacturer's data.

Figure 77. Full Swing Pierce Oscillator Connections

4.36.3.4.2 Flash Reserved1 Register (FRSV1)

The FRSV1 register is reserved for factory testing.

Table 373. Flash Reserved1 Register (FRSV1)

0x0107

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

All FRSV1 bits read 0 and are not writable.

4.36.3.4.3 Flash Address Registers (FADDR)

NOTE

The LSB of the MCU global address is not stored in the FADDR registers, since the Flash block is not byte addressable.

The FADDR registers are the Flash address registers.

Table 374. Flash Address High Register (FADDRHI - Normal Mode)

0x0108

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Table 375. Flash Address Low Register (FADDRLO - Normal Mode)

0x0109

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Table 376. Flash Address High Register (FADDRHI - Special Mode)

0x0108

	7	6	5	4	3	2	1	0
R	0	0	FAB[13:8]					
W								
Reset	0	0	0	0	0	0	0	0

4.37.4.7 Interrupts

The D2DI only originates interrupt requests, when D2DI is enabled (D2DIE bit in D2DCTL0 set). There are two different interrupt requests from the D2D module. The interrupt vector offset and interrupt priority are chip dependent.

4.37.4.7.1 D2D External Interrupt

This is a level sensitive active high external interrupt driven by the D2DINT input. This interrupt is enabled if the D2DIE bit in the D2DCTL1 register is set. The interrupt must be cleared using an target specific clearing sequence. The status of the D2D input pin can be observed by reading the D2DIF bit in the D2DSTAT1 register.

The D2DINIT signal is asserted also in the wait and stop mode; it can be used to leave these modes.

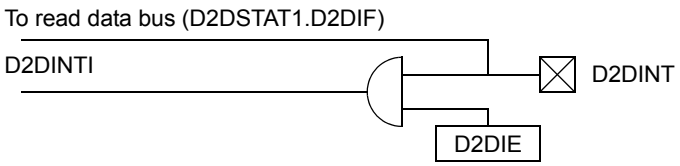


Figure 95. D2D External Interrupt Scheme

4.37.4.7.2 D2D Error Interrupt

Those D2D interface specific interrupts are level sensitive and are all cleared by writing a 1 to the ERRIF flag in the D2DSTAT0 register. This interrupt is not locally maskable and should be tied to the highest possible interrupt level in the system, on an S12 architecture to the XIRQ. See the chapter “Vectors” of the MCU description for details.

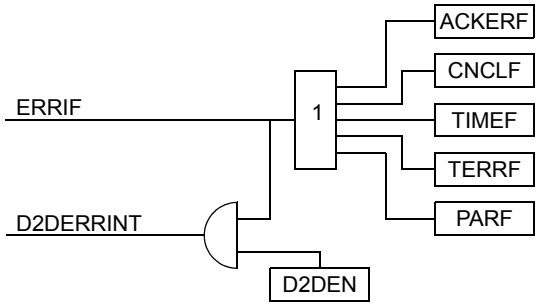


Figure 96. D2D Internal Interrupts

4.37.5 Initialization Information

During initialization the transfer width, clock divider and timeout value must be set according to the capabilities of the target device before starting any transaction. See the D2D Target specification for details.

4.37.6 Application Information

4.37.6.1 Entering low power mode

The D2DI module is typically used on a microcontroller along with an analog companion device containing the D2D target interface and supplying the power. Interface specification does not provide special wires for signalling low power modes to the target device. The CPU should determine when it is time to enter one of the above power modes.The basic flow is as follows:

1. CPU determines there is no more work pending.
2. CPU writes a byte to a register on the analog die using blocking write configuring which mode to enter.
3. Analog die acknowledges that write sending back an acknowledge symbol on the interface.
4. CPU executes WAIT or STOP command.
5. Analog die can enter low-power mode - (S12 needs some more cycles to stack data)

4.38.3.2.4 SPI Status Register (SPISR)

Table 415. SPI Status Register (SPISR)

0x00EB

	7	6	5	4	3	2	1	0
R	SPIF	0	SPTEF	MODF	0	0	0	0
W								
Reset	0	0	1	0	0	0	0	0

Read: Anytime
Write: Has no effect

Table 416. SPISR Field Descriptions

Field	Description
7 SPIF	**SPIF Interrupt Flag** — This bit is set after a received data byte has been transferred into the SPI data register. This bit is cleared by reading the SPISR register (with SPIF set) followed by a read access to the SPI data register. 0 Transfer not yet complete. 1 New data copied to SPIDR.
5 SPTEF	**SPI Transmit Empty Interrupt Flag** — If set, this bit indicates the transmit data register is empty. To clear this bit and place data into the transmit data register, SPISR must be read with SPTEF = 1, followed by a write to SPIDR. Any write to the SPI data register without reading SPTEF = 1, is effectively ignored. 0 SPI data register not empty. 1 SPI data register empty.
4 MODF	**Mode Fault Flag** — This bit is set if the $\overline{SS}$ input becomes low, while the SPI is configured as a master and mode fault detection is enabled, the MODFEN bit of SPICR2 register is set. Refer to MODFEN bit description in Section 4.38.3.2.2, “SPI Control Register 2 (SPICR2)". The flag is cleared automatically by a read of the SPI status register (with MODF set) followed by a write to the SPI control register 1. 0 Mode fault has not occurred. 1 Mode fault has occurred.

4.38.3.2.5 SPI Data Register (SPIDR)

Table 417. SPI Data Register (SPIDR)

0x00ED

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	2	Bit 0
Reset	0	0	0	0	0	0	0	0

Read: Anytime; normally read only when SPIF is set
Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows a data byte to be queued and transmitted. For an SPI configured as a master, a queued data byte is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set. If SPIF is cleared and a byte has been received, the received byte is transferred from the receive shift register to the SPIDR and SPIF is set. If SPIF is set and not serviced, and a second byte has been received, the second received byte is kept as valid byte in the receive shift register until the start of another transmission. The byte in the SPIDR does not change.