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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	6.2 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	1270
Number of Macrocells	980
Number of Gates	-
Number of I/O	114
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5m1270zt144i5

1. MAX V Device Family Overview

MV51001-1.2

The MAX® V family of low cost and low power CPLDs offer more density and I/Os per footprint versus other CPLDs. Ranging in density from 40 to 2,210 logic elements (LEs) (32 to 1,700 equivalent macrocells) and up to 271 I/Os, MAX V devices provide programmable solutions for applications such as I/O expansion, bus and protocol bridging, power monitoring and control, FPGA configuration, and analog IC interface.

MAX V devices feature on-chip flash storage, internal oscillator, and memory functionality. With up to 50% lower total power versus other CPLDs and requiring as few as one power supply, MAX V CPLDs can help you meet your low power design requirement.

This chapter contains the following sections:

Feature Summary

The following list summarizes the MAX V device family features:

- Low-cost, low-power, and non-volatile CPLD architecture
- Instant-on (0.5 ms or less) configuration time
- Standby current as low as 25 µA and fast power-down/reset operation
- Fast propagation delay and clock-to-output times
- Internal oscillator
- Emulated RSDS output support with a data rate of up to 200 Mbps
- Emulated LVDS output support with a data rate of up to 304 Mbps
- Four global clocks with two clocks available per logic array block (LAB)
- User flash memory block up to 8 Kbits for non-volatile storage with up to 1000 read/write cycles
- Single 1.8-V external supply for device core
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)

- I/Os are fully compliant with the PCI-SIG® PCI Local Bus Specification, revision 2.2 for 3.3-V operation
- Hot-socket compliant
- Built-in JTAG BST circuitry compliant with IEEE Std. 1149.1-1990

Table 1–1 lists the MAX V family features.

Table 1–1. MAX V Family Features

Feature	5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
LEs	40	80	160	240	570	1,270	2,210
Typical Equivalent Macrocells	32	64	128	192	440	980	1,700
User Flash Memory Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192	8,192
Global Clocks	4	4	4	4	4	4	4
Internal Oscillator	1	1	1	1	1	1	1
Maximum User I/O pins	54	79	79	114	159	271	271
t_{PD1} (ns) *(1)*	7.5	7.5	7.5	7.5	9.0	6.2	7.0
f_{CNT} (MHz) *(2)*	152	152	152	152	152	304	304
t_{SU} (ns)	2.3	2.3	2.3	2.3	2.2	1.2	1.2
t_{CO} (ns)	6.5	6.5	6.5	6.5	6.7	4.6	4.6

Notes to Table 1–1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum global clock frequency, f_{CNT}, is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

MAX V devices accept 1.8 V on their VCCINT pins. The 1.8-V V_{CCINT} external supply powers the device core directly. MAX V devices operate internally at 1.8 V. The supported MultiVolt I/O interface voltage levels (V_{CCIO}) are 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

MAX V devices are available in two speed grades: –4 and –5, with –4 being the fastest. For commercial applications, speed grades –C4 and –C5 are available. For industrial and automotive applications, speed grade –I5 and –A5 are available, respectively. These speed grades represent the overall relative performance, not any specific timing parameter.

For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics for MAX V Devices* chapter.

MAX V devices are available in space-saving FineLine BGA (FBGA), Micro FineLine BGA (MBGA), plastic enhanced quad flat pack (EQFP), and thin quad flat pack (TQFP) packages (refer to Table 1–2 and Table 1–3). MAX V devices support vertical migration within the same package (for example, you can migrate between the 5M570Z, 5M1270Z, and 5M2210Z devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide

the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

Table 1–2. MAX V Packages and User I/O Pins *(Note 1)*

Device	64-Pin MBGA	64-Pin EQFP	68-Pin MBGA	100-Pin TQFP	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	324-Pin FBGA
5M40Z	30	54	—	—	—	—	—	—
5M80Z	30	54	52	79	—	—	—	—
5M160Z	—	54	52	79	79	—	—	—
5M240Z	—	—	52	79	79	114	—	—
5M570Z	—	—	—	74	74	114	159	—
5M1270Z	—	—	—	—	—	114	211	271
5M2210Z	—	—	—	—	—	—	203	271

Note to Table 1–2:

(1) Device packages under the same arrow sign have vertical migration capability.

Table 1–3. MAX V Package Sizes

Package	64-Pin MBGA	64-Pin EQFP	68-Pin MBGA	100-Pin TQFP	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	324-Pin FBGA
Pitch (mm)	0.5	0.4	0.5	0.5	0.5	0.5	1	1
Area (mm^2)	20.25	81	25	256	36	484	289	361
Length × width (mm × mm)	4.5 × 4.5	9 × 9	5 × 5	16 × 16	6 × 6	22 × 22	17 × 17	19 × 19

Integrated Software Platform

The Quartus II software provides an integrated environment for HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and programming of MAX V devices.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

You can debug your MAX V designs using In-System Sources and Probes Editor in the Quartus II software. This feature allows you to easily control any internal signal and provides you with a completely dynamic debugging environment.

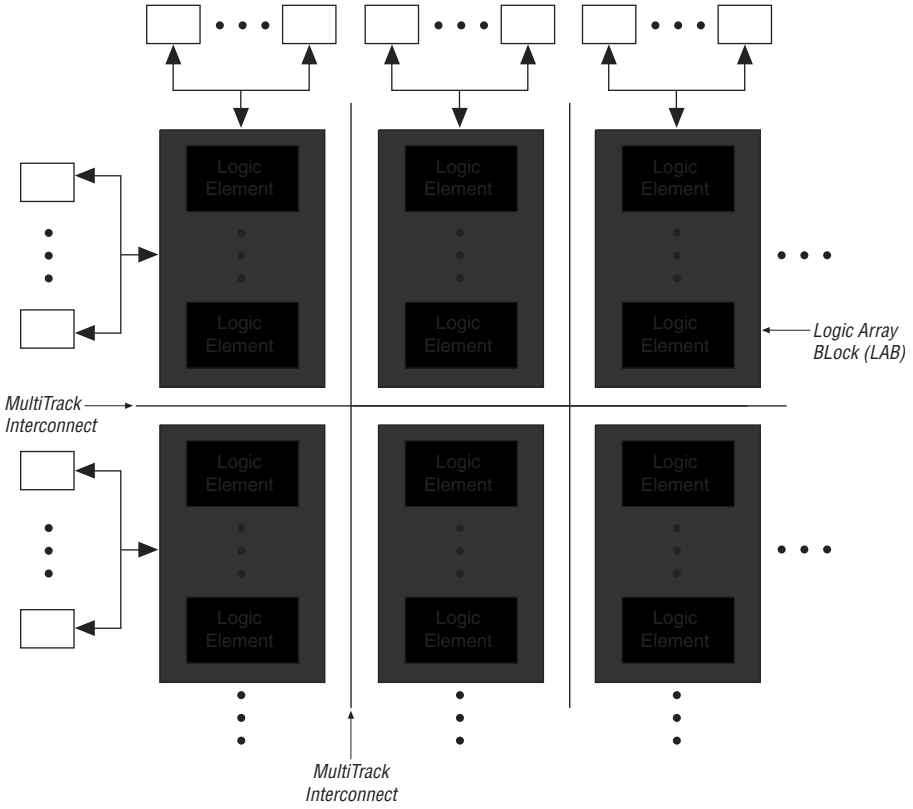
For more information about the In-System Sources and Probes Editor, refer to the *Design Debugging Using In-System Sources and Probes* chapter of the *Quartus II Handbook*.

Device Pin-Outs

For more information, refer to the MAX V Device Pin-Out Files page.

Figure 2–1 shows a functional block diagram of the MAX V device.

Figure 2–1. Device Block Diagram



Each MAX V device contains a flash memory block within its floorplan. This block is located on the left side of the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices. On the 5M240Z (T144 package), 5M570Z, 5M1270Z, and 5M2210Z devices, the flash memory block is located on the bottom-left area of the device. The majority of this flash memory storage is partitioned as the dedicated configuration flash memory (CFM) block. The CFM block provides the non-volatile storage for all of the SRAM configuration information. The CFM automatically downloads and configures the logic and I/O at power-up, providing instant-on operation.

For more information about configuration upon power-up, refer to the *Hot Socketing and Power-On Reset for MAX V Devices* chapter.

A portion of the flash memory within the MAX V device is partitioned into a small block for user data. This user flash memory (UFM) block provides 8,192 bits of general-purpose user storage. The UFM provides programmable port connections to the logic array for reading and writing. There are three LAB rows adjacent to this block, with column numbers varying by device.

improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This mode provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within a LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows a LAB to use LUTs for a single combinational function and the registers for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. For more information about LUT chain and register chain connections, refer to "MultiTrack Interconnect" on page 2–14.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in to 1, which adds one to the LSB. The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The MAX V LE can operate in one of the following modes:

- "Normal Mode"
- "Dynamic Arithmetic Mode"

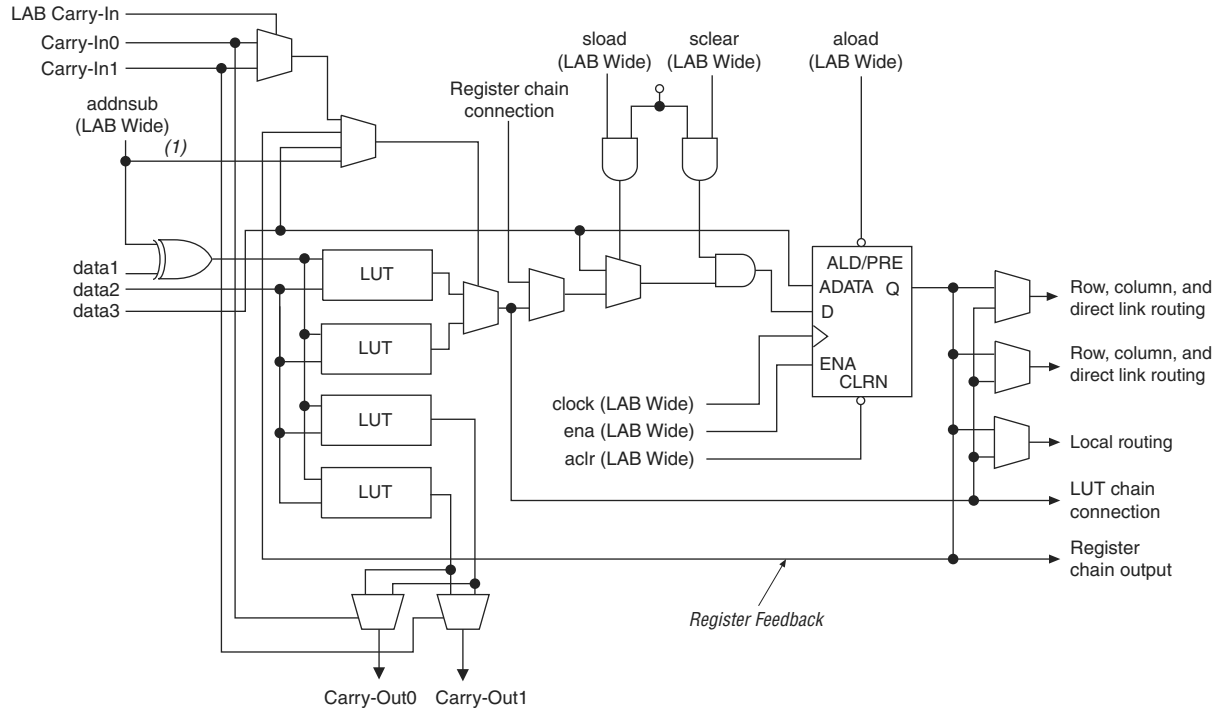
Each mode uses LE resources differently. In each mode, eight available inputs to the LE, the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, along with parameterized functions such as the library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

The other two LUTs use the data1 and data2 signals to generate two possible carry-out signals: one for a carry of 1 and the other for a carry of 0. The carry-in0 signal acts as the carry-select for the carry-out0 output and carry-in1 acts as the carry-select for the carry-out1 output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The addnsub LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2–8. LE in Dynamic Arithmetic Mode



Note to Figure 2–8:

(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The carry-in0 and carry-in1 signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The Quartus II software automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but does not extend between LAB rows.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. MAX V devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX V devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources without using any of the four global resources. Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the `DEV_CLRn` pin is a regular I/O pin.

By default, all registers in MAX V devices are set to power-up low. However, this power-up state can be set to high on individual registers during design entry using the Quartus II software.

LE RAM

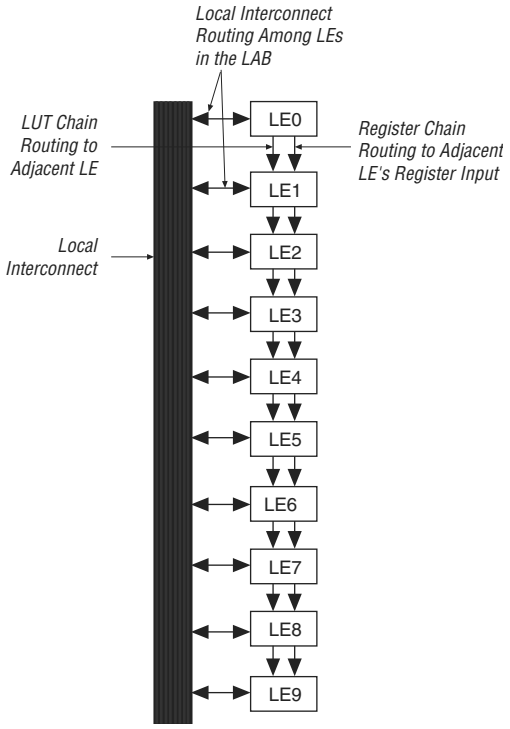
The Quartus II memory compiler can configure the unused LEs as LE RAM.

MAX V devices support the following memory types:

- FIFO synchronous R/W
- FIFO asynchronous R/W
- 1 port SRAM
- 2 port SRAM
- 3 port SRAM
- shift registers

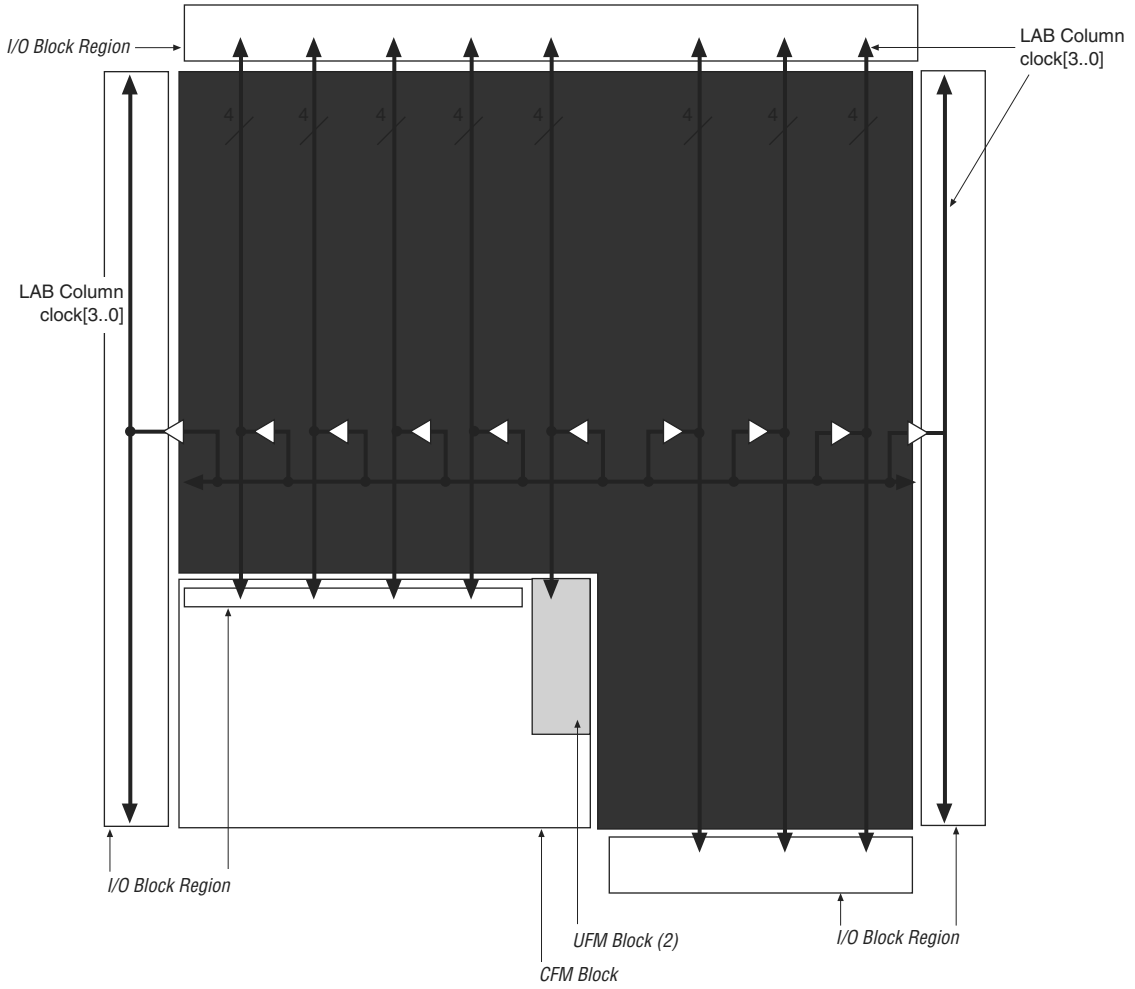
For more information about memory, refer to the *Internal Memory (RAM and ROM) User Guide*.

Figure 2–11. LUT Chain and Register Chain Interconnects



The C4 interconnects span four LABs up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–12 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by column and row IOEs. For LAB interconnection, a primary LAB or its vertical LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–14. Global Clock Network ***(Note 1)***



Notes to Figure 2–14:

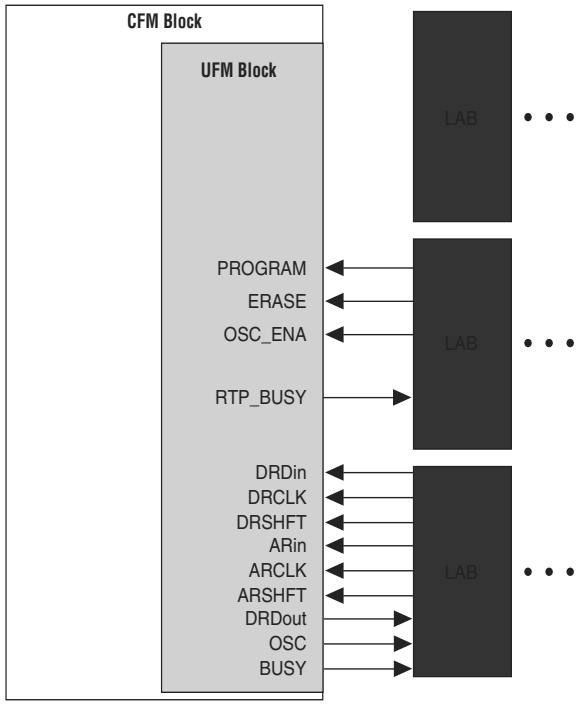
(1) LAB column clocks in I/O block regions provide high fan-out output enable signals.

(2) LAB column clocks drive to the UFM block.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory that contains the CFM block, as shown in Figure 2–1 and Figure 2–2. The UFM block for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices is located on the left side of the device adjacent to the left most LAB column. The UFM blocks for the 5M570Z, 5M1270Z, and 5M2210Z devices are located at the bottom left of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, `GCLK[3..0]`. The interface regions for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices are shown in Figure 2–16. The interface regions for 5M570Z, 5M1270Z, and 5M2210Z devices are shown in Figure 2–17.

Figure 2–16. 5M40Z, 5M80Z, 5M160Z, and 5M240Z UFM Block LAB Row Interface *(Note 1), (2)*



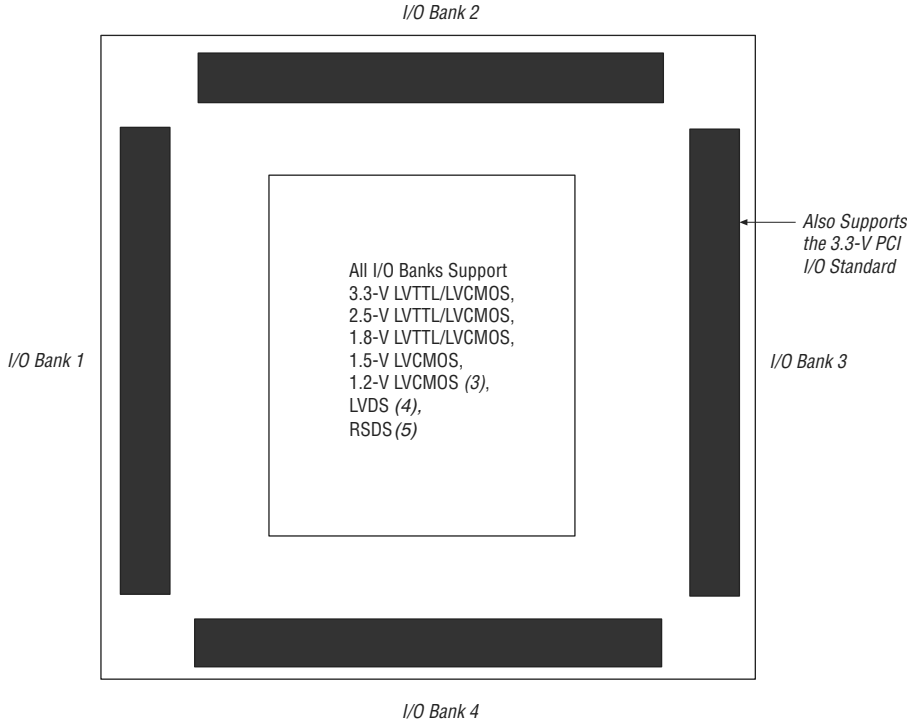
Notes to Figure 2–16:

(1) The UFM block inputs and outputs can drive to and from all types of interconnects, not only DirectLink interconnects from adjacent row LABs.

(2) Not applicable to the T144 package of the 5M240Z device.

The 5M1270Z and 5M2210Z devices support four I/O banks, as shown in Figure 2–23. Each of these banks support all of the LVTTL, LVCMOS, LVDS, and RSDS standards shown in Table 2–4. PCI compliant I/O is supported in Bank 3. Bank 3 supports the PCI clamping diode on inputs and PCI drive compliance on outputs. You must use Bank 3 for designs requiring PCI compliant I/O pins. The Quartus II software automatically places I/O pins in this bank if assigned with the PCI I/O standard.

Figure 2–23. I/O Banks for 5M1270Z and 5M2210Z Devices *(Note 1), (2)*



Notes to Figure 2–23:

(1) Figure 2–23 is a top view of the silicon die.
(2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.
(3) This I/O standard is not supported in Bank 1.
(4) Emulated LVDS output using a three resistor network (LVDS_E_3R).
(5) Emulated RSDS output using a three resistor network (RSDS_E_3R).

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX V devices.

The JTAG pins for MAX V devices are dedicated pins that cannot be used as regular I/O pins. The pins `TMS`, `TDI`, `TDO`, and `TCK` support all the I/O standards shown in Table 2–4 on page 2–29 except for PCI and 1.2-V LVCMOS. These pins reside in Bank 1 for all MAX V devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX V 5M1270Z and 5M2210Z devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX V device speed grades that meet the PCI timing specifications.

Table 2–5. 3.3-V PCI Electrical Specifications and PCI Timing Support for MAX V Devices

Device	33-MHz PCI
5M1270Z	All Speed Grades
5M2210Z	All Speed Grades

LVDS and RSDS Channels

The MAX V device supports emulated LVDS and RSDS outputs on both row and column I/O banks. You can configure the rows and columns as emulated LVDS or RSDS output buffers that use two single-ended output buffers with three external resistor networks.

Table 2–6. LVDS and RSDS Channels supported in MAX V Devices *(Note 1)*

Device	64 MBGA	64 EQFP	68 MBGA	100 TQFP	100 MBGA	144 TQFP	256 FBGA	324 FBGA
5M40Z	10 eTx	20 eTx	—	—	—	—	—	—
5M80Z	10 eTx	20 eTx	20 eTx	33 eTx	—	—	—	—
5M160Z	—	20 eTx	20 eTx	33 eTx	33 eTx	—	—	—
5M240Z	—	—	20 eTx	33 eTx	33 eTx	49 eTx	—	—
5M570Z	—	—	—	28 eTx	28 eTx	49 eTx	75 eTx	—
5M1270Z	—	—	—	—	—	42 eTx	90 eTx	115 eTx
5M2210Z	—	—	—	—	—	—	83 eTx	115 eTx

Note to Table 2–6:

(1) eTx = emulated LVDS output buffers (LVDS_E_3R) or emulated RSDS output buffers (RSDS_E_3R).

Schmitt Trigger

The input buffer for each MAX V device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX V inputs, but adds a small, nominal input delay.

The JTAG input pins (`TMS`, `TCK`, and `TDI`) have Schmitt trigger buffers that are always enabled.

The `TCK` input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

Programmable Pull-Up Resistor

Each MAX V device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

☞ The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.

☞ The programmable pull-up resistor is active during power-up, ISP, and if the device is unprogrammed.

Programmable Input Delay

The MAX V IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX V architecture supports the MultiVolt I/O interface feature, which allows MAX V devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation (V_{CCINT}), and up to four sets for input buffers and I/O output driver buffers (V_{CCIO}), depending on the number of I/O banks available in the devices where each set of VCCIO pins powers one I/O bank. The 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z devices each have two I/O banks while the 5M1270Z and 5M2210Z devices each have four I/O banks.

Connect VCCIO pins to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2–8 summarizes MAX V MultiVolt I/O support.

Table 2–8. MultiVolt I/O Support in MAX V Devices (Part 1 of 2) *(Note 1)*

VCCIO (V)	Input Signal						Output Signal					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.2	✓	—	—	—	—	—	✓	—	—	—	—	—
1.5	—	✓	✓	✓	✓	—	✓	✓	—	—	—	—
1.8	—	✓	✓	✓	✓	—	✓ *(2)*	✓ *(2)*	✓	—	—	—
2.5	—	—	—	✓	✓	—	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	—	—

Recommended Operating Conditions

Table 3–2 lists recommended operating conditions for the MAX V device family.

Table 3–2. Recommended Operating Conditions for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT} *(1)*	1.8-V supply voltage for internal logic and in-system programming (ISP)	MAX V devices	1.71	1.89	V
V_{CCIO} *(1)*	Supply voltage for I/O buffers, 3.3-V operation	—	3.00	3.60	V
	Supply voltage for I/O buffers, 2.5-V operation	—	2.375	2.625	V
	Supply voltage for I/O buffers, 1.8-V operation	—	1.71	1.89	V
	Supply voltage for I/O buffers, 1.5-V operation	—	1.425	1.575	V
	Supply voltage for I/O buffers, 1.2-V operation	—	1.14	1.26	V
V_I	Input voltage	*(2)*, *(3)*, *(4)*	–0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V
T_J	Operating junction temperature	Commercial range	0	85	°C
		Industrial range	–40	100	°C
		Extended range *(5)*	–40	125	°C

Notes to Table 3–2:

(1) MAX V device ISP and/or user flash memory (UFM) programming using JTAG or logic array is not guaranteed outside the recommended operating conditions (for example, if brown-out occurs in the system during a potential write/program sequence to the UFM, Altera recommends that you read back the UFM contents and verify it against the intended write data).

(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) During transitions, the inputs may overshoot to the voltages shown below based on the input duty cycle. The DC case is equivalent to 100% duty cycle. For more information about 5.0-V tolerance, refer to the *Using MAX V Devices in Multi-Voltage Systems* chapter.

V_{IN}	Max. Duty Cycle
4.0 V	100% (DC)
4.1 V	90%
4.2 V	50%
4.3 V	30%
4.4 V	17%
4.5 V	10%

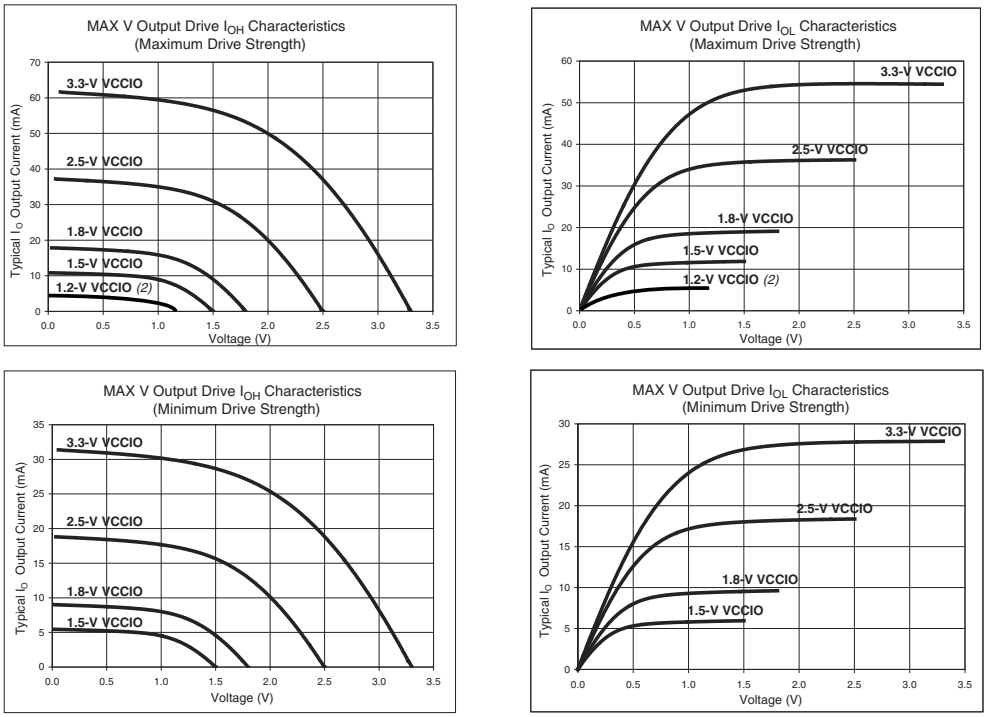
(4) All pins, including the clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(5) For the extended temperature range of 100 to 125°C, MAX V UFM programming (erase/write) is only supported using the JTAG interface. UFM programming using the logic array interface is not guaranteed in this range.

Output Drive Characteristics

Figure 3–1 shows the typical drive strength characteristics of MAX V devices.

Figure 3–1. Output Drive Characteristics of MAX V Devices *(Note 1)*



Notes to Figure 3–1:

(1) The DC output current per pin is subject to the absolute maximum rating of Table 3–1 on page 3–1.

(2) 1.2-V V_{CCIO} is only applicable to the maximum drive strength.

I/O Standard Specifications

Table 3–5 through Table 3–13 on page 3–8 list the I/O standard specifications for the MAX V device family.

Table 3–5. 3.3-V LVTTL Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.8	V
V_{OH}	High-level output voltage	IOH = –4 mA *(1)*	2.4	—	V
V_{OL}	Low-level output voltage	IOL = 4 mA *(1)*	—	0.45	V

Note to Table 3–5:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3–17. Device Performance for MAX V Devices (Part 2 of 2)

Resource Used	Design Size and Function	Resources Used			Performance				Unit
					5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z		5M1270Z/ 5M2210Z		
		Mode	LEs	UFM Blocks	C4	C5, I5	C4	C5, I5	
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI *(2)*	37	1	9.7	9.7	8.0	8.0	MHz
	512 × 8	Parallel *(3)*	73	1	*(4)*	*(4)*	*(4)*	*(4)*	MHz
	512 × 16	I^2C *(3)*	142	1	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	kHz

Notes to Table 3–17:

(1) This design is a binary loadable up counter.
(2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of logic elements (LEs) used.
(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
(4) This design is asynchronous.
(5) The I^2C megafunction is verified in hardware up to 100-kHz serial clock line rate.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 3–18 through Table 3–25 on page 3–19 list the MAX V device internal timing microparameters for LEs, input/output elements (IOEs), UFM blocks, and MultiTrack interconnects.

For more information about each internal timing microparameters symbol, refer to *AN629: Understanding Timing in Altera CPLDs*.

Table 3–18. LE Internal Timing Microparameters for MAX V Devices (Part 1 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}	LE combinational look-up table (LUT) delay	—	1,215	—	2,247	—	742	—	914	ps
t_{COMB}	Combinational path delay	—	243	—	309	—	192	—	236	ps
t_{CLR}	LE register clear delay	401	—	545	—	309	—	381	—	ps
t_{PRE}	LE register preset delay	401	—	545	—	309	—	381	—	ps
t_{SU}	LE register setup time before clock	260	—	321	—	271	—	333	—	ps
t_{H}	LE register hold time after clock	0	—	0	—	0	—	0	—	ps
t_{CO}	LE register clock-to-output delay	—	380	—	494	—	305	—	376	ps

Table 3–18. LE Internal Timing Microparameters for MAX V Devices (Part 2 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLKHL}	Minimum clock high or low time	253	—	339	—	216	—	266	—	ps
t_{C}	Register control delay	—	1,356	—	1,741	—	1,114	—	1,372	ps

Table 3–19. IOE Internal Timing Microparameters for MAX V Devices

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FASTIO}	Data output delay from adjacent LE to I/O block	—	170	—	428	—	207	—	254	ps
t_{IN}	I/O input pad and buffer delay	—	907	—	986	—	920	—	1,132	ps
t_{GLOB} *(1)*	I/O input pad and buffer delay used as global signal pin	—	2,261	—	3,322	—	1,974	—	2,430	ps
t_{IOE}	Internally generated output enable delay	—	530	—	1,410	—	374	—	460	ps
t_{DL}	Input routing delay	—	318	—	509	—	291	—	358	ps
t_{OD} *(2)*	Output delay buffer and pad delay	—	1,319	—	1,543	—	1,383	—	1,702	ps
t_{XZ} *(3)*	Output buffer disable delay	—	1,045	—	1,276	—	982	—	1,209	ps
t_{ZX} *(4)*	Output buffer enable delay	—	1,160	—	1,353	—	1,303	—	1,604	ps

Notes to Table 3–19:

(1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB}, shown in Table 3–19, are based on a 5M240Z device target.

(2) For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–34 on page 3–24 and Table 3–35 on page 3–25.

(3) For more information about t_{XZ} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–22 on page 3–15 and Table 3–23 on page 3–15.

(4) For more information about t_{ZX} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–20 on page 3–14 and Table 3–21 on page 3–14.

Table 3–20 through Table 3–23 list the adder delays for t_{ZX} and t_{XZ} microparameters when using an I/O standard other than 3.3-V LVTTL with 16 mA drive strength.

Table 3–20. t_{ZX} IOE Microparameter Adders for Fast Slew Rate for MAX V Devices

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	72	—	74	—	101	—	125	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	72	—	74	—	101	—	125	ps
2.5-V LVTTL / LVCMOS	14 mA	—	126	—	127	—	155	—	191	ps
	7 mA	—	196	—	197	—	545	—	671	ps
1.8-V LVTTL / LVCMOS	6 mA	—	608	—	610	—	721	—	888	ps
	3 mA	—	681	—	685	—	2012	—	2477	ps
1.5-V LVCMOS	4 mA	—	1162	—	1157	—	1590	—	1957	ps
	2 mA	—	1245	—	1244	—	3269	—	4024	ps
1.2-V LVCMOS	3 mA	—	1889	—	1856	—	2860	—	3520	ps
3.3-V PCI	20 mA	—	72	—	74	—	–18	—	–22	ps
LVDS	—	—	126	—	127	—	155	—	191	ps
RSDS	—	—	126	—	127	—	155	—	191	ps

Table 3–21. t_{ZX} IOE Microparameter Adders for Slow Slew Rate for MAX V Devices

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	5,951	—	6,063	—	6,012	—	5,743	ps
	8 mA	—	6,534	—	6,662	—	8,785	—	8,516	ps
3.3-V LVCMOS	8 mA	—	5,951	—	6,063	—	6,012	—	5,743	ps
	4 mA	—	6,534	—	6,662	—	8,785	—	8,516	ps
2.5-V LVTTL / LVCMOS	14 mA	—	9,110	—	9,237	—	10,072	—	9,803	ps
	7 mA	—	9,830	—	9,977	—	12,945	—	12,676	ps
1.8-V LVTTL / LVCMOS	6 mA	—	21,800	—	21,787	—	21,185	—	20,916	ps
	3 mA	—	23,020	—	23,037	—	24,597	—	24,328	ps
1.5-V LVCMOS	4 mA	—	39,120	—	39,067	—	34,517	—	34,248	ps
	2 mA	—	40,670	—	40,617	—	39,717	—	39,448	ps
1.2-V LVCMOS	3 mA	—	69,505	—	70,461	—	55,800	—	55,531	ps
3.3-V PCI	20 mA	—	6,534	—	6,662	—	35	—	44	ps

Table 3–30 lists the external I/O timing parameters for the F324 package of the 5M1270Z device.

Table 3–30. Global Clock External I/O Timing Parameters for the 5M1270Z Device *(Note 1), (2)*

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.5	—	1.9	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
t_{CH}	Global clock high time	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

Notes to Table 3–30:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

(2) Only applicable to the F324 package of the 5M1270Z device.

Table 3–31 lists the external I/O timing parameters for the 5M2210Z device.

Table 3–31. Global Clock External I/O Timing Parameters for the 5M2210Z Device *(Note 1)*

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.5	—	1.9	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
t_{CH}	Global clock high time	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

Note to Table 3–31:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

External Timing I/O Delay Adders

The I/O delay timing parameters for the I/O standard input and output adders and the input delays are specified by speed grade, independent of device density.

Table 3–32 through Table 3–36 on page 3–25 list the adder delays associated with I/O pins for all packages. If you select an I/O standard other than 3.3-V LVTTL, add the input delay adder to the external t_{SU} timing parameters listed in Table 3–26 on page 3–20 through Table 3–31. If you select an I/O standard other than 3.3-V LVTTL with 16 mA drive strength and fast slew rate, add the output delay adder to the external t_{CO} and t_{PD} listed in Table 3–26 on page 3–20 through Table 3–31.

Table 3–32. External Timing Input Delay Adders for MAX V Devices

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	42	—	42	—	246	—	303	ps
	With Schmitt Trigger	—	429	—	483	—	787	—	968	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	378	—	368	—	695	—	855	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	658	—	1,334	—	1,642	ps
1.2-V LVCMOS	Without Schmitt Trigger	—	1,055	—	1,010	—	2,324	—	2,860	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps

Table 3–33. External Timing Input Delay t_{GLOB} Adders for GCLK Pins for MAX V Devices (Part 1 of 2)

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	400	—	493	ps