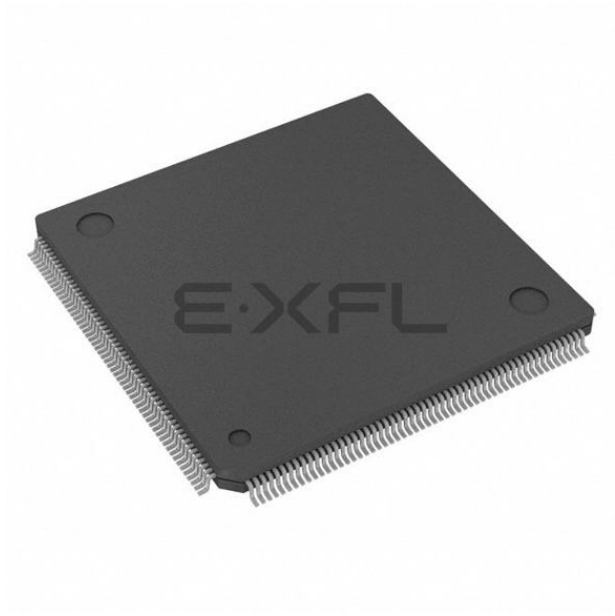

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	190
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	216-LQFP
Supplier Device Package	216-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c49l0agl2000a

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32-kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

- Two power supplies
  - Wide range voltage: VCC = 2.7 V to 5.5 V
  - Power supply for VBAT: VBAT = 1.65 V to 5.5 V

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
33	-	-	-	P5C TIOA11_2 MADATA28_0 RTCCO_1 SUBOUT_1	E	I
34	24	-	G6	P30 RX0_1 TIOA13_2 INT03_2 MDQM2_0 I2SDI0_0	E	K
35	25	-	H4	P31 TX0_1 TIOB13_2 MDQM3_0 I2SCK0_0	E	I
36	26	21	H2	P32 BIN2_1 INT19_0 S_DATA1_0	L	K
37	27	22	J1	P33 FRCK0_0 ZIN2_1 S_DATA0_0	L	I
38	28	23	H3	P34 IC03_0 INT00_1 S_CLK_0	L	K
39	29	24	H1	VCC	-	-
40	30	25	H5	VSS	-	-
41	31	26	H6	P35 IC02_0 INT01_1 S_CMD_0	L	K
42	32	27	J5	P36 IC01_0 INT02_1 S_DATA3_0	L	K
43	33	28	J4	P37 IC00_0 INT03_1 S_DATA2_0	L	K

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
77	62	54	M6	P49 VWAKEUP	O	U
78	63	-	K5	PF0 SCS63_0 RX2_1 FRCK1_1 TIOA15_1 INT22_1	E	K
79	64	-	K6	PF1 SCS62_0 TX2_1 TIOB15_1 INT23_1	E	K
80	65	55	L6	P70 ADTG_8 SIN1_1 INT06_0 MRDY_0	I	K
81	66	56	J6	P71 SOT1_1 (SDA1_1) MAD00_0	E	I
82	67	57	L8	P72 SIN9_0 TIOB0_0 INT07_0 MAD01_0	E	K
83	68	58	K8	P73 SOT9_0 (SDA9_0) TIOB1_0 MAD02_0	E	I
84	69	59	J8	P74 SCK9_0 (SCL9_0) TIOB2_0 MAD03_0	E	I
85	70	-	N8	PF2 RTO10_1 (PPG10_1) TIOA6_1 MRASX_0	L	I
86	71	-	M8	PF3 RTO11_1 (PPG10_1) TIOB6_1 INT05_1 MCASX_0	L	K
87	72	-	N9	PF4 RTO12_1 (PPG12_1) TIOA7_1 INT06_1 MSDWEX_0	L	K

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
115	95	79	K13	P11 AN01 SOT10_0 (SDA10_0) TIOB0_2 BIN0_2	F	L
116	96	80	K12	P12 AN02 SCK10_0 (SCL10_0) TIOA1_2 ZIN0_2	F	L
117	97	81	K14	P13 AN03 SIN6_1 RX1_1 INT25_1	F	M
118	98	82	K11	P14 AN04 SOT6_1 (SDA6_1) TX1_1	F	L
119	-	-	-	PB8 ADTG_6 SCS63_1 INT08_2 TRACED8	E	O
120	-	-	-	PB9 SIN9_1 AIN2_2 INT09_2 TRACED9	E	O
121	-	-	-	PBA SOT9_1 (SDA9_1) BIN2_2 TRACED10	E	N
122	-	-	-	PBB SCK9_1 (SCL9_1) ZIN2_2 TRACED11	E	N
123	99	83	J13	P15 AN05 SIN11_0 TIOB1_2 AIN1_2 INT09_0	F	M
124	100	84	J12	P16 AN06 SOT11_0 (SDA11_0) TIOA2_2 BIN1_2	F	L

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
200	-	-	-	P6C SOT14_1 (SDA14_1) IC21_1 TIOA6_2	E	I
201	-	-	-	P6B SIN14_1 IC20_1 TIOB7_2 INT14_2	E	K
202	-	-	-	P6A DTTI2X_1 TIOA7_2	E	I
203	-	-	-	P69 RTO20_1 (PPG20_1) TIOB14_2	E	I
204	-	-	-	P68 SCK13_1 (SCL13_0) RTO21_1 (PPG20_1) TIOA14_2	E	I
205	-	-	-	P67 SOT13_1 (SDA13_1) RTO22_1 (PPG22_1) TIOB15_2	E	I
206	-	-	-	P66 SIN13_1 RTO23_1 (PPG22_1) TIOA15_2 INT15_2	E	K
207	167	-	E6	P65 RTO24_1 (PPG24_1) INT28_1	E	K
208	168	-	B5	P64 CTS4_0 RTO25_1 (PPG24_1) INT29_1	I	K
209	169	137	C5	P63 ADTG_3 RTS4_0 INT30_0 MOEX_0	L	K
210	170	138	B4	P62 SCK4_0 (SCL4_0) MWEX_0	L	I

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
External Interrupt	INT06_0	External interrupt request 06 input pin	80	65	55	L6
	INT06_1		87	72	-	N9
	INT06_2		103	-	-	-
	INT07_0	External interrupt request 07 input pin	82	67	57	L8
	INT07_1		88	73	-	P9
	INT07_2		102	-	-	-
	INT08_0	External interrupt request 08 input pin	114	94	78	L11
	INT08_1		127	103	-	J9
	INT08_2		119	-	-	-
	INT09_0	External interrupt request 09 input pin	123	99	83	J13
	INT09_1		128	104	-	H10
	INT09_2		120	-	-	-
	INT10_0	External interrupt request 10 input pin	130	106	86	H9
	INT10_1		138	112	-	G13
	INT10_2		149	-	-	-
	INT11_0	External interrupt request 11 input pin	133	109	89	G14
	INT11_1		139	113	-	F14
	INT11_2		151	-	-	-
	INT12_0	External interrupt request 12 input pin	194	162	132	E7
	INT12_1		169	139	-	C11
	INT12_2		175	-	-	-
	INT13_0	External interrupt request 13 input pin	184	152	122	E8
	INT13_1		170	140	-	D11
	INT13_2		176	-	-	-
	INT14_0	External interrupt request 14 input pin	192	160	130	A6
	INT14_1		171	141	-	B10
	INT14_2		201	-	-	-
	INT15_0	External interrupt request 15 input pin	193	161	131	D7
	INT15_1		172	142	-	C10
	INT15_2		206	-	-	-
	INT16_0	External interrupt request 16 input pin	25	20	17	G2
	INT16_1		45	35	30	J2
	INT17_0	External interrupt request 17 input pin	30	21	18	G3
	INT17_1		46	36	31	K1
	INT18_0	External interrupt request 18 input pin	31	22	19	G4
	INT18_1		47	37	32	K2
	INT19_0	External interrupt request 19 input pin	36	26	21	H2
	INT19_1		48	38	33	K3
	INT20_0	External interrupt request 20 input pin	91	76	60	K9
	INT20_1		89	74	-	M9

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PA0	General-purpose I/O port A	2	2	2	B2
	PA1		3	3	3	C2
	PA2		4	4	4	C3
	PA3		5	5	5	D5
	PA4		6	6	6	D2
	PA5		7	7	7	D1
	PA6		8	8	8	D3
	PA7		9	9	9	D4
	PA8		14	13	10	E5
	PA9		15	14	11	F1
	PAA		16	15	12	F2
	PAB		17	16	13	F3
	PAC		18	17	14	F4
	PAD		23	18	15	F5
	PAE		24	19	16	F6
	PAF		25	20	17	G2
	PB0	General-purpose I/O port B	126	102	-	J10
	PB1		127	103	-	J9
	PB2		128	104	-	H10
	PB3		129	105	-	J14
	PB4		138	112	-	G13
	PB5		139	113	-	F14
	PB6		140	114	-	G12
	PB7		141	115	-	G11
	PB8		119	-	-	-
	PB9		120	-	-	-
	PBA		121	-	-	-
	PBB		122	-	-	-
	PBC		148	-	-	-
	PBD		149	-	-	-
	PBE		150	-	-	-
	PBF		151	-	-	-

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	56	46	38	N2
	AIN0_1		65	-	-	-
	AIN0_2		114	94	78	L11
	BIN0_0	QPRC ch.0 BIN input pin	57	47	39	N3
	BIN0_1		66	-	-	-
	BIN0_2		115	95	79	K13
	ZIN0_0	QPRC ch.0 ZIN input pin	58	48	40	M3
	ZIN0_1		67	-	-	-
	ZIN0_2		116	96	80	K12
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch.1 AIN input pin	91	76	60	K9
	AIN1_1		94	-	-	-
	AIN1_2		123	99	83	J13
	BIN1_0	QPRC ch.1 BIN input pin	92	77	61	P10
	BIN1_1		95	-	-	-
	BIN1_2		124	100	84	J12
	ZIN1_0	QPRC ch.1 ZIN input pin	93	78	62	N10
	ZIN1_1		101	-	-	-
	ZIN1_2		125	101	85	J11
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch.2 AIN input pin	2	2	2	B2
	AIN2_1		32	23	20	G5
	AIN2_2		120	-	-	-
	BIN2_0	QPRC ch.2 BIN input pin	3	3	3	C2
	BIN2_1		36	26	21	H2
	BIN2_2		121	-	-	-
	ZIN2_0	QPRC ch.2 ZIN input pin	4	4	4	C3
	ZIN2_1		37	27	22	J1
	ZIN2_2		122	-	-	-
Quadrature Position/ Revolution Counter 3	AIN3_0	QPRC ch.3 AIN input pin	18	17	14	F4
	AIN3_1		45	35	30	J2
	AIN3_2		149	-	-	-
	BIN3_0	QPRC ch.3 BIN input pin	23	18	15	F5
	BIN3_1		46	36	31	K1
	BIN3_2		150	-	-	-
	ZIN3_0	QPRC ch.3 ZIN input pin	24	19	16	F6
	ZIN3_1		47	37	32	K2
	ZIN3_2		151	-	-	-
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	211	171	139	C4
	RTCCO_1		33	-	-	-
	SUBOUT_0	Sub clock output pin	211	171	139	C4
	SUBOUT_1		33	-	-	-

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Reset	INITX	External Reset Input pin. A reset is valid when INITX= L.	72	57	49	N5
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1= L must be input.	104	84	68	N13
	MD0	Mode 0 pin. During normal operation, MD0= L must be input. During serial programming to Flash memory, MD0= H must be input.	105	85	69	N12
Power	VCC	Power supply Pin	1	1	1	C1
			39	29	24	H1
			55	45	37	N1
			64	54	46	P4
			109	89	73	M14
			137	-	-	-
			159	129	105	E14
			163	133	109	A13
			188	156	126	A9
			213	173	141	A4
GND	VSS	GND Pin	40	30	25	H5
			54	44	36	M1
			63	53	45	P3
			108	88	72	N14
			136	-	-	-
			162	132	108	B14
			189	157	127	A8
			216	176	144	B1
			-	-	-	E1
			-	-	-	G1
			-	-	-	P7
			-	-	-	P11
			-	-	-	L14
			-	-	-	A11
			-	-	-	A5
			-	-	-	N7
			-	-	-	M7
			-	-	-	K7
			-	-	-	J7
			-	-	-	G7
			-	-	-	H7
			-	-	-	H8
			-	-	-	G8

Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_2FFF		Multi-Function Timer unit 2
0x4002_3000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_CFFF		Reserved
0x4003_D000	0x4003_DFFF		I^2S prescaler
0x4003_E000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface

Start Address	End Address	Bus	Peripherals
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch 0
0x4006_3000	0x4006_3FFF		CAN ch 1
0x4006_4000	0x4006_BFFF		Reserved
0x4006_C000	0x4006_CFFF		I^2S
0x4006_D000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x4007_FFFF		CAN-FD (CAN ch 2)
0x4008_0000	0x4008_0FFF		Programmable-CRC
0x4008_1000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		Workflash I/F register
0xD000_0000	0xDFFF_FFFF		High-speed quad SPI control register

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θ_{JA} (°C/W)	Maximum Permissible Power (mW)	
			T_A = +85°C	T_A = +105°C
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645
LQQ216 (0.4-mm pitch)	Single-layered both sides	46	870	435
	4 layers	32	1250	625
LBE192 (0.8-mm pitch)	Single-layered both sides	-	-	-
	4 layers	35	1143	571

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

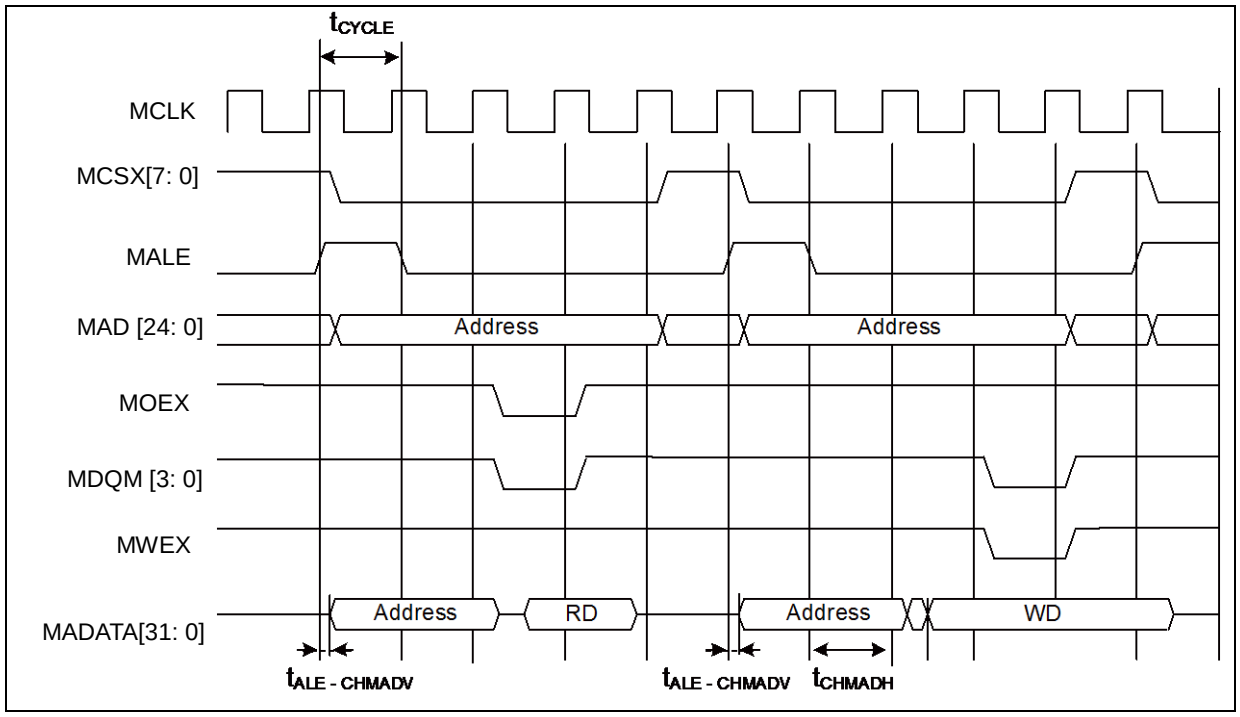
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

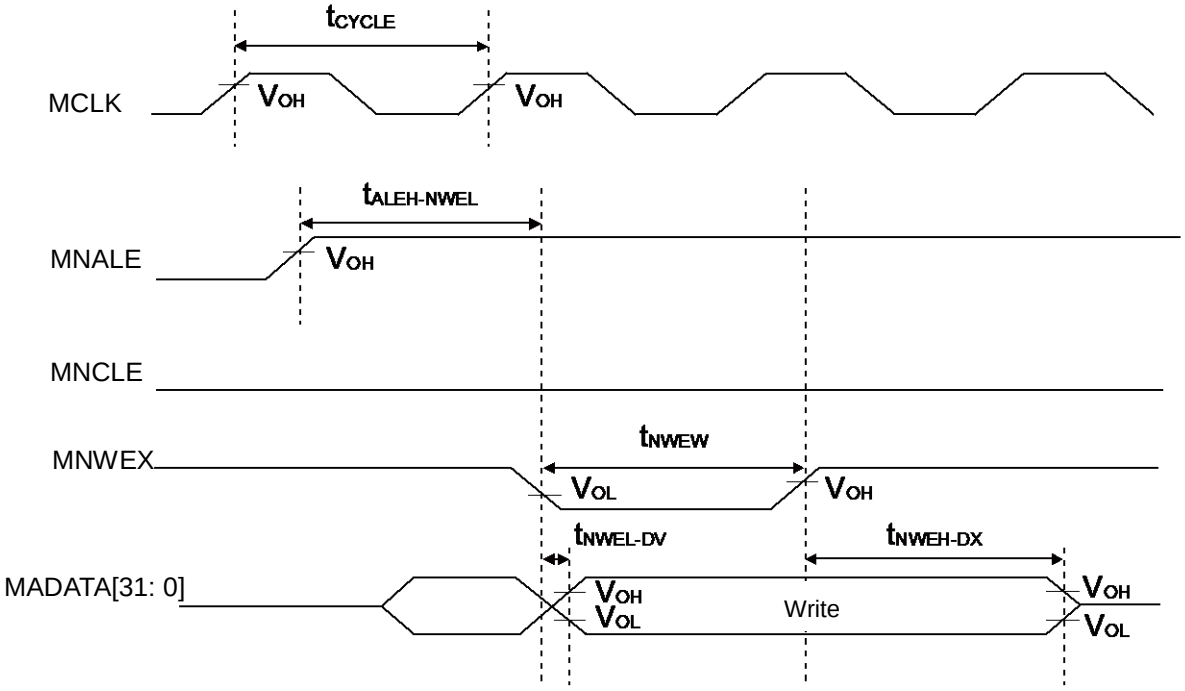
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24: 0]	-	0	10	ns	
Multiplexed address hold time	t_{CHMADH}		-	MCLK×n+0	MCLK×n+10	ns	

Note:

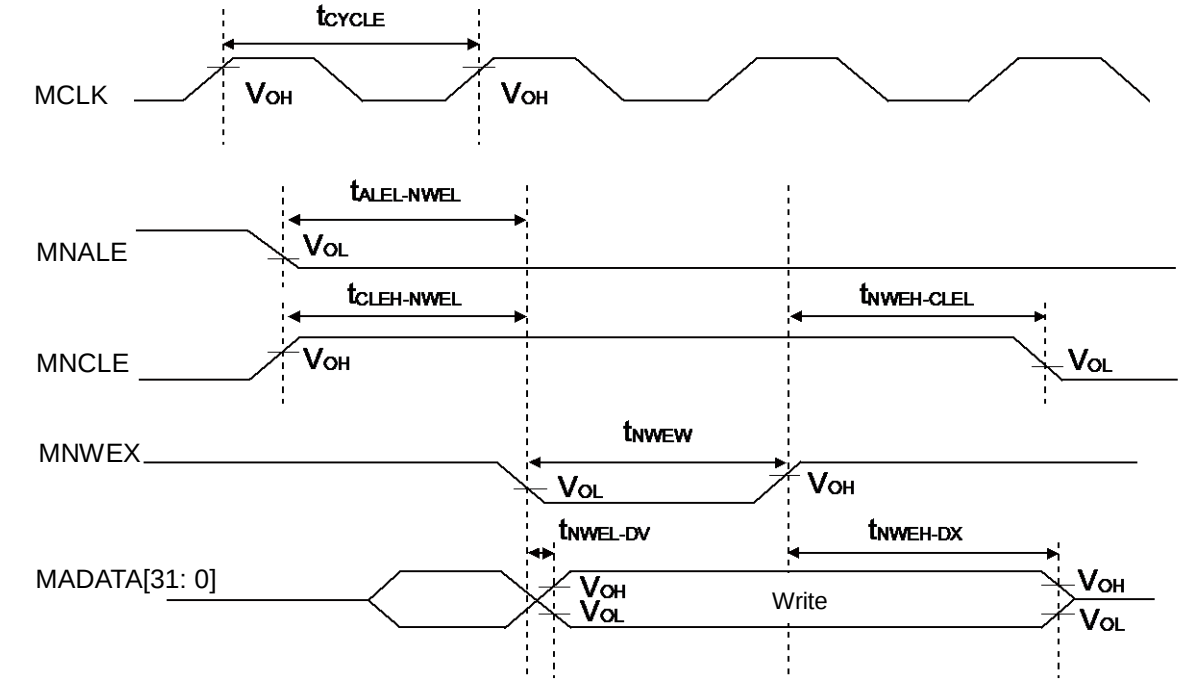
- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*



NAND Flash Address Write



NAND Flash Command Write



When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

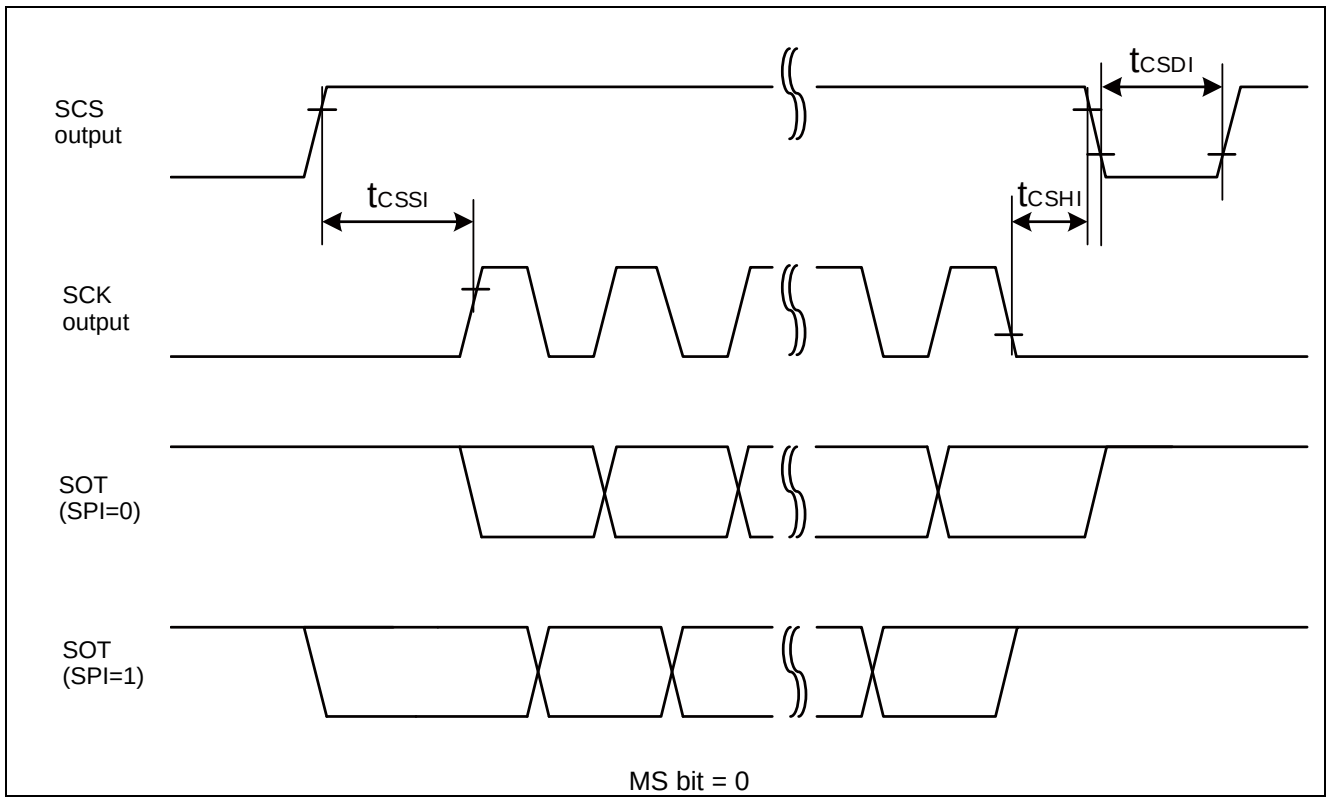
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

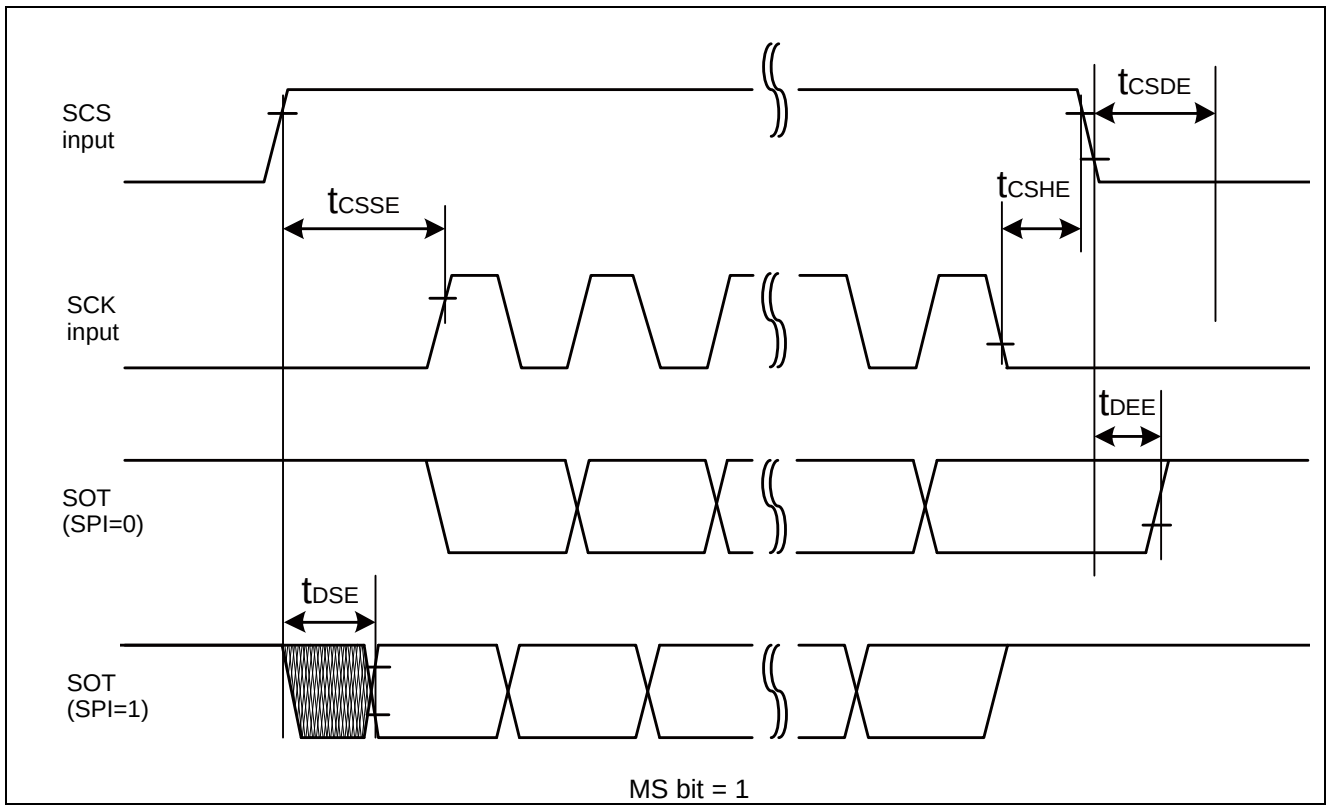
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

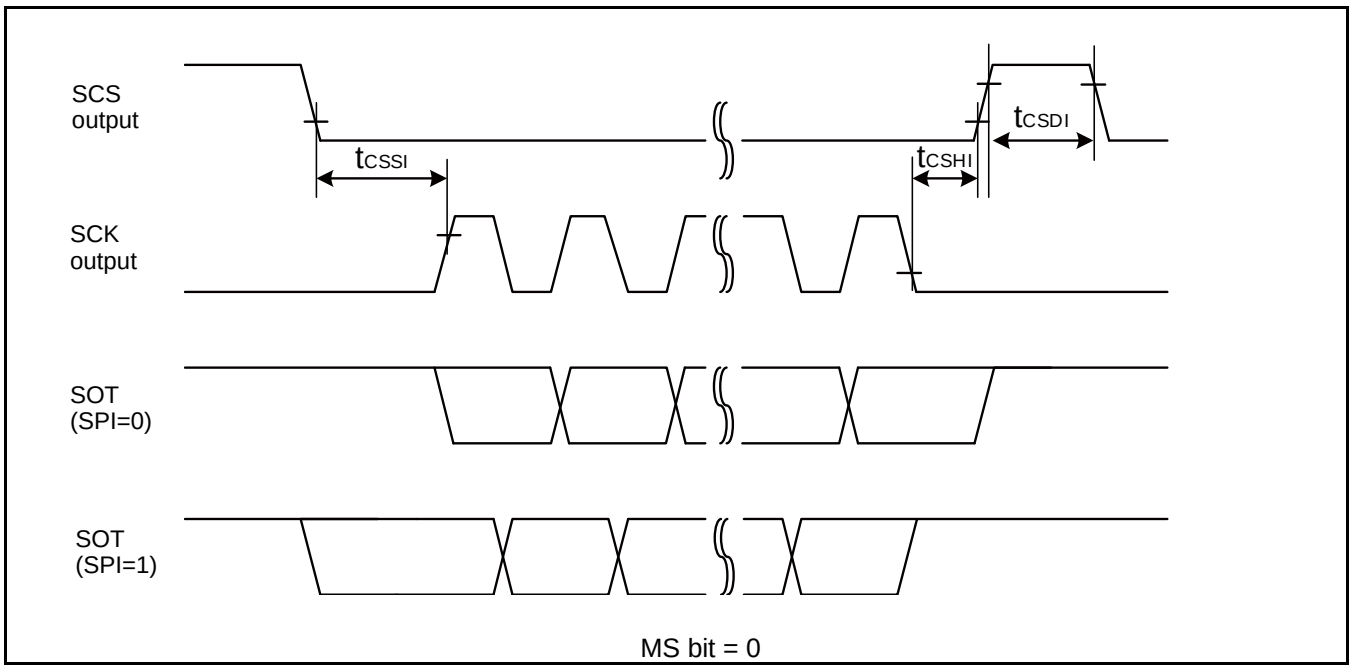
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



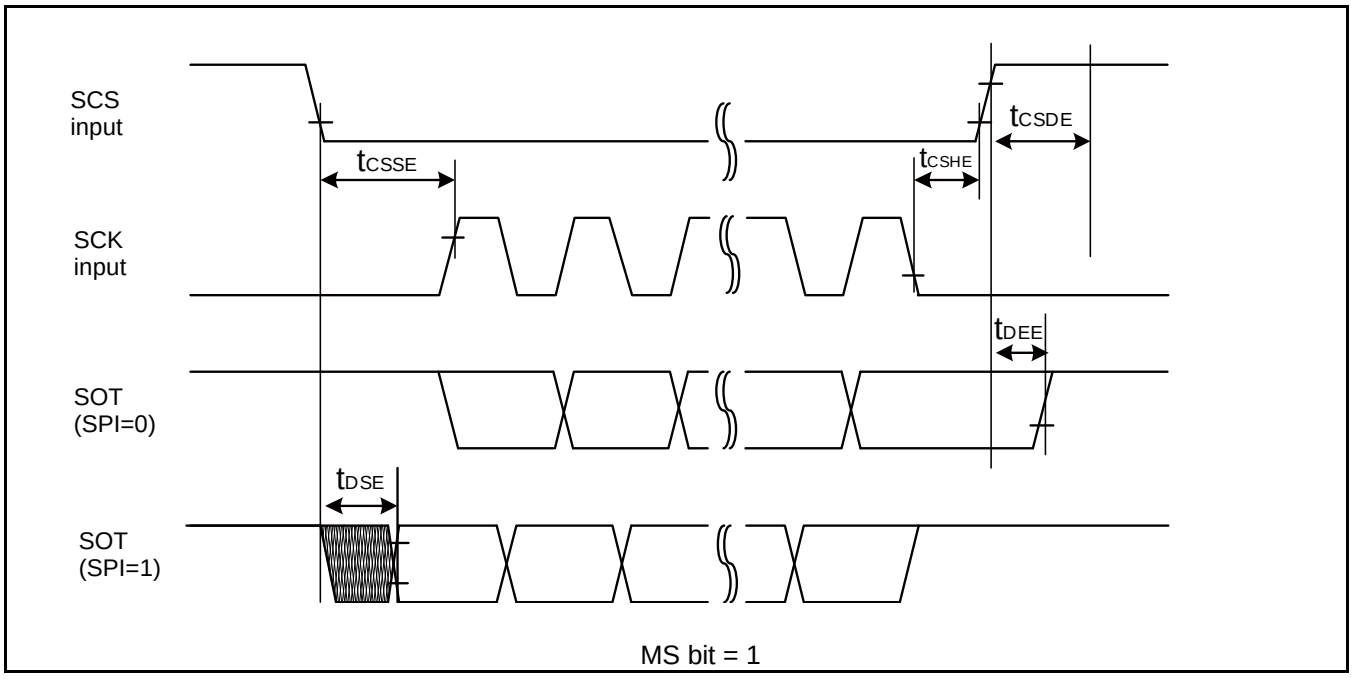
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

12.4.19 I²S Timing

Master Mode Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDI}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

*: Except for the first bit of transmission frame

Notes:

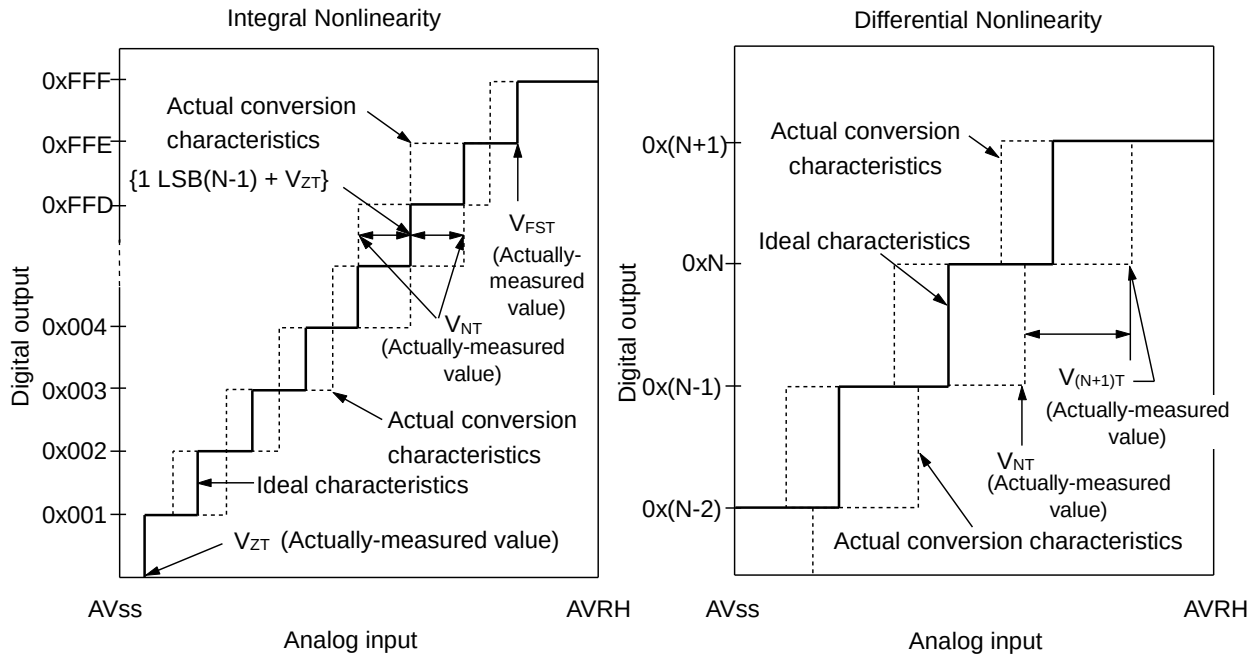
- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.

Definition of 12-bit A/D Converter Terms

■ Resolution: Analog variation that is recognized by an A/D converter.

■ Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.

■ Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



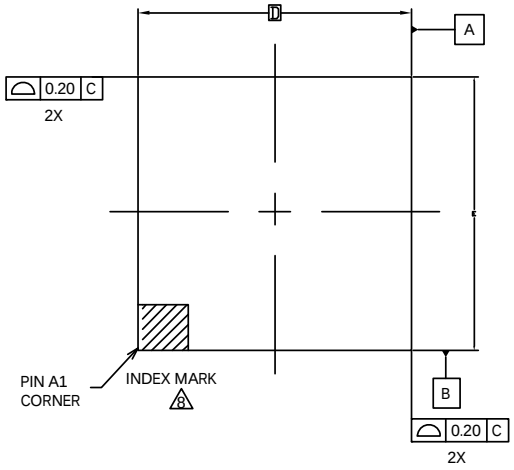
$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

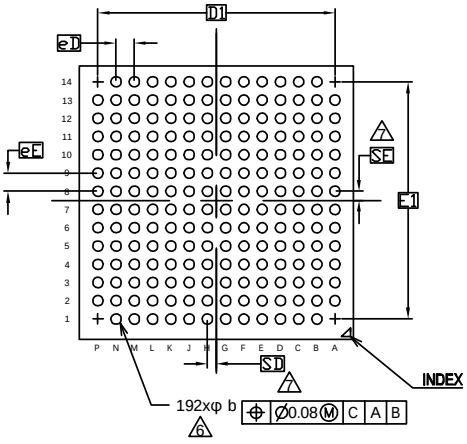
$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

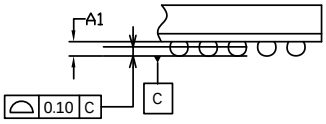
Package Type	Package Code
PFBGA 192	LBE 192



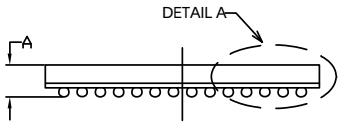
TOP VIEW



BOTTOM VIEW



DETAIL A



SIDE VIEW

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.45
A1	0.25	0.35	0.45
D	12.00 BSC		
E	12.00 BSC		
D1	10.40 BSC		
E 1	10.40 BSC		
MD	14		
ME	14		
n	192		
Φb	0.35	0.45	0.55
eD	0.80 BSC		
eE	0.80 BSC		
SD / SE	0.40 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-13493 **

PACKAGE OUTLINE, 192 BALL FBGA
12.00X12.00X1.45 MM LBE192 REV**