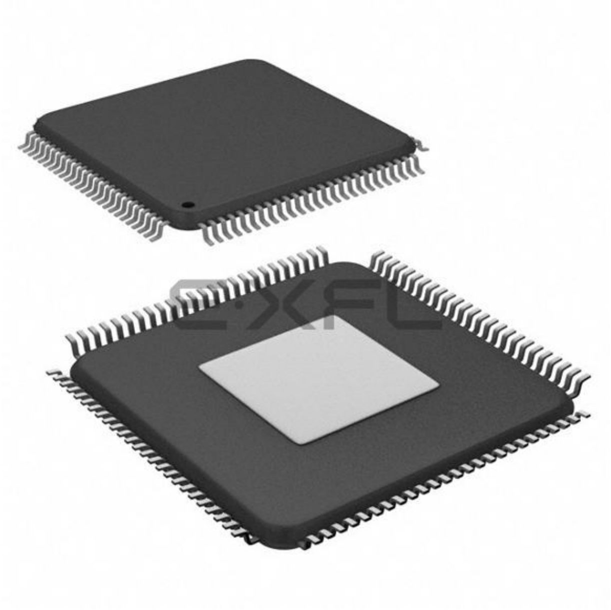
Infineon Technologies - XC226756F66LACKXUMA1 Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc226756f66lackxuma1

Data Sheet, V2.1, Aug. 2008

XC226x

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

Microcontrollers

Never stop thinking

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	I	St/B	**JTAG Test Mode Selection Input**
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
8	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	CCU62_CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**
9	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_SCLKOUT	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU62_CCPOS2A	I	St/B	**CCU62 Position Input 2**
	TCK_C	I	St/B	**JTAG Clock Input**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**
11	P6.0	O0 / I	St/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	St/A	**External Analog MUX Control Output 0 (ADC0)**
	$\overline{\text{BRKOUT}}$	O3	St/A	**OCDS Break Signal Output**
	ADCx_REQGTyC	I	St/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	St/A	**USIC1 Channel 1 Shift Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
69	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	AD4	OH / I	St/B	**External Bus Interface Address/Data Line 4**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
70	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLKOUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COUT62	O2	St/B	**CCU60 Channel 2 Output**
	AD5	OH / I	St/B	**External Bus Interface Address/Data Line 5**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
71	P0.6	O0 / I	St/B	**Bit 6 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CCU61_ COUT63	O3	St/B	**CCU61 Channel 3 Output**
	A6	OH	St/B	**External Bus Interface Address Line 6**
	U1C1_DX0A	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_ CTRAPA	I	St/B	**CCU61 Emergency Trap Input**
	U1C1_DX1B	I	St/B	**USIC1 Channel 1 Shift Clock Input**
72	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	U1C0_ SELO0	O3	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	AD6	OH / I	St/B	**External Bus Interface Address/Data Line 6**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX2D	I	St/B	**USIC1 Channel 0 Shift Control Input**
	CCU60_ CTRAPA	I	St/B	**CCU60 Emergency Trap Input**
73	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_ COUT63	O2	St/B	**CCU60 Channel 3 Output**
	AD7	OH / I	St/B	**External Bus Interface Address/Data Line 7**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_ CCPOS0A	I	St/B	**CCU60 Position Input 0**
	RxDC4C	I	St/B	**CAN Node 4 Receive Data Input**

Table 4 **Pin Definitions and Functions** (cont'd)

Pin	Symbol	Ctrl.	Type	Function
83	P10.11	O0 / I	St/B	**Bit 11 of Port 10, General Purpose Input/Output**
	U1C0_ SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
	AD11	OH / I	St/B	**External Bus Interface Address/Data Line 11**
	U1C0_DX1D	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	RxDC2B	I	St/B	**CAN Node 2 Receive Data Input**
	TMS_B	I	St/B	**JTAG Test Mode Selection Input**
84	P1.2	O0 / I	St/B	**Bit 2 of Port 1, General Purpose Input/Output**
	CCU62_ CC62	O1 / I	St/B	**CCU62 Channel 2 Input/Output**
	U1C0_ SELO6	O2	St/B	**USIC1 Channel 0 Select/Control 6 Output**
	U2C1_ SCLKOUT	O3	St/B	**USIC2 Channel 1 Shift Clock Output**
	A10	OH	St/B	**External Bus Interface Address Line 10**
	ESR1_4	I	St/B	**ESR1 Trigger Input 4**
	CCU61_ T12HRB	I	St/B	**External Run Control Input for T12 of CCU61**
	EX2AINA	I	St/B	**External Interrupt Trigger Input**
	U2C1_DX0D	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX1C	I	St/B	**USIC2 Channel 1 Shift Clock Input**
85	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	TDO_B	O3	St/B	**JTAG Test Data Output**
	AD12	OH / I	St/B	**External Bus Interface Address/Data Line 12**
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**

With this hardware most XC226x instructions can be executed in a single machine cycle of 12.5 ns with an 80-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XC226x instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Up to five independent CAN nodes
- Up to 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.13 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 μs and 13.4 s can be monitored (@ 80 MHz).
The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

3.14 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XC226x from a number of external or internal clock sources:

- External clock signals with pad or core voltage levels
- External crystal using the on-chip oscillator
- On-chip clock source for operation without crystal
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals or from the on-chip clock source. See also **Section 4.6.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

3.15 Parallel Ports

The XC226x provides up to 75 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 9**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 9 Summary of the XC226x's Parallel Ports

Port	Width	Alternate Functions
Port 0	8	Address lines, Serial interface lines of USIC1, CAN0, and CAN1, Input/Output lines for CCU61
Port 1	8	Address lines, Serial interface lines of USIC1 and USIC2, Input/Output lines for CCU62, OCDS control, interrupts
Port 2	13	Address and/or data lines, bus control, Serial interface lines of USIC0, CAN0, and CAN1, Input/Output lines for CCU60, CCU63, and CAPCOM2, Timer control signals, JTAG, interrupts, system clock output
Port 4	8	Chip select signals, Serial interface lines of CAN2, Input/Output lines for CAPCOM2, Timer control signals
Port 5	16	Analog input channels to ADC0, Input/Output lines for CCU6x, Timer control signals, JTAG, OCDS control, interrupts

Pullup/Pulldown Device Behavior

Most pins of the XC226x feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 12** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

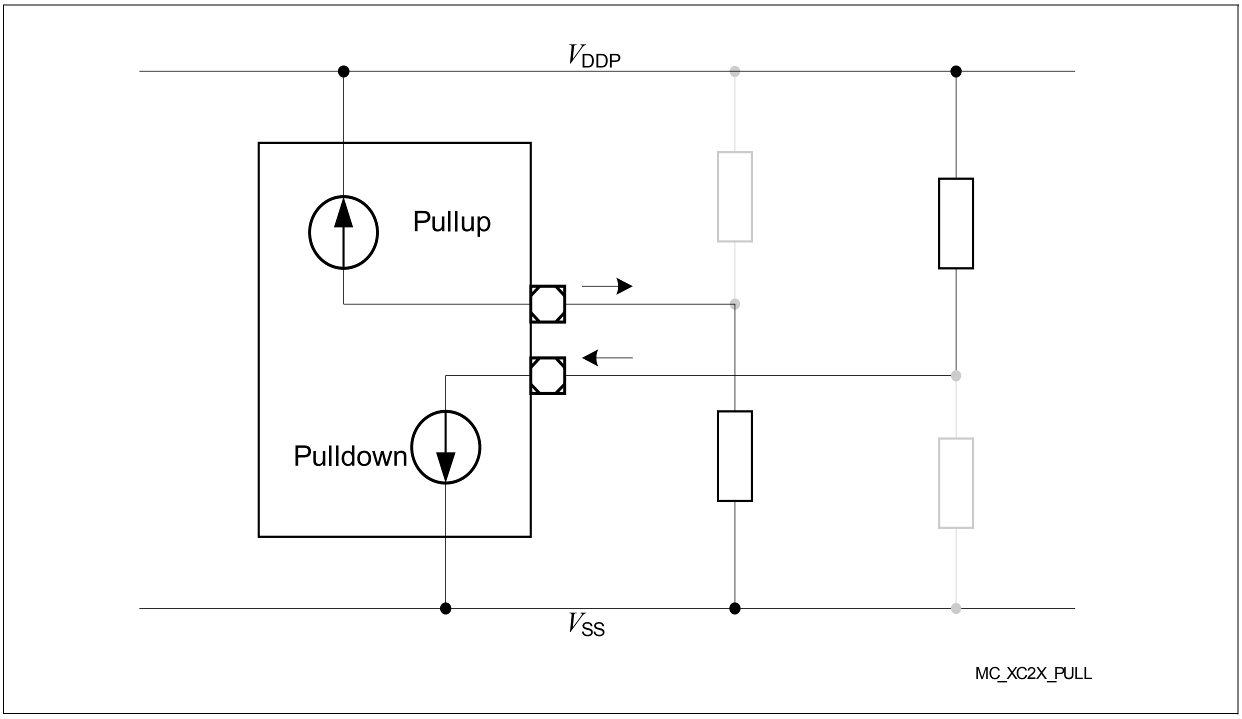


Figure 12 Pullup/Pulldown Current Definition

Table 18 A/D Converter Characteristics (cont'd)
(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Switched capacitance of the reference input	C_{AREFS}	CC	–	7	pF	[6)7)]
Resistance of the reference input path	R_{AREF}	CC	–	2	kΩ	[6)7)]

1) TUE is tested at $V_{AREFx} = V_{DDPA}$, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if the absolute sum of input overload currents on Port 5 or Port 15 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

2) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.

4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{ADCI} depend on programming and are found in **Table 19**.

5) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.

6) Not subject to production test - verified by design/characterization.

7) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

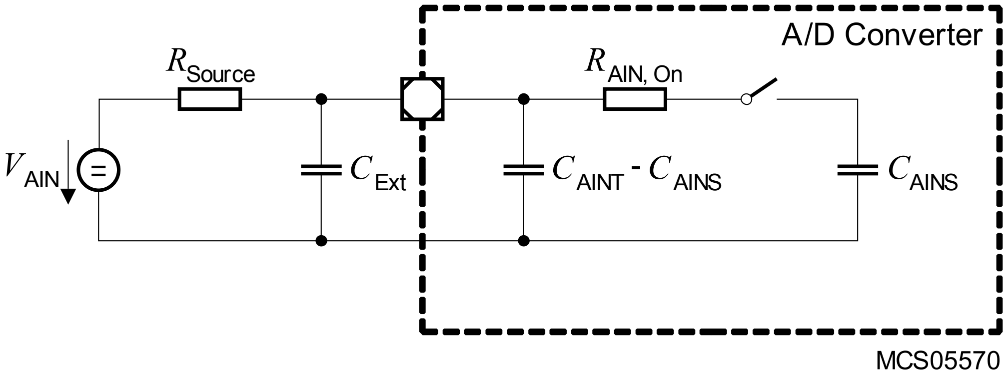


Figure 15 Equivalent Circuitry for Analog Inputs

Sample time and conversion time of the XC226x's A/D converters are programmable. The timing above can be calculated using **Table 19**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 19 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time t_S
000000_B	f_{SYS}	00_H	$t_{\mathrm{ADCI}} \times 2$
000001_B	$f_{\mathrm{SYS}} / 2$	01_H	$t_{\mathrm{ADCI}} \times 3$
000010_B	$f_{\mathrm{SYS}} / 3$	02_H	$t_{\mathrm{ADCI}} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{\mathrm{ADCI}} \times$ (STC+2)
111110_B	$f_{\mathrm{SYS}} / 63$	FE_H	$t_{\mathrm{ADCI}} \times 256$
111111_B	$f_{\mathrm{SYS}} / 64$	FF_H	$t_{\mathrm{ADCI}} \times 257$

Converter Timing Example A:

Assumptions: f_{SYS} = 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock $f_{\mathrm{ADCI}} = f_{\mathrm{SYS}} / 4$ = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time $t_S = t_{\mathrm{ADCI}} \times 2$ = 100 ns

Conversion 10-bit:

$t_{C10} = 13 \times t_{\mathrm{ADCI}} + 2 \times t_{\mathrm{SYS}} = 13 \times 50\ \mathrm{ns} + 2 \times 12.5\ \mathrm{ns} = 0.675\ \mu\mathrm{s}$

Conversion 8-bit:

$t_{C8} = 11 \times t_{\mathrm{ADCI}} + 2 \times t_{\mathrm{SYS}} = 11 \times 50\ \mathrm{ns} + 2 \times 12.5\ \mathrm{ns} = 0.575\ \mu\mathrm{s}$

Converter Timing Example B:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02_H, STC = 03_H
Analog clock $f_{\mathrm{ADCI}} = f_{\mathrm{SYS}} / 3$ = 13.3 MHz, i.e. t_{ADCI} = 75 ns
Sample time $t_S = t_{\mathrm{ADCI}} \times 5$ = 375 ns

Conversion 10-bit:

$t_{C10} = 16 \times t_{\mathrm{ADCI}} + 2 \times t_{\mathrm{SYS}} = 16 \times 75\ \mathrm{ns} + 2 \times 25\ \mathrm{ns} = 1.25\ \mu\mathrm{s}$

Conversion 8-bit:

$t_{C8} = 14 \times t_{\mathrm{ADCI}} + 2 \times t_{\mathrm{SYS}} = 14 \times 75\ \mathrm{ns} + 2 \times 25\ \mathrm{ns} = 1.10\ \mu\mathrm{s}$

4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XC226x into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 20 Various System Parameters

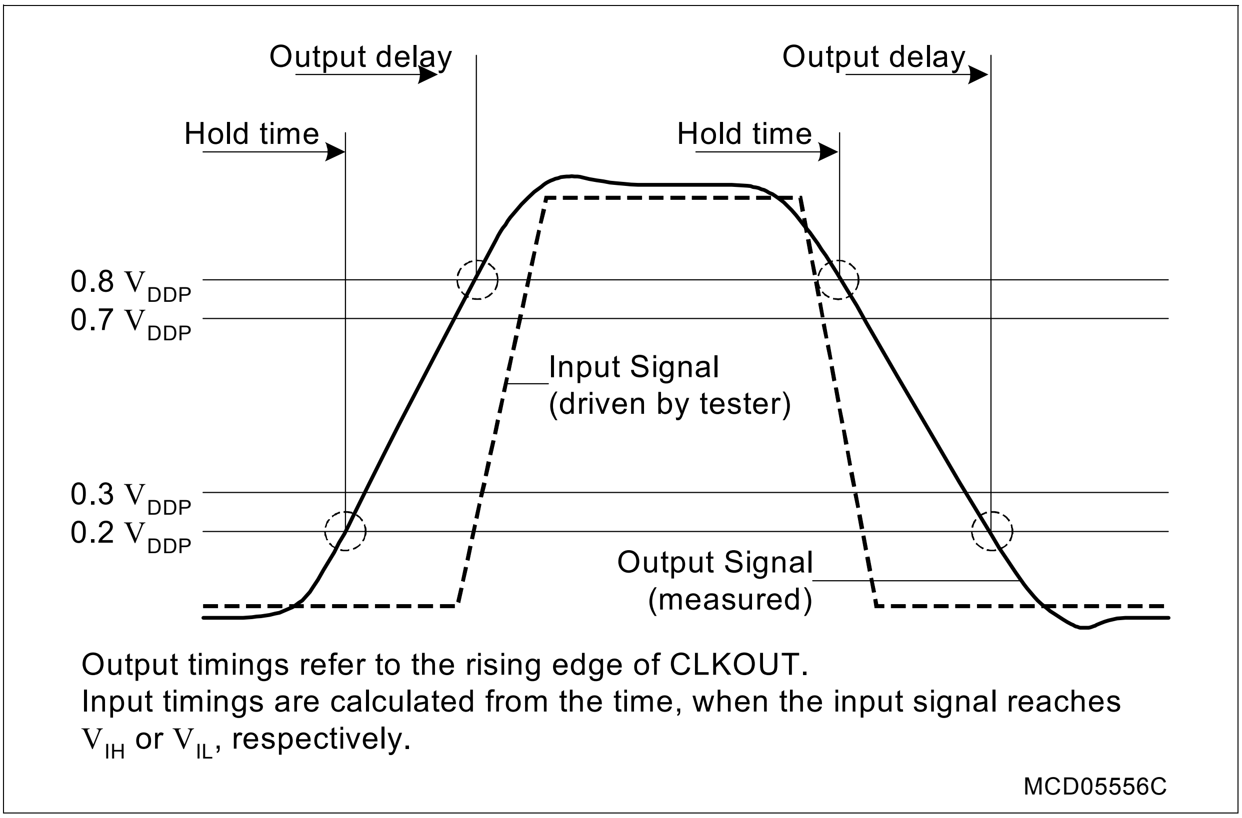
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply watchdog (SWD) supervision level (see **Table 21**)	V_{SWD} CC	V_{LV} - 0.150	V_{LV}	V_{LV} + 0.100	V	V_{LV} = selected voltage in upper voltage area
		V_{LV} - 0.125	V_{LV}	V_{LV} + 0.050	V	V_{LV} = selected voltage in lower voltage area
Core voltage (PVC) supervision level (see **Table 22**)	V_{PVC} CC	V_{LV} - 0.070	V_{LV}	V_{LV} + 0.030	V	V_{LV} = selected voltage
Current control limit	I_{CC} CC	13	–	30	mA	Power domain DMP_M
		90	–	150	mA	Power domain DMP_1
Wakeup clock source frequency	f_{WU} CC	400	500	600	kHz	FREQSEL = 00_B
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Startup time from stopover mode	t_{SSO} CC	200	260	320	µs	User instruction from PSRAM
Startup time from standby mode	t_{SSB} CC	2.5	2.8	3.5	ms	User instruction from Flash

4.6 AC Parameters

These parameters describe the dynamic behavior of the XC226x.

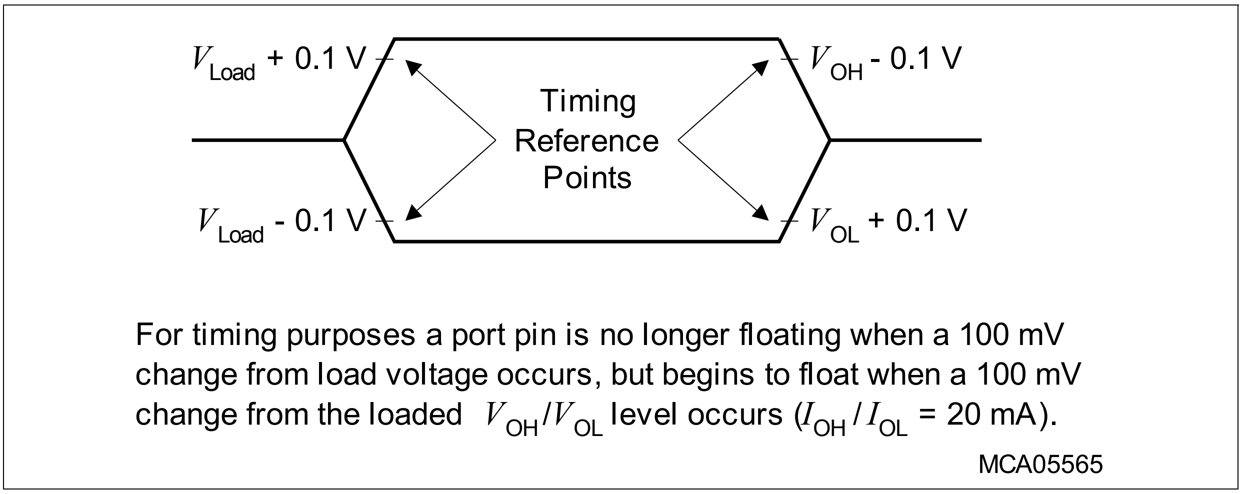
4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

Figure 16 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

Figure 17 Floating Waveforms

4.6.2 Definition of Internal Timing

The internal operation of the XC226x is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XC226x.

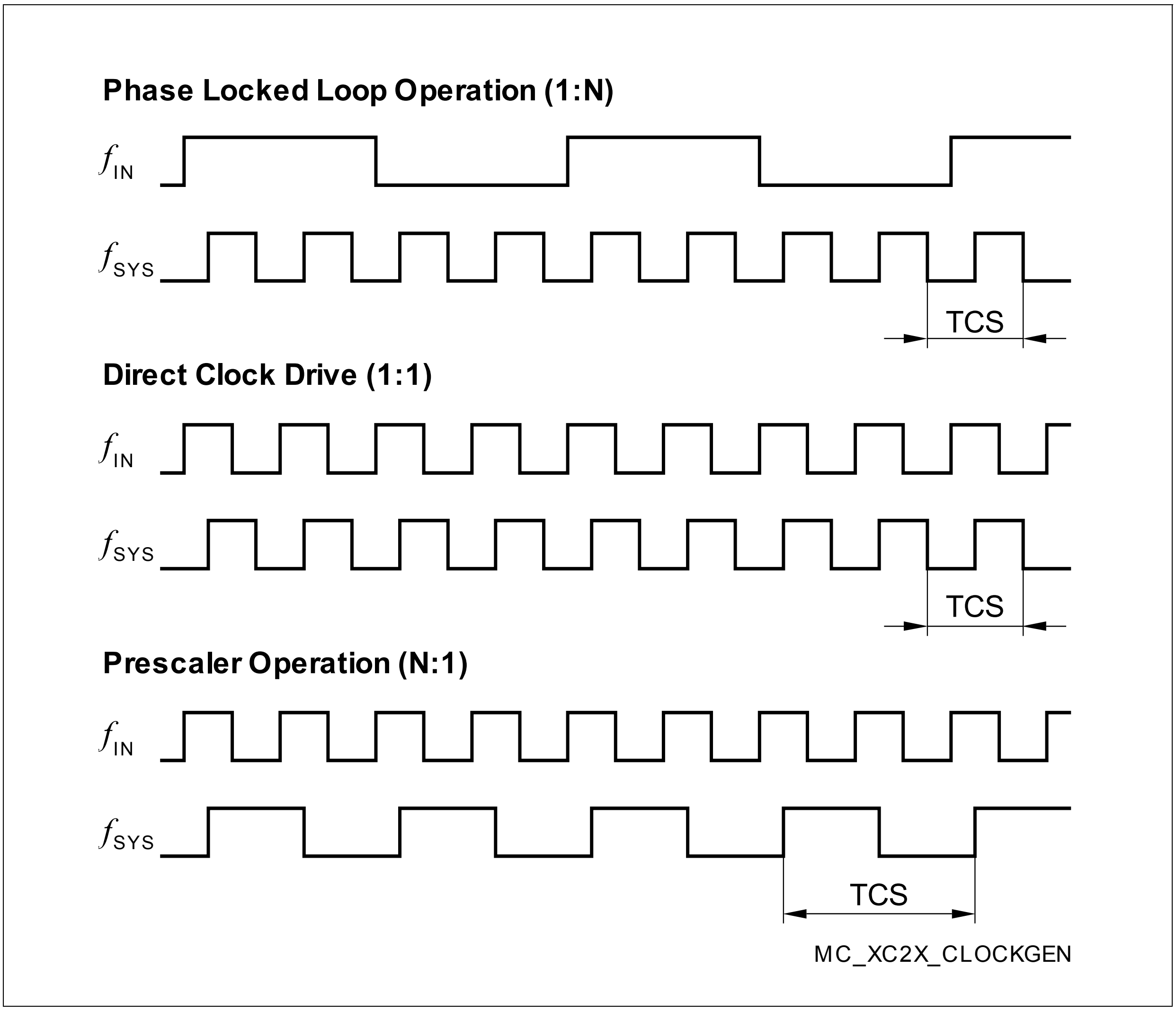


Figure 18 Generation Mechanisms for the System Clock

Note: The example of PLL operation shown in ***Figure 18*** *uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XC226x. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. In connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Table 26 External Clock Input Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDI}	–	1.7	V	[1]
Input voltage (amplitude) on XTAL1	V_{AX1} SR	0.3 × V_{DDI}	–	–	V	Peak-to-peak voltage[2]
XTAL1 input current	I_{IL} CC	–	–	±20	µA	$0\ \mathrm{V} < V_{\mathrm{IN}} < V_{\mathrm{DDI}}$
Oscillator frequency	f_{OSC} CC	4	–	40	MHz	Clock signal
		4	–	16	MHz	Crystal or Resonator
High time	t_1 SR	6	–	–	ns	
Low time	t_2 SR	6	–	–	ns	
Rise time	t_3 SR	–	8	8	ns	
Fall time	t_4 SR	–	8	8	ns	

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

4.6.4 External Bus Timing

The following parameters specify the behavior of the XC226x bus interface.

Table 27 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit	Note / Test Condition
			Min.	Max.		
CLKOUT cycle time	t_5	CC	40/25/12.5[1]		ns	
CLKOUT high time	t_6	CC	3	–	ns	
CLKOUT low time	t_7	CC	3	–	ns	
CLKOUT rise time	t_8	CC	–	3	ns	
CLKOUT fall time	t_9	CC	–	3	ns	

[1] The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{SYS} = 25/40/80 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

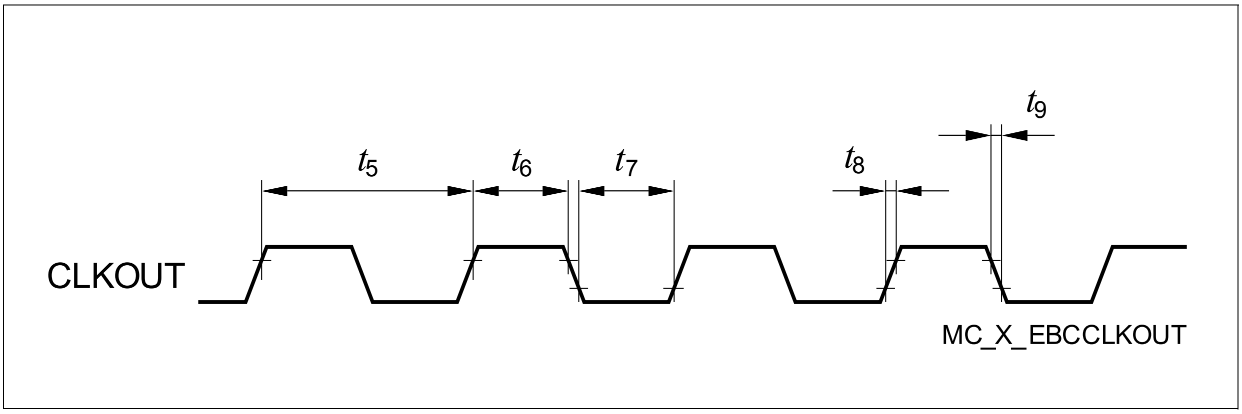


Figure 21 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

4.6.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 31 SSC Master/Slave Mode Timing for Upper Voltage Range (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	–	[1]	ns	[2]
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$0.5 \times t_{BIT}$	–	[3]	ns	
Transmit data output valid time	t_3 CC	-6	–	13	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-7	–	–	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	7	–	–	ns	[4]
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	5	–	–	ns	[4]
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	7	–	–	ns	[4]
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	5	–	–	ns	[4]
Data output DOUT valid time	t_{14} CC	8	–	29	ns	[4]

[1] The maximum value further depends on the settings for the slave select output leading delay.

[2] $t_{SYS} = 1/f_{SYS}$ (= 12.5 ns @ 80 MHz)

[3] The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.

[4] These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).