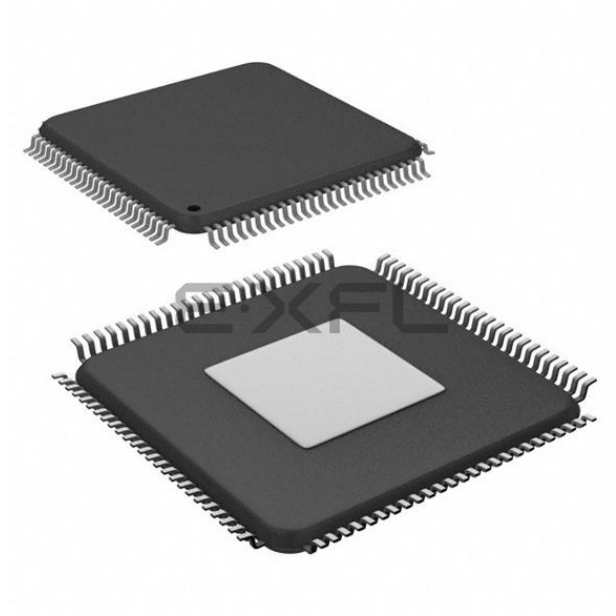

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Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc226796f80lackxuma1

2 General Device Information

The XC226x derivatives are high-performance members of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

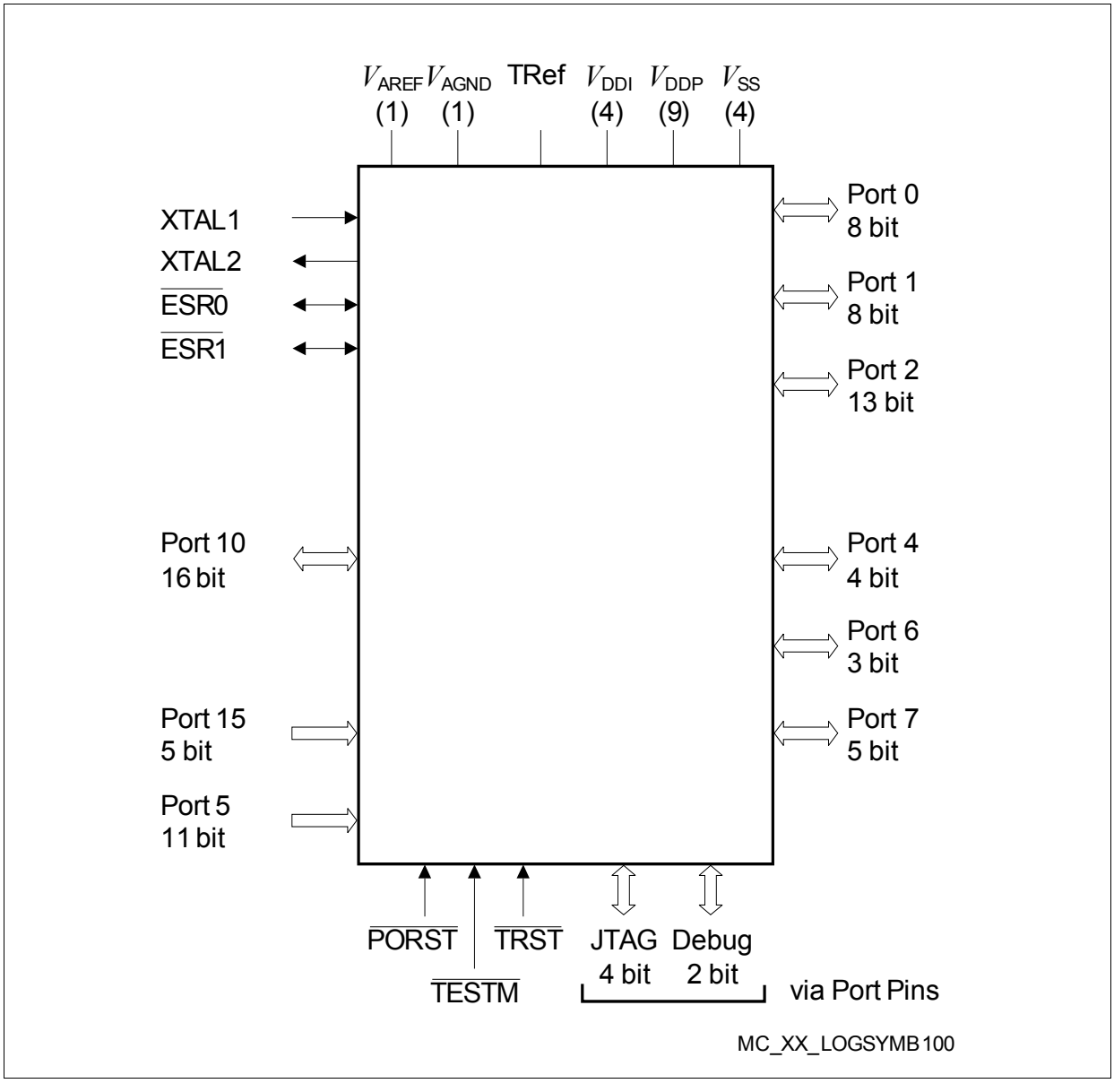

Figure 1 Logic Symbol

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
45	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	A17	OH	St/B	**External Bus Interface Address Line 17**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**
46	P2.5	O0 / I	St/B	**Bit 5 of Port 2, General Purpose Input/Output**
	U0C0_ SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_18	O3 / I	St/B	**CAPCOM2 CC18IO Capture Inp./ Compare Out.**
	A18	OH	St/B	**External Bus Interface Address Line 18**
	U0C0_DX1D	I	St/B	**USIC0 Channel 0 Shift Clock Input**
47	P4.2	O0 / I	St/B	**Bit 2 of Port 4, General Purpose Input/Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_26	O3 / I	St/B	**CAPCOM2 CC26IO Capture Inp./ Compare Out.**
	$\overline{CS2}$	OH	St/B	**External Bus Interface Chip Select 2 Output**
	T2IN	I	St/B	**GPT1 Timer T2 Count/Gate Input**
48	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_ SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_ SELO1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	A19	OH	St/B	**External Bus Interface Address Line 19**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	RxDC0D	I	St/B	**CAN Node 0 Receive Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
99	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** *Note: After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.*
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**
10	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see **Table 12** for details.
38, 64, 88	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see **Table 12** for details. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6, and P15 are fed from supply voltage V_{DDPA}.*
2, 25, 27, 50, 52, 75, 77, 100	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6, and P15 are fed from supply voltage V_{DDPB}.*
1, 26, 51, 76	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected to V_{SS}. The respective board area must be connected to ground (if soldered) or left free.*

1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC2000 Family. In order to to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 5**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

Up to 768 Kbytes of on-chip Flash memory store code, constant data, and control data. The on-chip Flash memory consists of up to three modules with a maximum capacity of 256 Kbytes each. Each module is organized in 4-Kbyte sectors.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

*Note: The actual size of the Flash memory depends on the chosen derivative (see **Table 1**).*

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.5**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

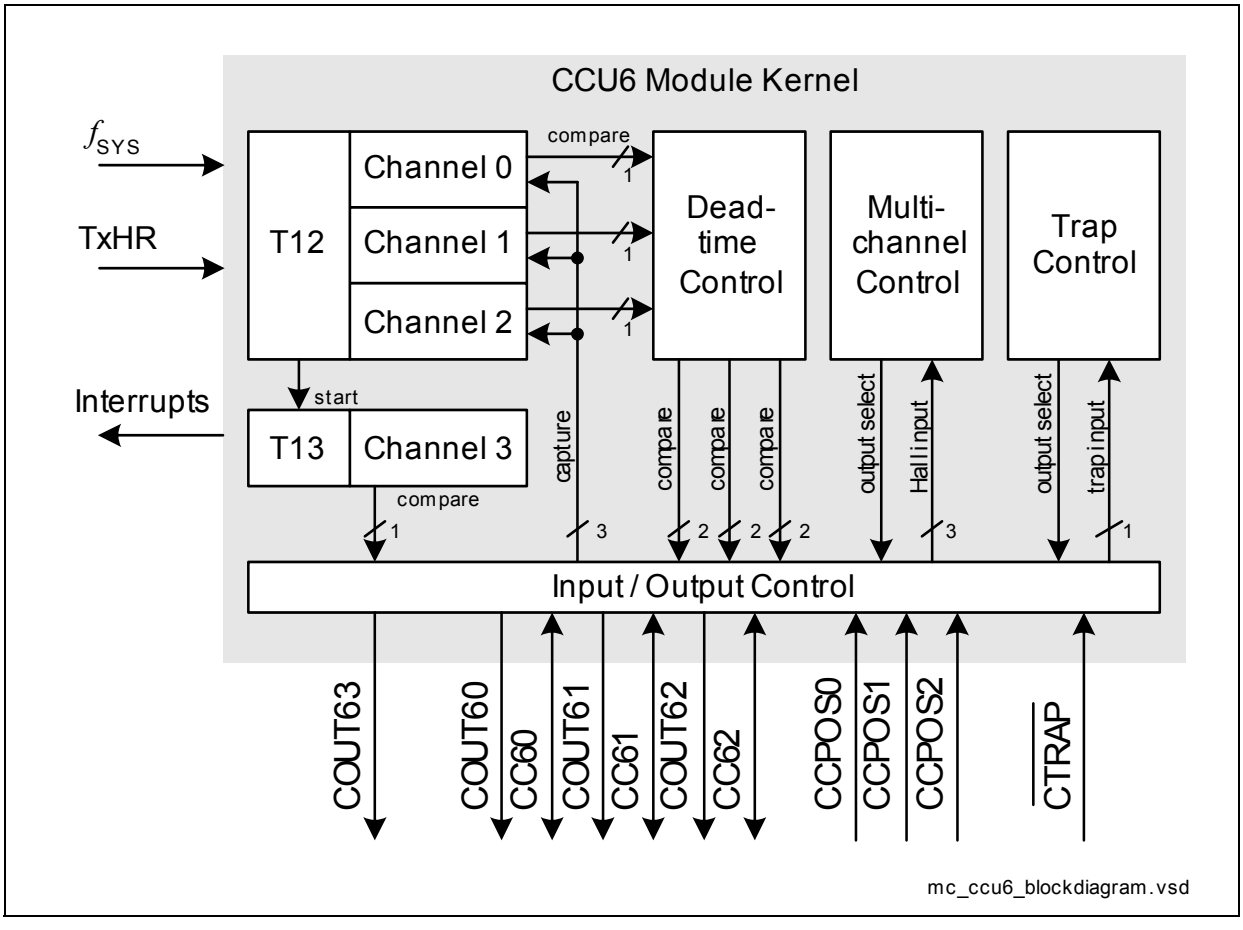

Figure 6 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

Table 9 Summary of the XC226x's Parallel Ports (cont'd)

Port	Width	Alternate Functions
Port 6	4	ADC control lines, Serial interface lines of USIC1, Timer control signals, OCDS control
Port 7	5	ADC control lines, Serial interface lines of USIC0 and CAN4, Input/Output lines for CCU62, Timer control signals, JTAG, OCDS control,system clock output
Port 10	16	Address and/or data lines, bus control, Serial interface lines of USIC0, USIC1, CAN2, CAN3, and CAN4, Input/Output lines for CCU60, JTAG, OCDS control
Port 15	8	Analog input channels to ADC1, Timer control signals

3.16 Power Management

The XC226x provides the means to control the power it consumes either at a given time or averaged over a certain duration.
Three mechanisms can be used (and partly in parallel):

- **Supply Voltage Management** permits the temporary reduction of the supply voltage of major parts of the logic or even its complete disconnection. This drastically reduces the power consumed because it eliminates leakage current, particularly at high temperature.
  Several power reduction modes provide the best balance of power reduction and wake-up time.
- **Clock Generation Management** controls the frequency of internal and external clock signals. Clock signals for currently inactive parts of logic are disabled automatically. The user can drastically reduce the consumed power by reducing the XC226x system clock frequency.
  External circuits can be controlled using the programmable frequency output EXTCLK.
- **Peripheral Management** permits temporary disabling of peripheral modules. Each peripheral can be disabled and enabled separately. The CPU can be switched off while the peripherals can continue to operate.

Wake-up from power reduction modes can be triggered either externally with signals generated by the external system, or internally by the on-chip wake-up timer. This supports intermittent operation of the XC226x by generating cyclic wake-up signals. Full performance is available to quickly react to action requests while the intermittent sleep phases greatly reduce the average system power consumption.

Note: When selecting the supply voltage and the clock source and generation method, the required parameters must be carefully written to the respective bitfields, to avoid unintended intermediate states. Recommended sequences are provided which ensure the intended operation of power supply system and clock system. Please refer to the Programmer's Guide.

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XC226x, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC226x. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 12 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital core supply voltage	V_{DDI}	1.4	–	1.6	V	
Core Supply Voltage Difference	ΔVDDI	-10	–	+10	mV	V_{DDIM} - V_{DDI1} 1)
Digital supply voltage for IO pads and voltage regulators, upper voltage range	V_{DDPA}, V_{DDPB}	4.5	–	5.5	V	2)
Digital supply voltage for IO pads and voltage regulators, lower voltage range	V_{DDPA}, V_{DDPB}	3.0	–	4.5	V	2)
Digital ground voltage	V_{SS}	0	–	0	V	Reference voltage
Overload current	I_{OV}	-5	–	5	mA	Per IO pin 3)4)
		-2	–	5	mA	Per analog input pin 3)4)
Overload positive current coupling factor for analog inputs 5)	K_{OVA}	–	1.0×10^{-6}	1.0×10^{-4}	–	$I_{OV} > 0$
Overload negative current coupling factor for analog inputs 5)	K_{OVA}	–	2.5×10^{-4}	1.5×10^{-3}	–	$I_{OV} < 0$
Overload positive current coupling factor for digital I/O pins 5)	K_{OVD}	–	1.0×10^{-4}	5.0×10^{-3}	–	$I_{OV} > 0$
Overload negative current coupling factor for digital I/O pins 5)	K_{OVD}	–	1.0×10^{-2}	3.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	Σ|IOV|	–	–	50	mA	4)

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.
4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
6) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.
   The leakage current value is not tested in the lower voltage range but only in the upper voltage range. This parameter is ensured by correlation.
7) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
   Leakage derating depending on temperature (T_J = junction temperature [°C]):
   I_{OZ} = 0.03 × $e^{(1.35 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 130°C the resulting leakage current is 4.41 µA.
   Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
   I_{OZ} = $I_{OZtempmax}$ - (1.3 × DV) [µA]
   This voltage derating formula is an approximation which applies for maximum temperature.
   Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal leakage.
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
   Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
   These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) Not subject to production test - verified by design/characterization.
   Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal capacitance.

Table 17 Leakage Power Consumption XC226x (Operating Conditions apply)

Parameter	Sym-bol	Values			Unit	Note / Test Condition[1]
		Min.	Typ.	Max.		
Leakage supply current[2] (DMP_1 powered) Formula[3]: 600,000 × $e^{-\alpha}$; α = 5000 / (273 + B×T_J); Typ.: B = 1.0, Max.: B = 1.3	I_{LK1}	–	0.03	0.05	mA	T_J = 25°C
		–	0.5	1.3	mA	T_J = 85°C
		–	2.1	6.2	mA	T_J = 125°C
		–	4.4	13.7	mA	T_J = 150°C
Leakage supply current[2] (DMP_1 off) Formula[3]: 500,000 × $e^{-\alpha}$; α = 3000 / (273 + B×T_J); Typ.: B = 1.0, Max.: B = 1.6	I_{LK0}	–	20	35	µA	T_J = 25°C
		–	115	330	µA	T_J = 85°C
		–	270	880	µA	T_J = 125°C
		–	420	1,450	µA	T_J = 150°C

1) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

2) The supply current caused by leakage depends mainly on the junction temperature (see **Figure 14**) and the supply voltage. The temperature difference between the junction temperature T_J and the ambient temperature T_A must be taken into account. As this fraction of the supply current does not depend on device activity, it must be added to other power consumption values.

3) This formula is valid for temperatures above 0°C. For temperatures below 0°C a value of below 10 µA can be assumed.

4.6.2 Definition of Internal Timing

The internal operation of the XC226x is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XC226x.

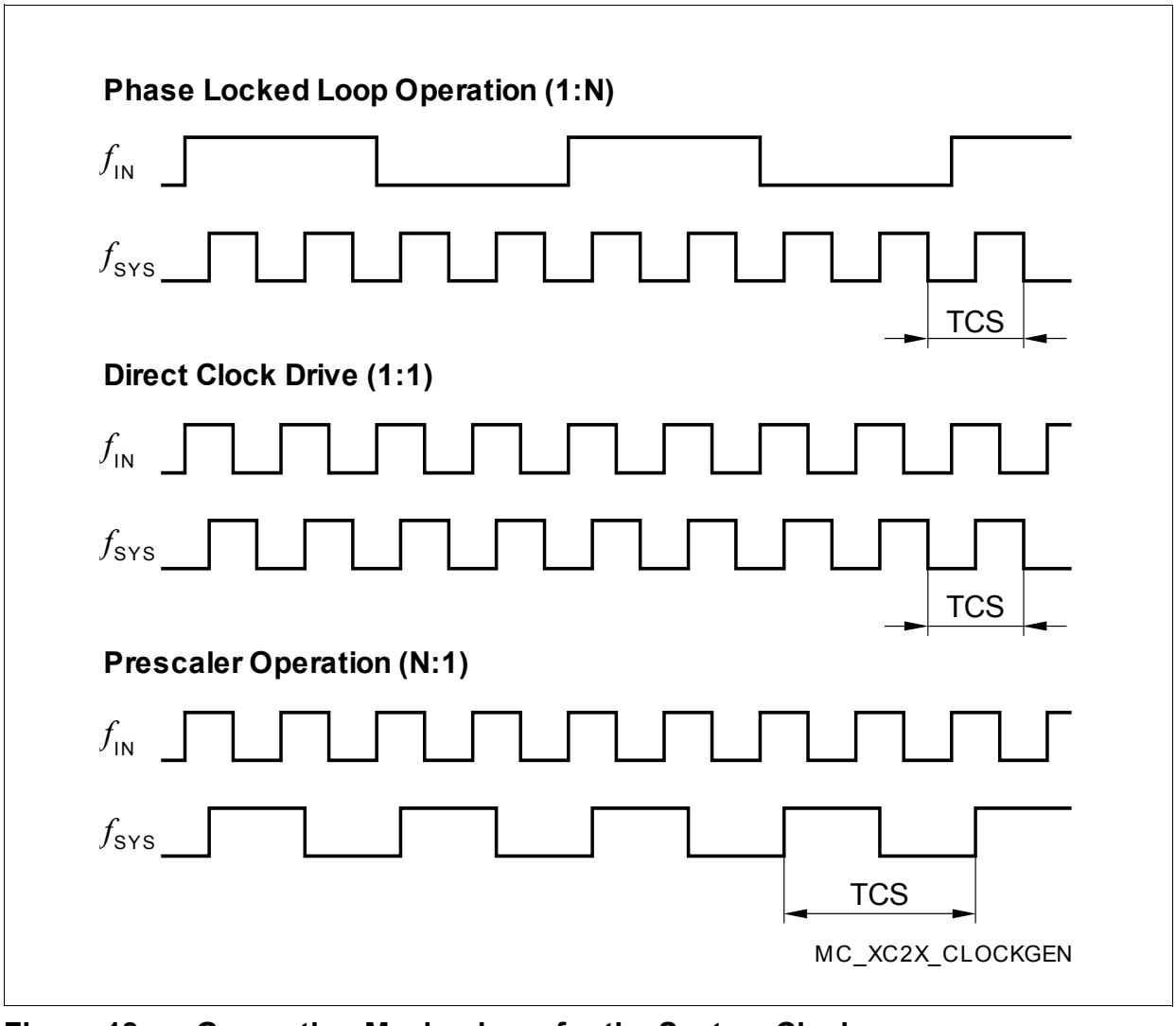

Figure 18 Generation Mechanisms for the System Clock

*Note: The example of PLL operation shown in **Figure 18** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

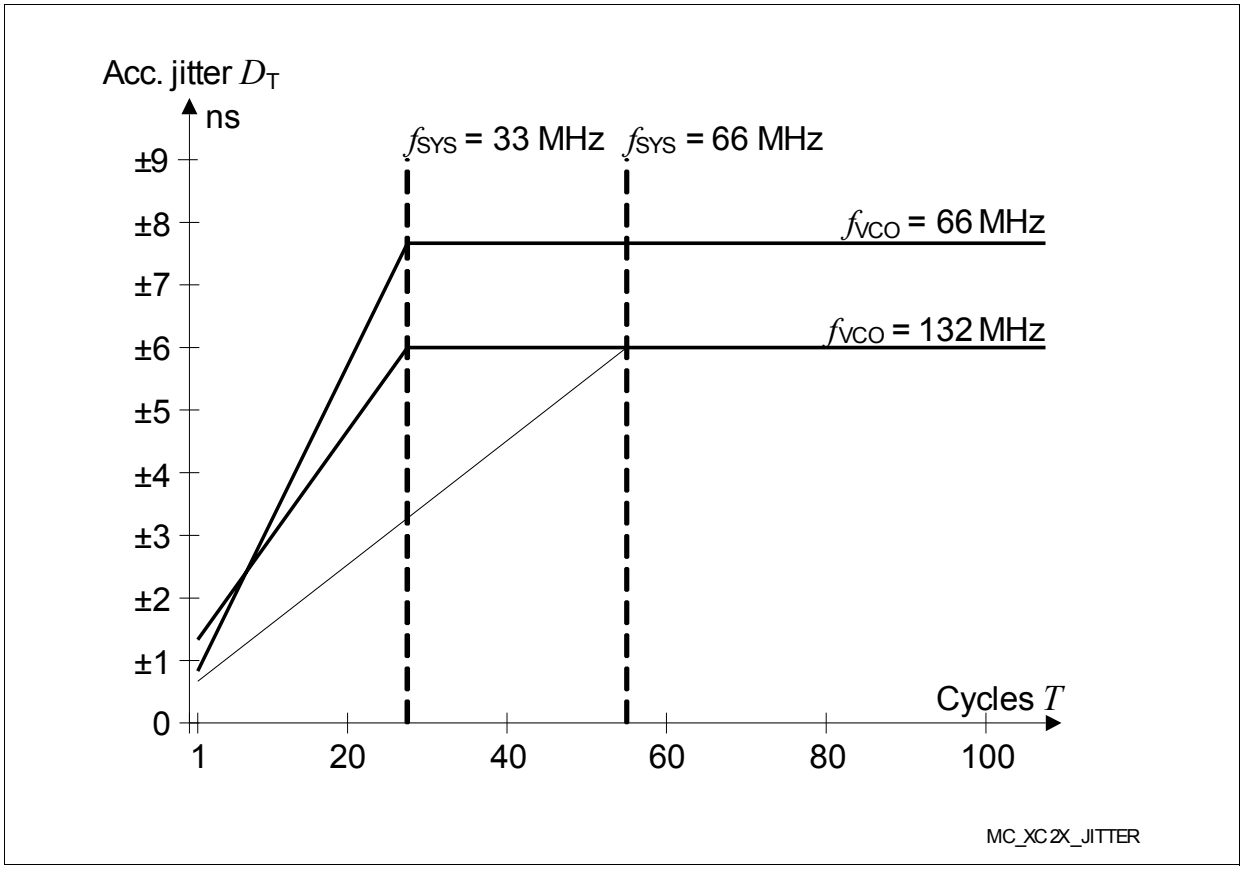

Figure 19 Approximated Accumulated PLL Jitter

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF (see **Table 12**).*
The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100/144 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 25 VCO Bands for PLL Operation[1)]

PLLCON0.VCOSEL	VCO Frequency Range	Base Frequency Range
00	50 … 110 MHz	10 … 40 MHz
01	100 … 160 MHz	20 … 80 MHz
1X	Reserved	

1) Not subject to production test - verified by design/characterization.

4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XC226x. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. In connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Table 26 External Clock Input Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDI}	–	1.7	V	1)
Input voltage (amplitude) on XTAL1	V_{AX1} SR	0.3 × V_{DDI}	–	–	V	Peak-to-peak voltage2)
XTAL1 input current	I_{IL} CC	–	–	±20	µA	0 V < V_{IN} < V_{DDI}
Oscillator frequency	f_{OSC} CC	4	–	40	MHz	Clock signal
		4	–	16	MHz	Crystal or Resonator
High time	t_1 SR	6	–	–	ns	
Low time	t_2 SR	6	–	–	ns	
Rise time	t_3 SR	–	8	8	ns	
Fall time	t_4 SR	–	8	8	ns	

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

Table 30 External Bus Cycle Timing for Lower Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: RD, WR(L/H)	t_{10} CC	–		20	ns	
Output valid delay for: BHE, ALE	t_{11} CC	–		20	ns	
Output valid delay for: A23 … A16, A15 … A0 (on P0/P1)	t_{12} CC	–		22	ns	
Output valid delay for: A15 … A0 (on P2/P10)	t_{13} CC	–		22	ns	
Output valid delay for: CS	t_{14} CC	–		20	ns	
Output valid delay for: D15 … D0 (write data, MUX-mode)	t_{15} CC	–		21	ns	
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	t_{16} CC	–		21	ns	
Output hold time for: RD, WR(L/H)	t_{20} CC	0		10	ns	
Output hold time for: BHE, ALE	t_{21} CC	0		10	ns	
Output hold time for: A23 … A16, A15 … A0 (on P2/P10)	t_{23} CC	0		10	ns	
Output hold time for: CS	t_{24} CC	0		10	ns	
Output hold time for: D15 … D0 (write data)	t_{25} CC	0		10	ns	
Input setup time for: READY, D15 … D0 (read data)	t_{30} SR	29		–	ns	
Input hold time for: READY, D15 … D0 (read data)[1)]	t_{31} SR	-6		–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

4.6.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 31 SSC Master/Slave Mode Timing for Upper Voltage Range (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	–	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0.5 × t_{BIT}	–	3)	ns	
Transmit data output valid time	t_3 CC	-6	–	13	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-7	–	–	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	7	–	–	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	5	–	–	ns	4)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	7	–	–	ns	4)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	5	–	–	ns	4)
Data output DOUT valid time	t_{14} CC	8	–	29	ns	4)

1) The maximum value further depends on the settings for the slave select output leading delay.

2) $t_{SYS} = 1/f_{SYS}$ (= 12.5 ns @ 80 MHz)

3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.

4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

4.6.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 33 JTAG Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	60	50	–	ns	–
TCK high time	t_2 SR	16	–	–	ns	–
TCK low time	t_3 SR	16	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	8	ns	–
TCK clock fall time	t_5 SR	–	–	8	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge[1]	t_8 CC	–	–	30	ns	C_L = 50 pF
	t_8 CC	10	–	–	ns	C_L = 20 pF
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	30	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1)]	t_{10} CC	–	–	30	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

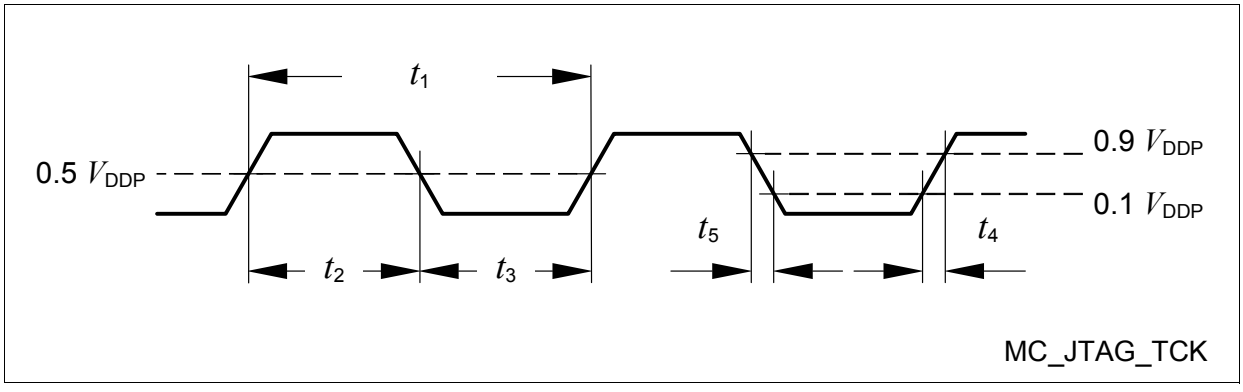

Figure 26 Test Clock Timing (TCK)

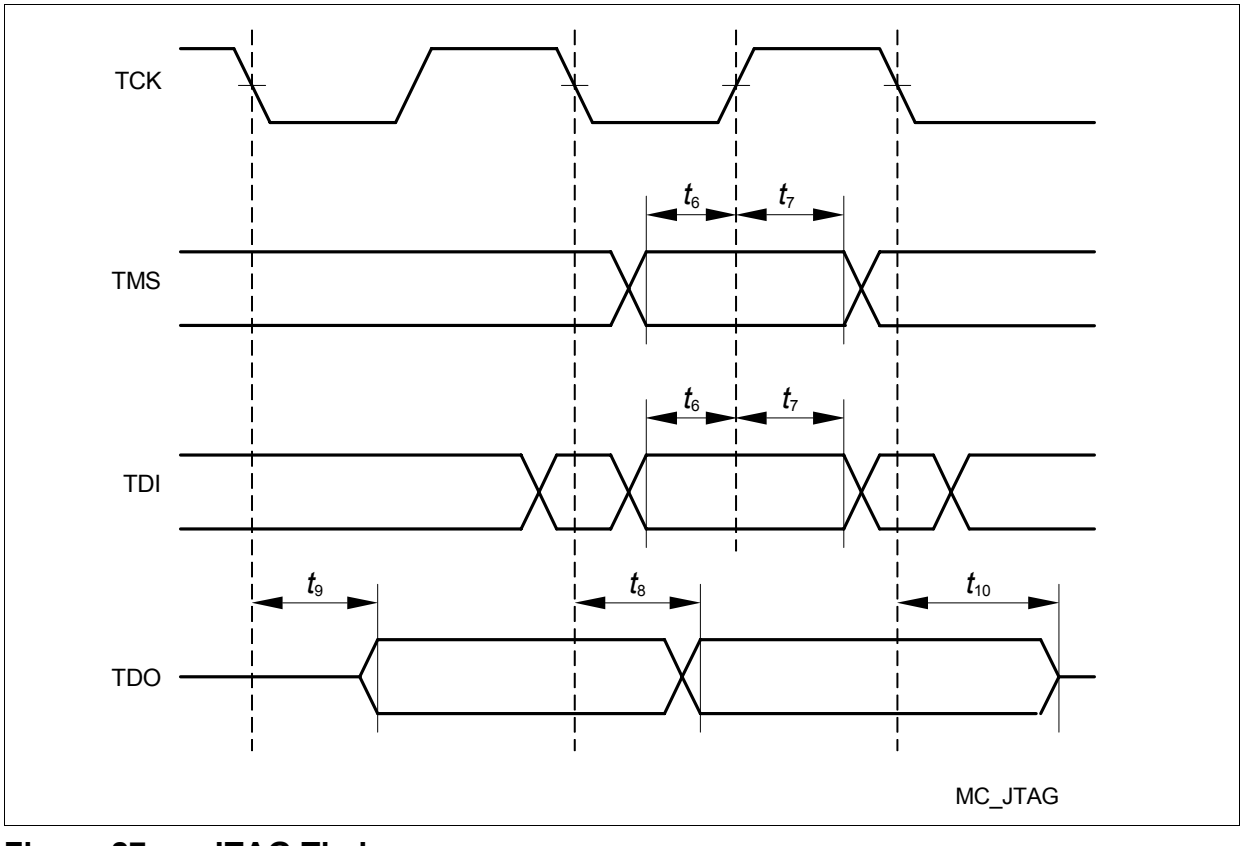

Figure 27 JTAG Timing