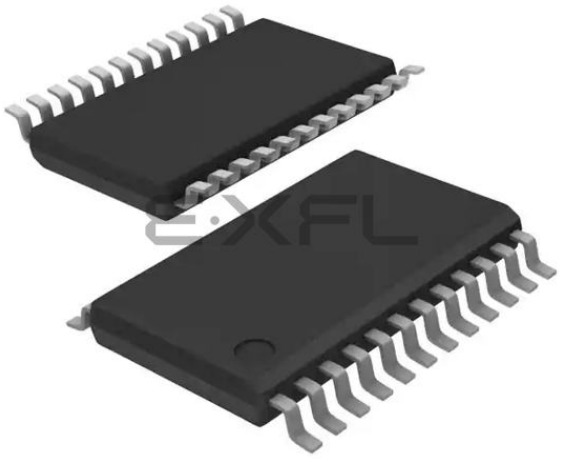

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	15MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	24-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc804m101jdh24j

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_16/ACMP_I4/ ADC_3	2	2	1	32	E2	[3]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
									ACMP_I4 — Analog comparator common input 4.
									ADC_3 — ADC input 3.
PIO0_17/ADC_9	3	-	2	1	E1	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
								A	**ADC_9 —** ADC input 9.
PIO0_18	1	1	-	31	-	[3]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
PIO0_19/DACOUT	24	24	-	26	-	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
								A	**DACOUT —** DAC output.
PIO0_20	13	13	-	15	-	[3]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
PIO0_21/ACMP_I5	12	12	-	10	-	[3]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
									ACMP_15 — Analog comparator common input 5.
PIO0_22	-	-	-	30	-	[3]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
PIO0_23	-	-	-	29	-	[3]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
PIO0_24	-	-	-	28	-	[3]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24.
PIO0_25	-	-	-	27	-	[3]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25.
PIO0_26	-	-	-	14	-	[3]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	-	-	-	13	-	[3]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28	-	-	-	12	-	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28.
PIO0_29	-	-	-	11	-	[3]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
PIO0_30	-	-	-	21	-	[3]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
VREFP	21	21	18	23	E4			A	**VREFP —** ADC positive reference voltage. Must be equal or lower than V_{DD}.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
V_{DD}	18	18	15	20	B4		-	-	If VDDIO is present, VDD is the supply voltage for the I/Os on the right side of the package and the core voltage regulator. If VDDIO is not present, VDD also supplies voltage to the I/Os on the left side of the package.
VDD_{IO}	-	3	-	-	-		-	-	If present, it is the supply voltage for the I/Os on the left side of the package.
V_{SS}	19		16	33[8]	C4		-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 15.5 “Pin states in different power modes”. For termination on unused pins, see Section 15.4 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[5] See Figure 16 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is not available in deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from deep power-down mode.

[6] The WKTCLKIN function is enabled in the PINENABLE0 register in the PMU. See the LPC804 user manual.

[7] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[8] Thermal pad for HVQFN33.

9.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

9.6.1 Features

- Nested Vectored Interrupt Controller is a part of the Arm Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC804, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the Arm exceptions SVCall and PendSV.
- Supports NMI.

9.6.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

9.7 System tick timer

The Arm Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

9.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 12 “LPC804 clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.
- The LPC804 uses a dual voltage I/O feature. The pins on one side of the package are supplied by VDDIO and the pins on the other side are supplied by VDD. Each of these two supplies can be connected to different voltages within the allowed Vdd range. This feature allows the device to level-shift signals from one off-chip voltage domain to another.

- The switch matrix provides level shifter functionality to allow up to two selected signals to be routed from user-selected pins in one voltage domain to selected pins in the alternate domain. This feature can also be used on a single supply device if voltage level shifting is not required.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 9.9 for details.

9.8.1 Standard I/O pad configuration

Figure 10 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

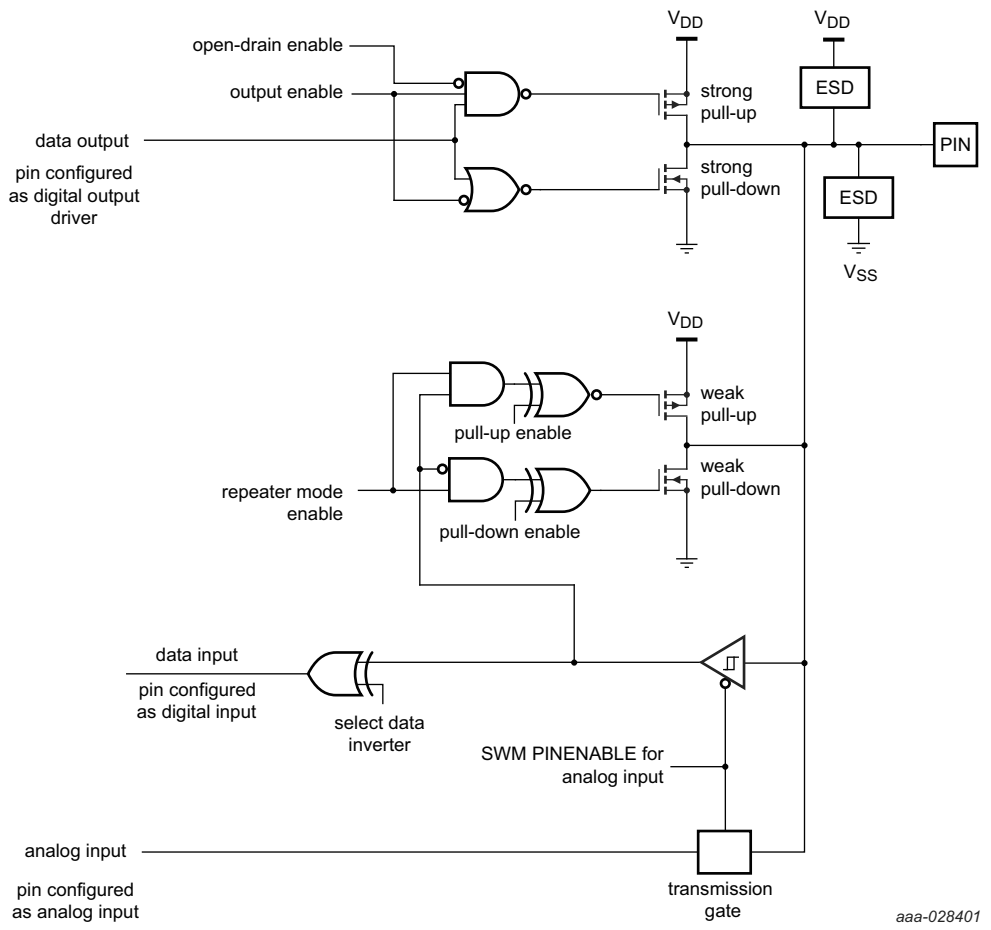


Fig 10. Standard I/O pad configuration

9.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, CTimer, Capacitive Touch, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Section 7.2 “Pin description”. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

9.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC804 use accelerated GPIO functions:

- GPIO registers are on the Arm Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 7 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

9.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 10).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

9.11 Pin interrupt

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt. The registers that control the pin interrupt are on the IO+ bus for fast single-cycle access.

9.13.1 Features

- Maximum data rates of up to 15 Mbit/s in master mode and up to 20 Mbit/s in slave mode for SPI functions connected to all digital pins.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

9.14 I^2C-bus interface (I^2C0 and I^2C1)

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master.

9.14.1 Features

- I^2C0 and I^2C1 support standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

9.15 Capacitive Touch Interface

The Capacitive Touch interface is designed to handle up to five capacitive buttons in different sensor configurations, such as slider, and button matrix. It operates in sleep, deep sleep, and power-down modes, allowing very low power performance.

The Capacitive Touch module measures the change in capacitance of an electrode plate when an earth-ground connected object (for example, finger) is brought within close proximity.

9.16 CTimer

9.16.1 General-purpose 32-bit timers/external event counter

The LPC804 has one general-purpose 32-bit timer/counter.

9.18 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

9.18.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

9.19 Self-Wake-up Timer (WKT)

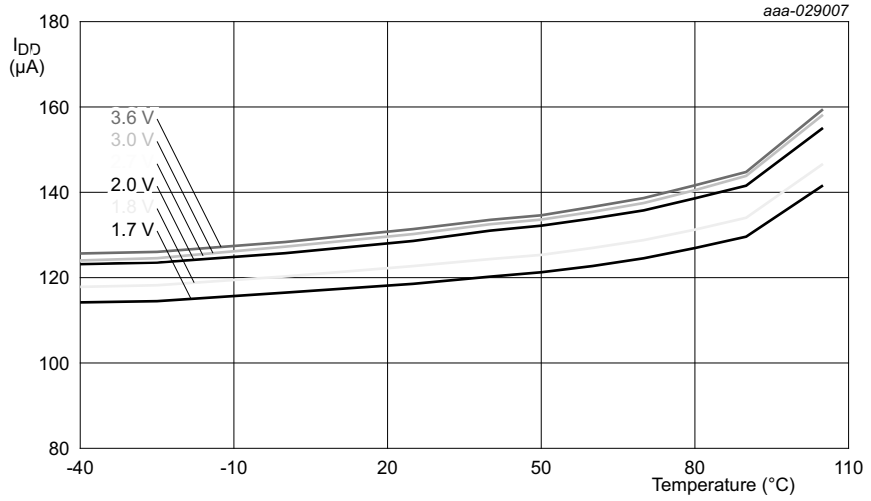
The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

9.19.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the FRO. The low-power oscillator can be used as the clock source in sleep, deep-sleep, and power-down modes.
- The WKT can be used for waking up the part from any reduced power mode or for general-purpose timing.

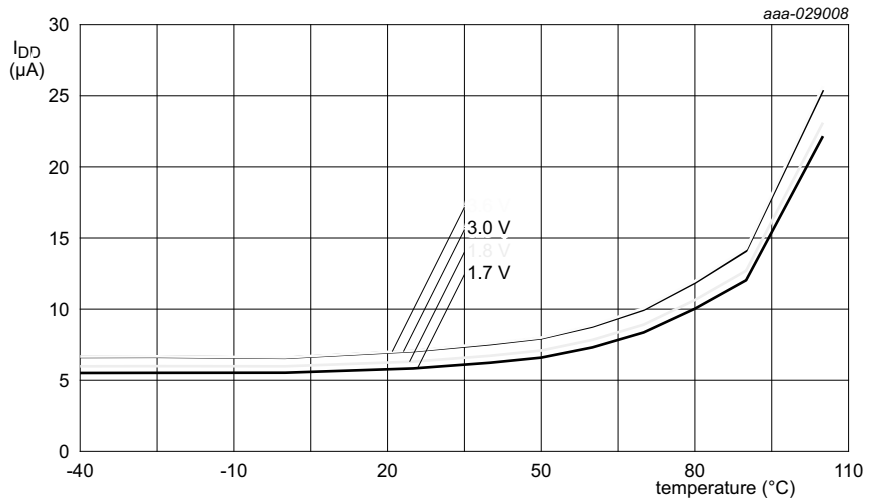
9.20 Programmable Logic Unit (PLU)

The PLU is comprised of 26 5-input LUT elements. Each LUT element contains a 32-bit truth table (look-up table) register and a 32:1 multiplexer. During operation, the five LUT inputs control the select lines of the multiplexer. This structure allows any desired logical combination of the five LUT inputs.



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register.

Fig 17. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register.

Fig 18. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

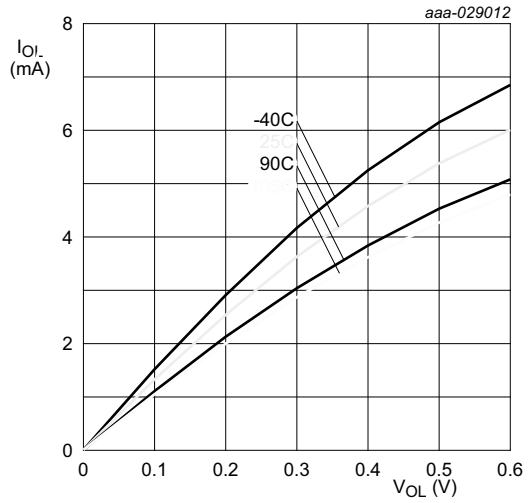
12.2.1 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG. and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C.

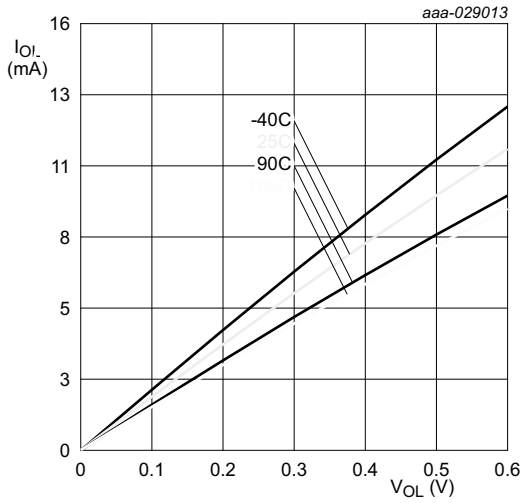
The supply currents are shown for system clock frequencies of 12 MHz and 15 MHz.

Table 13. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	15 MHz	
FRO	74	-	-	FRO = 12MHz. FRO output disabled.
BOD	39	-	-	Independent of main clock frequency.
Flash	80	-	-	-
LPOsc	1	-	-	FRO; independent of main clock frequency.
GPIO + pin interrupt	-	40	54	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	24	30	-
IOCON	-	28	36	-
CTimer	-	28	37	-
MRT	-	45	56	-
WWDT	-	31	41	-
I2C0	-	44	58	-
I2C1	-			
SPI0	-	33	42	-
USART0	-	39	46	-
USART1	-	40	50	-
Comparator ACMP	-	36	46	-
ADC	-	61	78	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	61	78	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	61	78	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
DAC	-	29	35	
Capacitive Touch	-	22	26	
PLU	-	118	149	
CRC	-	37	50	-

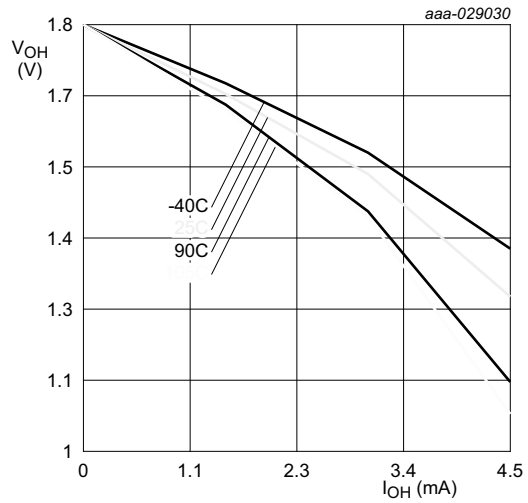


Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.

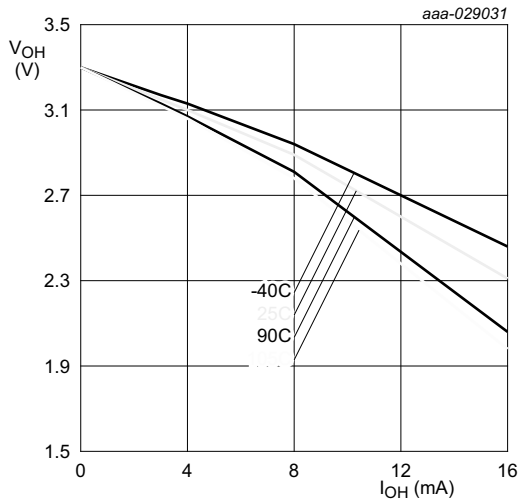


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

Fig 22. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

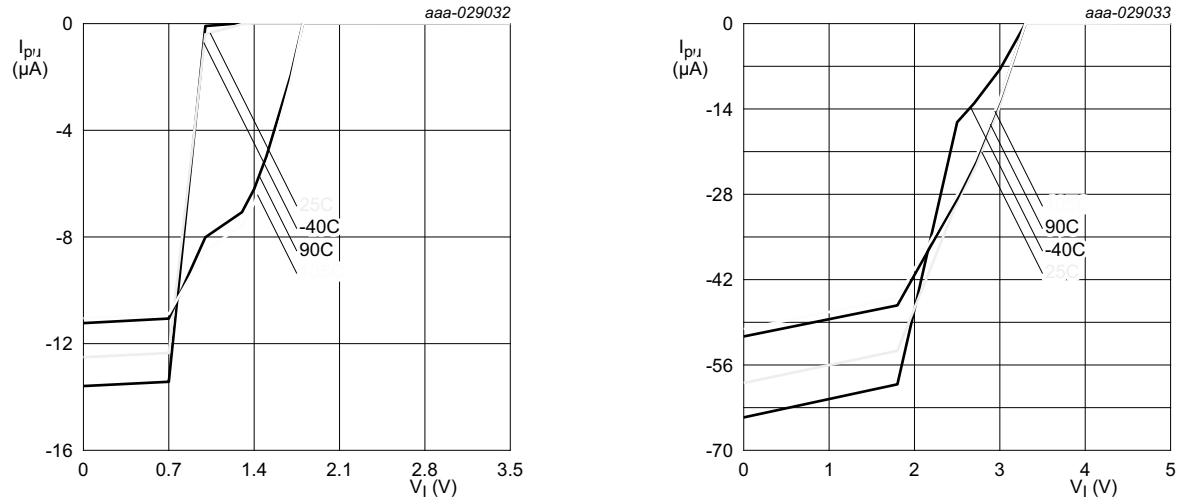


Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

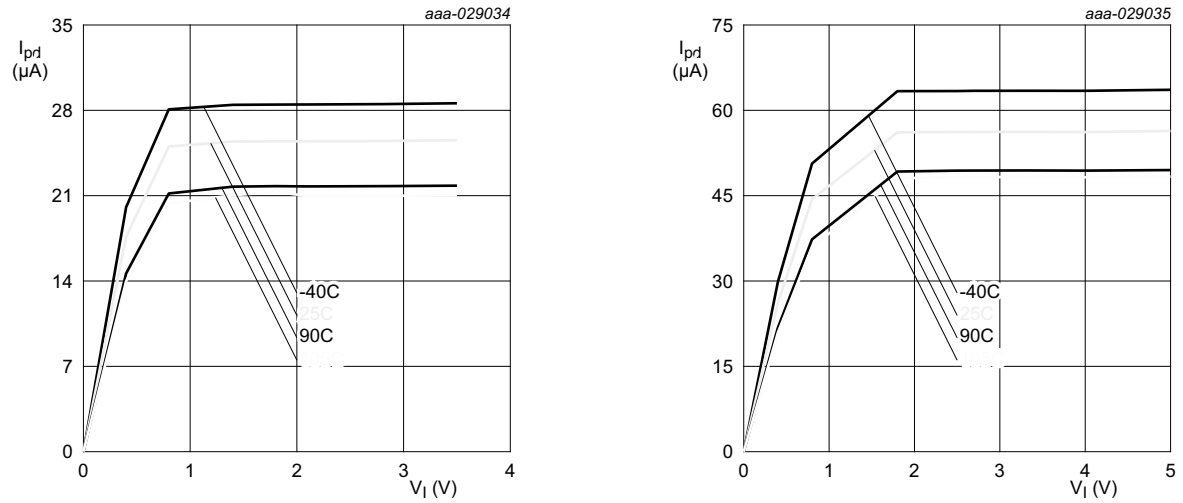
Fig 23. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

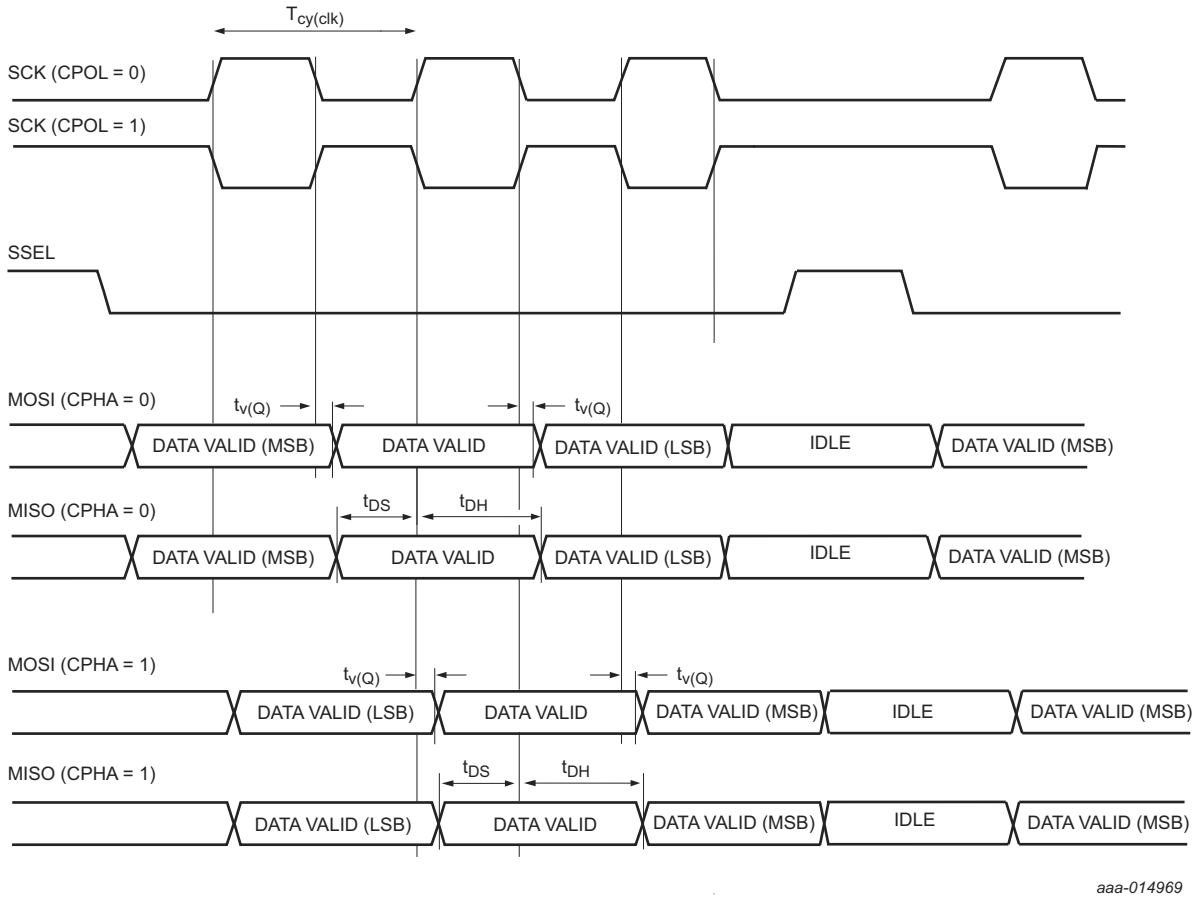
Fig 24. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 25. Typical pull-down current I_{PD} versus input voltage V_I



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the LPC804 *User manual*.

Fig 27. SPI master timing

13.8 Wake-up process

Table 23. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; Using FRO (15 MHz) as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	1.97	-	µs
		from deep-sleep mode	[2]	-	2.07	-	µs
		from power-down mode	[2]	-	25	-	µs
		from deep power-down mode	[4]	-	313	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler. ISR is located in SRAM.

[3] FRO enabled, all peripherals off.

[4] Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the Wake-Up pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

14. Characteristics of analog peripherals

14.1 BOD

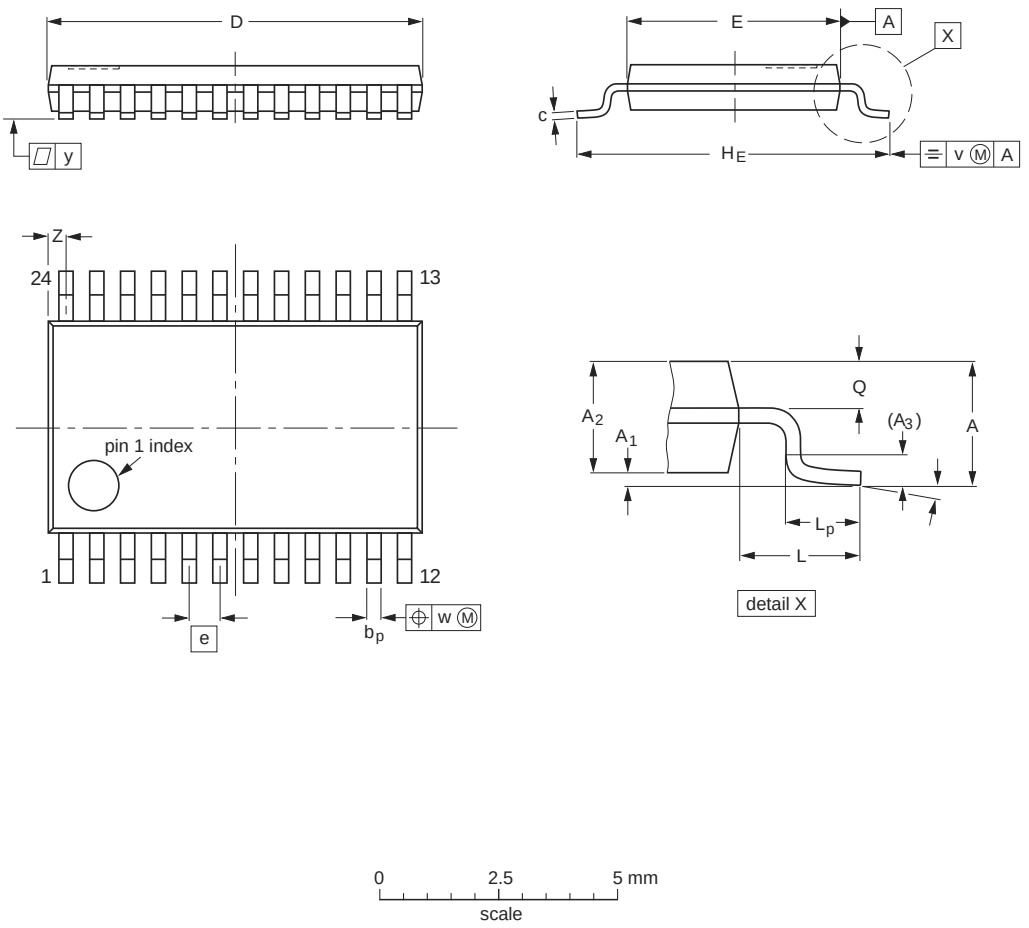
Table 24. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.24	-	V
		de-assertion		-	2.40	-	V
		interrupt level 2					
		assertion		-	2.52	-	V
		de-assertion		-	2.64	-	V
		interrupt level 3					
		assertion		-	2.81	-	V
		de-assertion		-	2.90	-	V
		reset level 0					
		assertion		-	1.51	-	V
		de-assertion		-	1.54	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC804 *user manual*.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

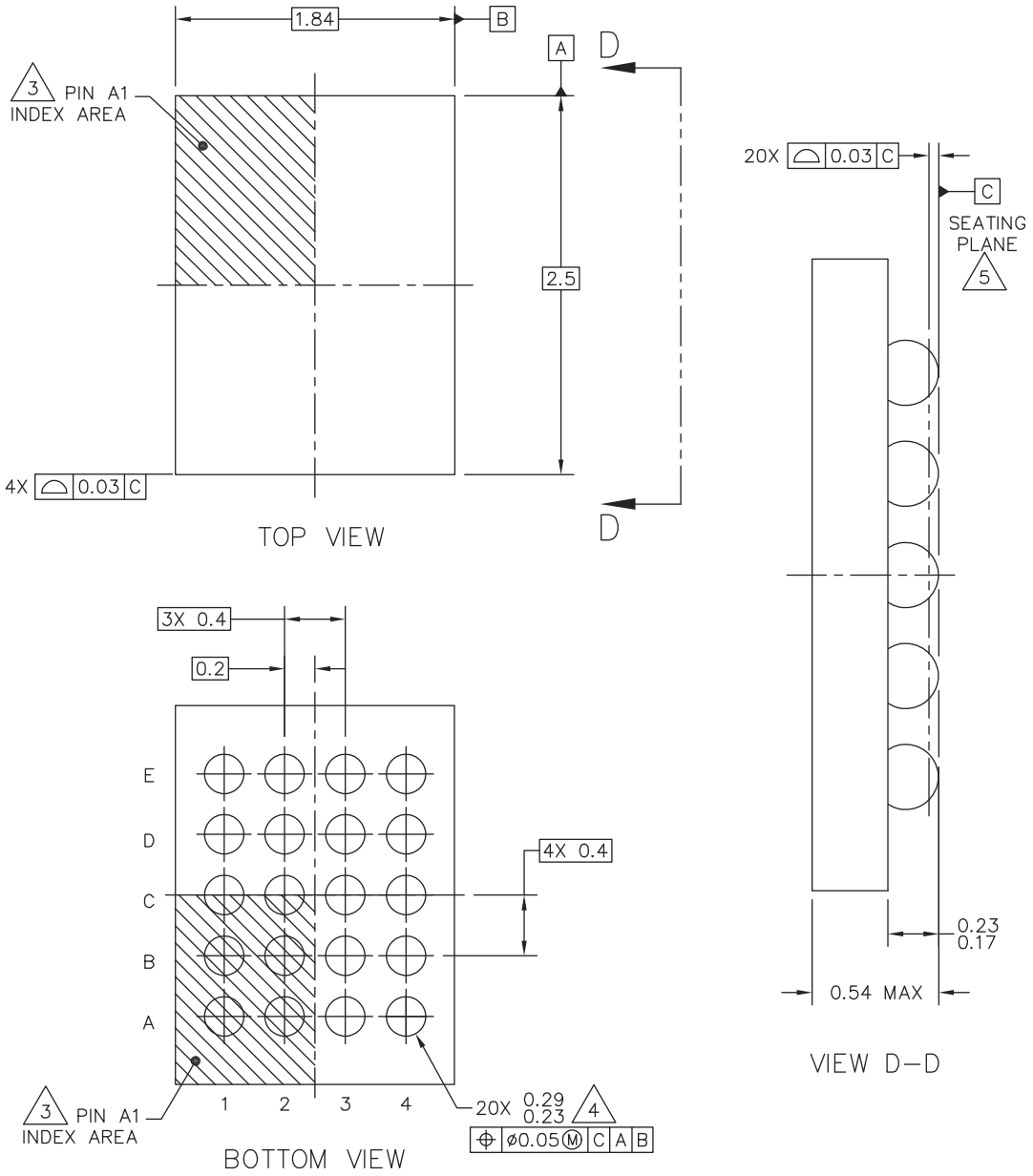
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 36. Package outline SOT355-1 (TSSOP24)



DATE: 24 MAY 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01253D	REVISION: 0	

Fig 38. Package outline WLCSP20 (2.50 ×1.84 × 0.5 mm)

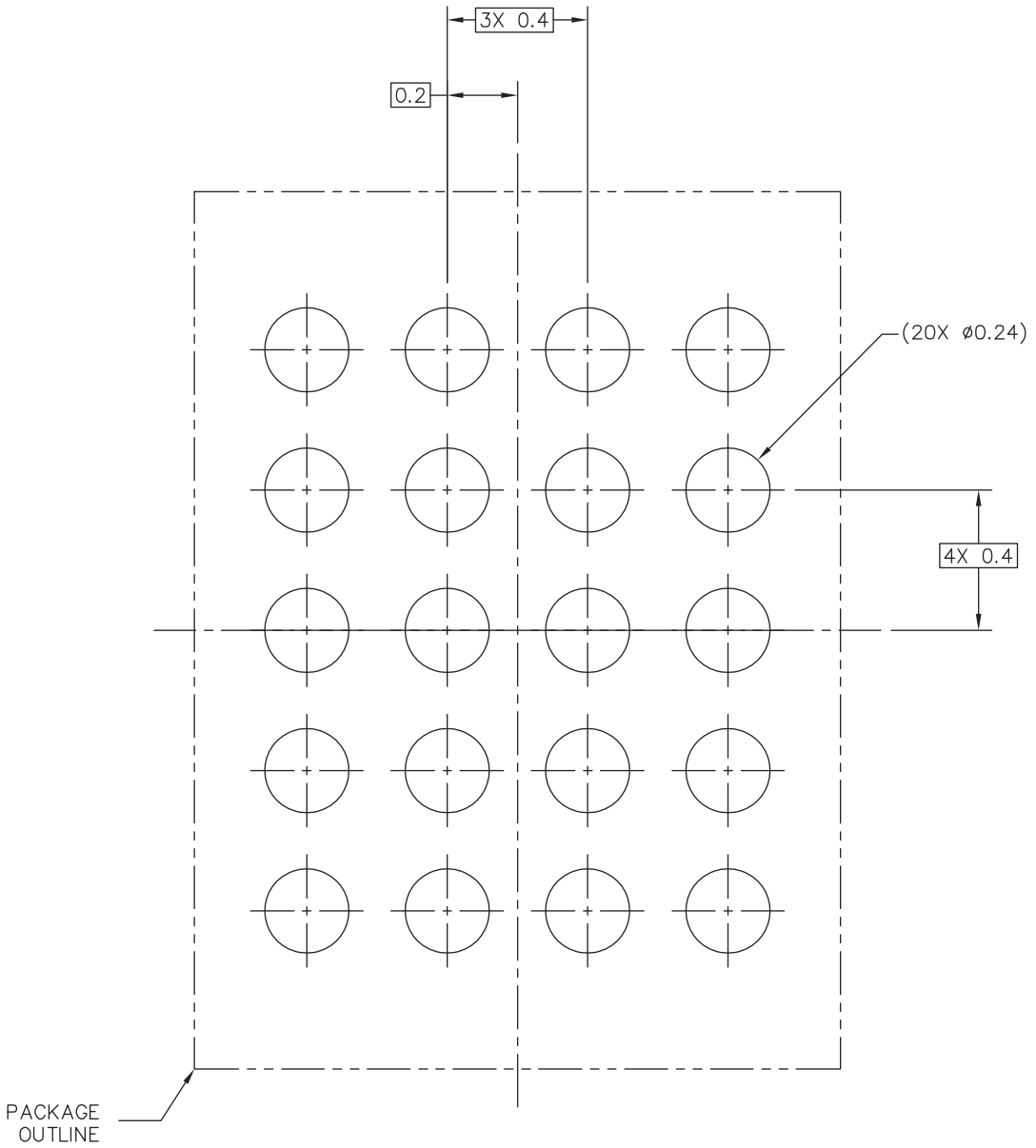


Fig 43. Reflow soldering for the WLCSP20 package (2 of 3)

18. Abbreviations

Table 34. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

19. References

[1] LPC804 User manual UM11065:

[2] LPC804 Errata sheet:

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

20. Revision history

Table 35. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC804 v.1.4	20180712	Product data sheet	201804020F01	LPC804 v.1.3
	• Added LPC804UK device. • Updated Section 5 “Marking”. • Updated Table 25 “12-bit ADC static characteristics”: Changed typical offset error ($E_{O)}$ to ±3 LSB. Added table note text: For device revision 1B, typical offset value is ±3 LSB. For device revision 1A, the typical offset value is ±8 LSB. • Updated Section 9.25.1 “Internal oscillators”. Changed heading title. • Updated Section 15.2 “Connecting power, clocks, and debug functions”: removed text: connect the external crystal.			
LPC804 v.1.3	20180323	Product data sheet	-	LPC804 v.1.2
Modifications:	• Fixed revision number. • Updated Table 15 “Flash characteristics”. t_{er} consolidated to t_{prog}/t_{er}. • Updated Section 9.25.4.4 “Deep power-down mode” with text: Five general-purpose registers are available to store information during deep power-down mode.			
LPC804 v.1.2	20180227	Product data sheet	-	LPC804 v.1.1
Modifications:	• Updated Table 12 “Static characteristics, supply pins”: Added condition: system clock = 1 MHz, V_{DD} = 3.3 V. • Updated Table 16 “Dynamic characteristic: FRO”: Max values: FRO clock frequency; Condition: −20 °C ≤ T_{amb} ≤ 70 °C and FRO clock frequency; Condition: −40 °C ≤ T_{amb} ≤ 105 °C. • Updated title of Section 13.1 “Flash memory (EEPROM based)”.			
LPC804 v.1.1	20180214	Product data sheet	-	LPC804 v.1
Modifications:	• Updated Section 2 “Features and benefits”. • Updated Table 5 “Movable functions (assign to pins PIO0_0 to PIO0_5, PIO0_7 to PIO0_30 through switch matrix)”. • Added level shifter functionality to Section 9.8 “I/O configuration”. • Updated Table 16 “Dynamic characteristic: FRO”: Changed frequencies to 9 MHz, 12 MHz, and 15 MHz. Added Condition: −20 °C ≤ T_{amb} ≤ 70 °C and Condition: −40 °C ≤ T_{amb} ≤ 70 °C.			
LPC804 v.1	20180126	Product data sheet	-	-

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