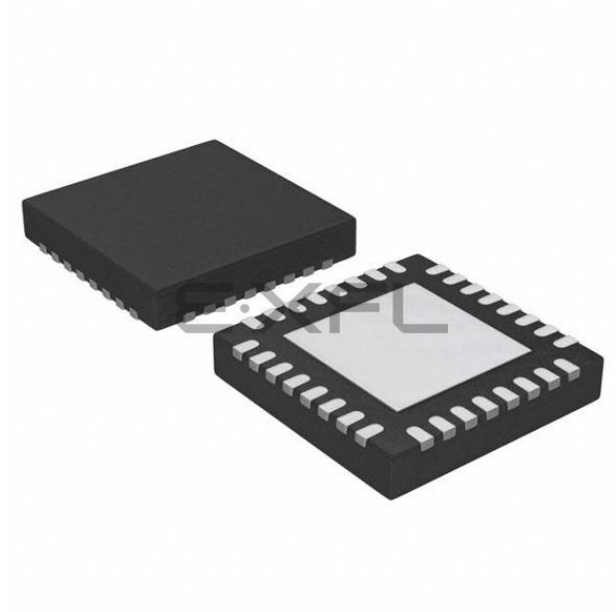

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	15MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc804m101jhi33y

- Wake-up from deep-sleep and power-down modes on activity on USART, SPI, and I^2C peripherals.
- Wake-up from deep power-down mode on multiple pins.
- Timer-controlled self wake-up from sleep, deep-sleep, and power-down modes.
- Power-On Reset (POR).
- Brownout detect (BOD).

- Unique device serial number for identification.
- Single power supply (1.71 V to 3.6 V).
- Operating temperature range -40 °C to +105 °C.
- Available in WLCSP20, TSSOP20, TSSOP24, and HVQFN33 packages.

5. Marking

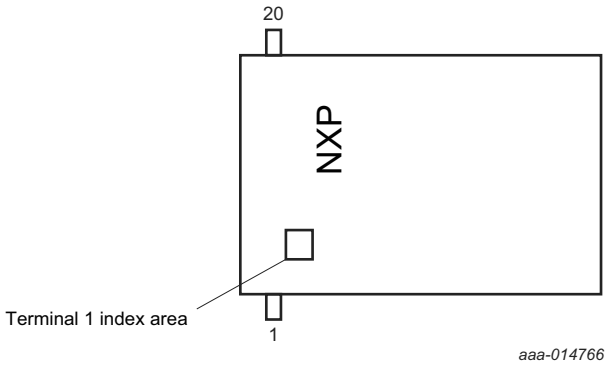


Fig 1. TSSOP20 and TSSOP24 package markings

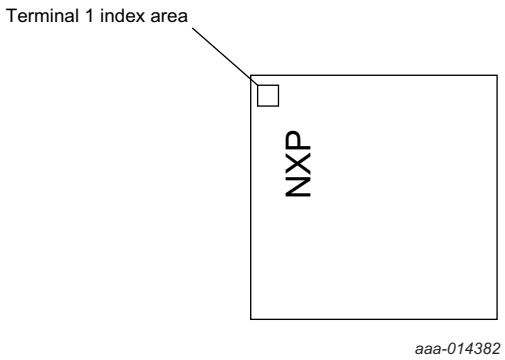


Fig 2. HVQFN33 package marking

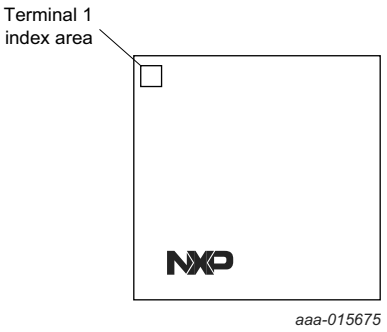


Fig 3. WLCSP20 package marking

The LPC804 HVQFN33 packages have the following top-side marking::

- First line: LPC804M1
- Second line: xxxx
- Third line: yywwx[R]
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

The LPC804 TSSOP20 packages typically have the following top-side marking:

- First line: LPC804
- Second line: M101
- Third line: xxxx
- Fourth line: xxywwx[R]
  - yww: Date code with y = year and ww = week.
  - xR = Boot code version and device revision.

The LPC804 TSSOP24 packages have the following top-side marking:

- The switch matrix provides level shifter functionality to allow up to two selected signals to be routed from user-selected pins in one voltage domain to selected pins in the alternate domain. This feature can also be used on a single supply device if voltage level shifting is not required.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 9.9 for details.

9.8.1 Standard I/O pad configuration

Figure 10 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

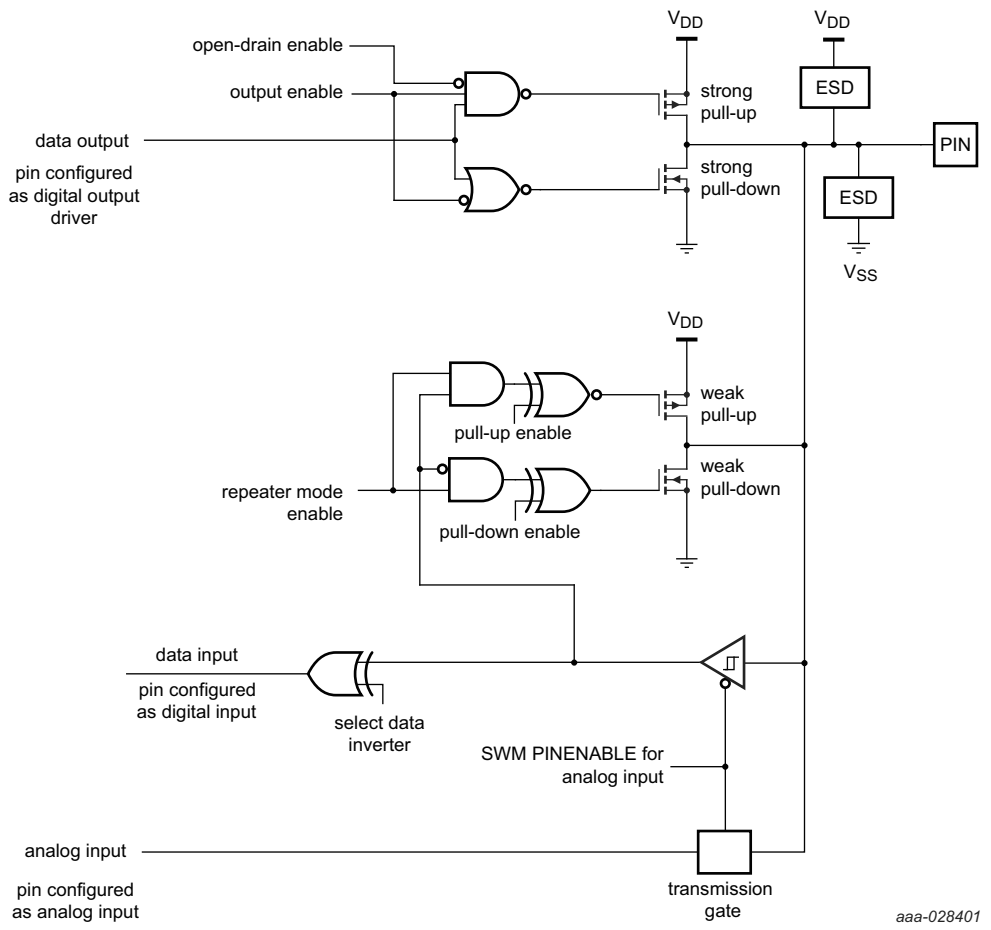


Fig 10. Standard I/O pad configuration

9.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, CTimer, Capacitive Touch, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Section 7.2 “Pin description”. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

9.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC804 use accelerated GPIO functions:

- GPIO registers are on the Arm Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 7 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

9.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 10).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

9.11 Pin interrupt

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt. The registers that control the pin interrupt are on the IO+ bus for fast single-cycle access.

9.20.1 Features

- The PLU is used to create small combinatorial and/or sequential logic networks including simple state machines.
- The PLU is comprised of an array of 26 inter-connectable, 5-input Look-up Table (LUT) elements, and four flip-flops.
- Eight primary outputs can be selected using a multiplexer from among all of the LUT outputs and the four flip-flops.
- An external clock to drive the four flip-flops must be applied to the PLU_CLKIN pin if a sequential network is implemented.
- Programmable logic can be used to drive on-chip inputs/triggers through external pin-to-pin connections.
- A tool suite is provided to facilitate programming of the PLU to implement the logic network described in a Verilog RTL design.

Remark: PLU cannot be used to wake-up from sleep, deep-sleep, power-down, and deep power-down modes.

9.21 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 27.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled through the switch matrix.

9.24 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

9.24.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1’s complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

9.25.4 Power control

The LPC804 supports the Arm Cortex-M0+ sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

9.25.4.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped. Resumption from the sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

9.25.4.2 Deep-sleep mode

In deep-sleep mode, the LPC804 core is in sleep mode and all peripheral clocks and all clock sources are off except for the FRO or low-power oscillator if selected. The FRO output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In deep-sleep mode, the application can keep the low power oscillator and the BOD circuit running for self-timed wakeup and BOD protection.

The LPC804 can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI (in slave mode), or the I2C blocks (in slave mode).

Any interrupt used for waking up from deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

9.25.4.3 Power-down mode

In power-down mode, the LPC804 is in sleep mode and all peripheral clocks and all clock sources are off except for low-power oscillator if selected. In addition, all analog blocks and the flash are shut down. In power-down mode, the application can keep the low-power oscillator and the BOD circuit running for self-timed wake up and BOD protection.

The LPC804 can wake up from power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI (in slave mode), or the I2C blocks (in slave mode).

Any interrupt used for waking up from power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

9.27 Emulation and debugging

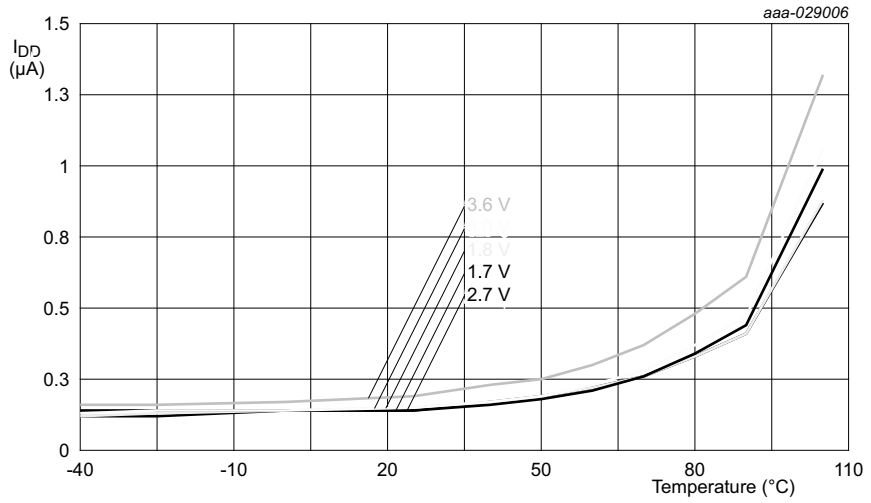
Debug functions are integrated into the Arm Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The Arm Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the Arm SWD debug ($\overline{\text{RESET}}$ = HIGH). The Arm SWD debug port is disabled while the LPC804 is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode. See Table 4.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.



WKT not running.

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

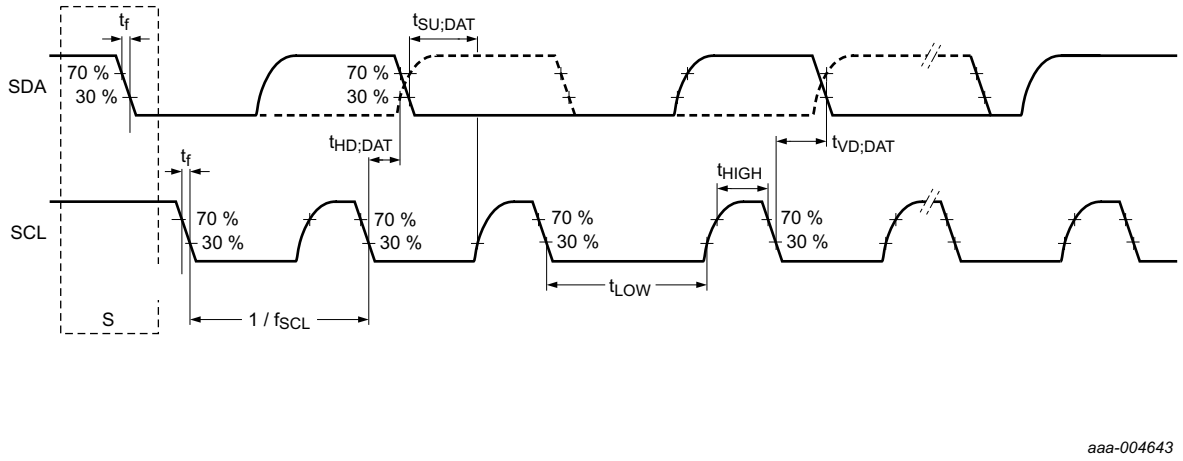


Fig 26. I²C-bus pins clock timing

13.8 Wake-up process

Table 23. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; Using FRO (15 MHz) as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	1.97	-	µs
		from deep-sleep mode	[2]	-	2.07	-	µs
		from power-down mode	[2]	-	25	-	µs
		from deep power-down mode	[4]	-	313	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler. ISR is located in SRAM.

[3] FRO enabled, all peripherals off.

[4] Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the Wake-Up pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

14.2.1 ADC input impedance

Figure 31 shows the ADC input impedance. In this figure:

- ADCx represents ADC input channel 0.
- ADCy represents ADC input channels 1 to 11.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If ADC input channel 0 is selected, the ADC input signal goes through $R_1 + R_{sw}$ to the sampling capacitor (C_{ia}).
- If ADC input channels 1 to 11 are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 5.6 kΩ, R_{sw} = 6.9 kΩ
- To calculate total resistance, use the following equation:
  - $R_{TOTAL} = R_{external} + R_{internal}$
  - $R_{external}$ = External resistance on the ADC input channel.
  - $R_{internal}$ for channel 0 = $R_1 + R_{SW}$ = 12.5 kΩ.
  - $R_{internal}$ for channels 1 to 11 = 6.9 kΩ.
- See Table 11 for C_{io}.
- See Table 25 for C_{ia}.

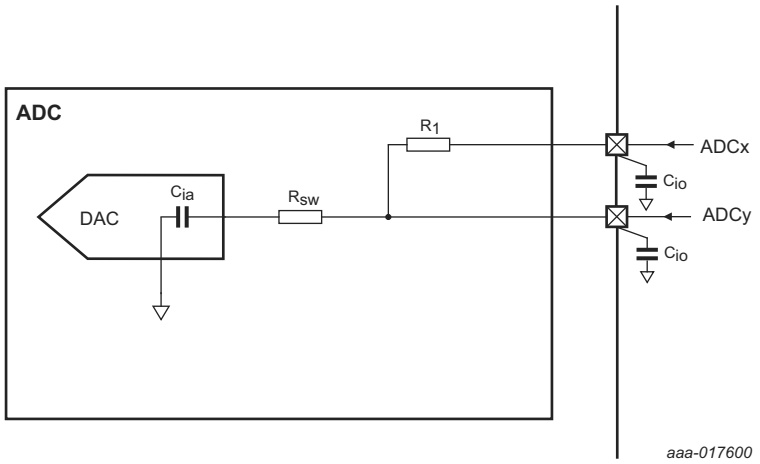


Fig 31. ADC input impedance

Table 29. Comparator voltage ladder reference static characteristics

V_{DD} = 1.8 V to 3.6 V. T_{amb} = -40 °C to + 105°C; external or internal reference.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$E_{V(O)}$	output voltage error	decimal code = 00	[2]	-	±6	-	mV
		decimal code = 08		-	±1	-	%
		decimal code = 16		-	±1	-	%
		decimal code = 24		-	±1	-	%
		decimal code = 30		-	±1	-	%
		decimal code = 31		-	±1	-	%

[1] Characterized though limited samples. Not tested in production.

[2] All peripherals except comparator, temperature sensor, and FRO turned off.

14.4 DAC

Table 30. 10-bit DAC electrical characteristics

V_{DD} = V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +105 °C unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
E_D	differential linearity error	[1][2]	-	0.4	-	LSB
$E_{L(adj)}$	integral non-linearity	[1][2]	-	6.0	-	LSB
E_O	offset error	[1][2]	-	±57.0	-	mV
E_G	gain error	[1][2]	-	±36.0	-	mV
C_L	load capacitance		-	200	-	pF
R_{OUT}	PIO0_19/DACOUT_0 pin resistance	[3]	-	90	200	Ω
V_{OUT}	Output voltage range		0.175	-	V_{DDA}-0.175	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C) and V_{DD} = V_{DDA} = 3.6 V.

[2] Characterized through bench measurements, not tested in production.

[3] DAC output voltage depends on the voltage divider ratio of the R_{OUT} and external load resistance.

15.3 I/O power consumption

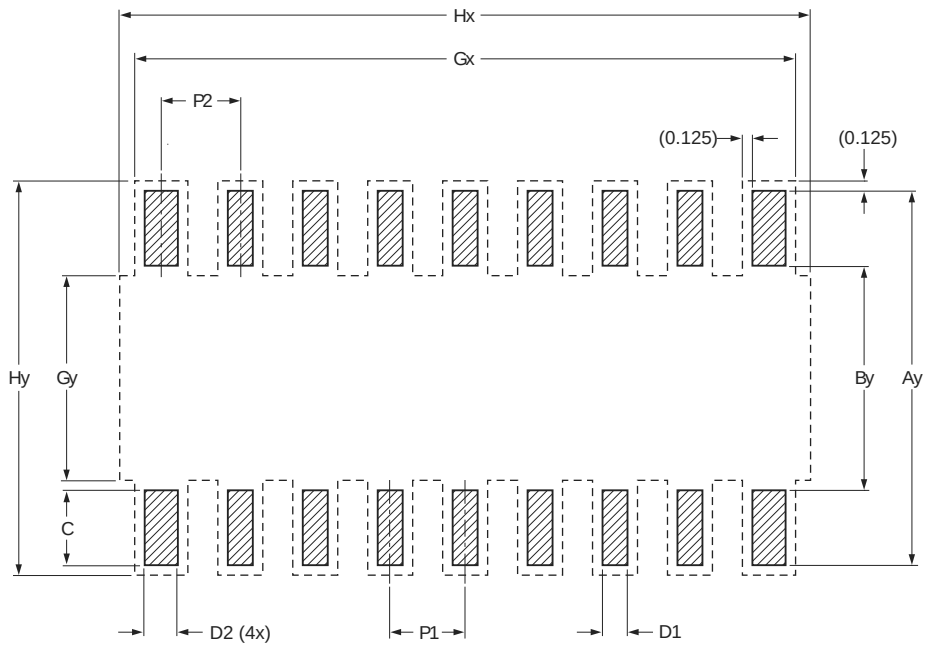
I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 14 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 14, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 14 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

Footprint information for re ow soldering of TSSOP24 package **SOT355-**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

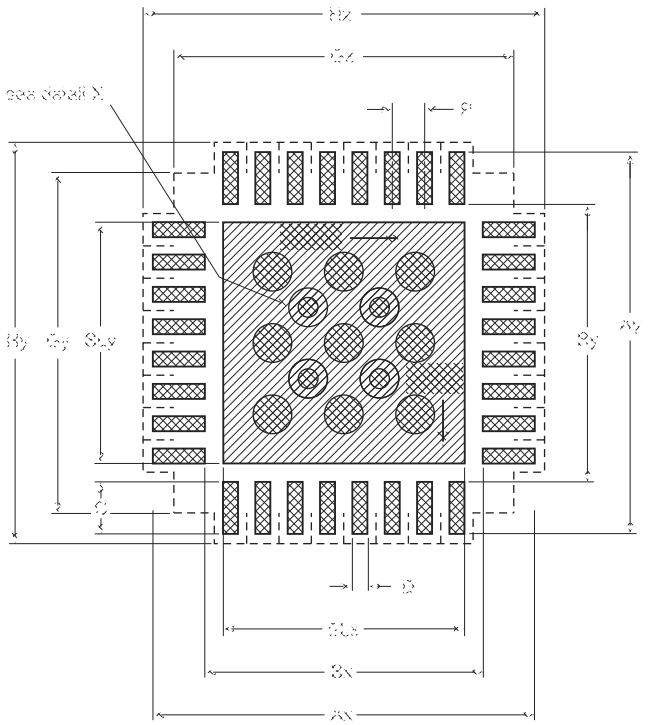
DIMENSIONS in mm

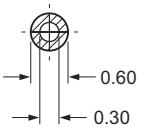
P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	8.200	5.300	8.600	7.450

sot355-1_fr

Fig 40. Reflow soldering of the TSSOP24 package

Footprint information for reflow soldering of HVQFN33 package





detail X

solder land

solder paste

occupied area

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

002aag766

Fig 41. Reflow soldering for the HVQFN33 (5x5) package

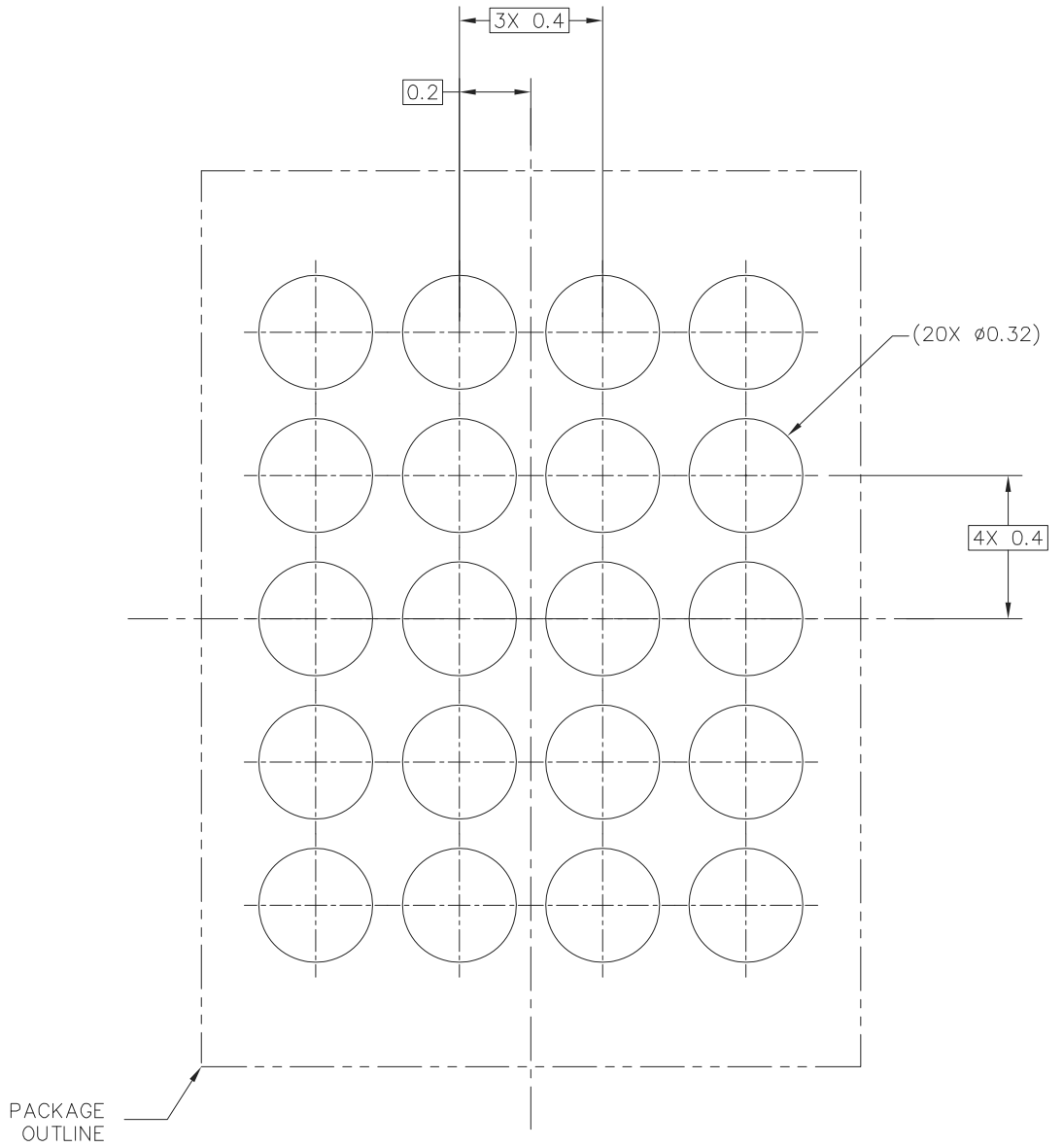


Fig 42. Reflow soldering for the WLCSP20 package (1 of 3)

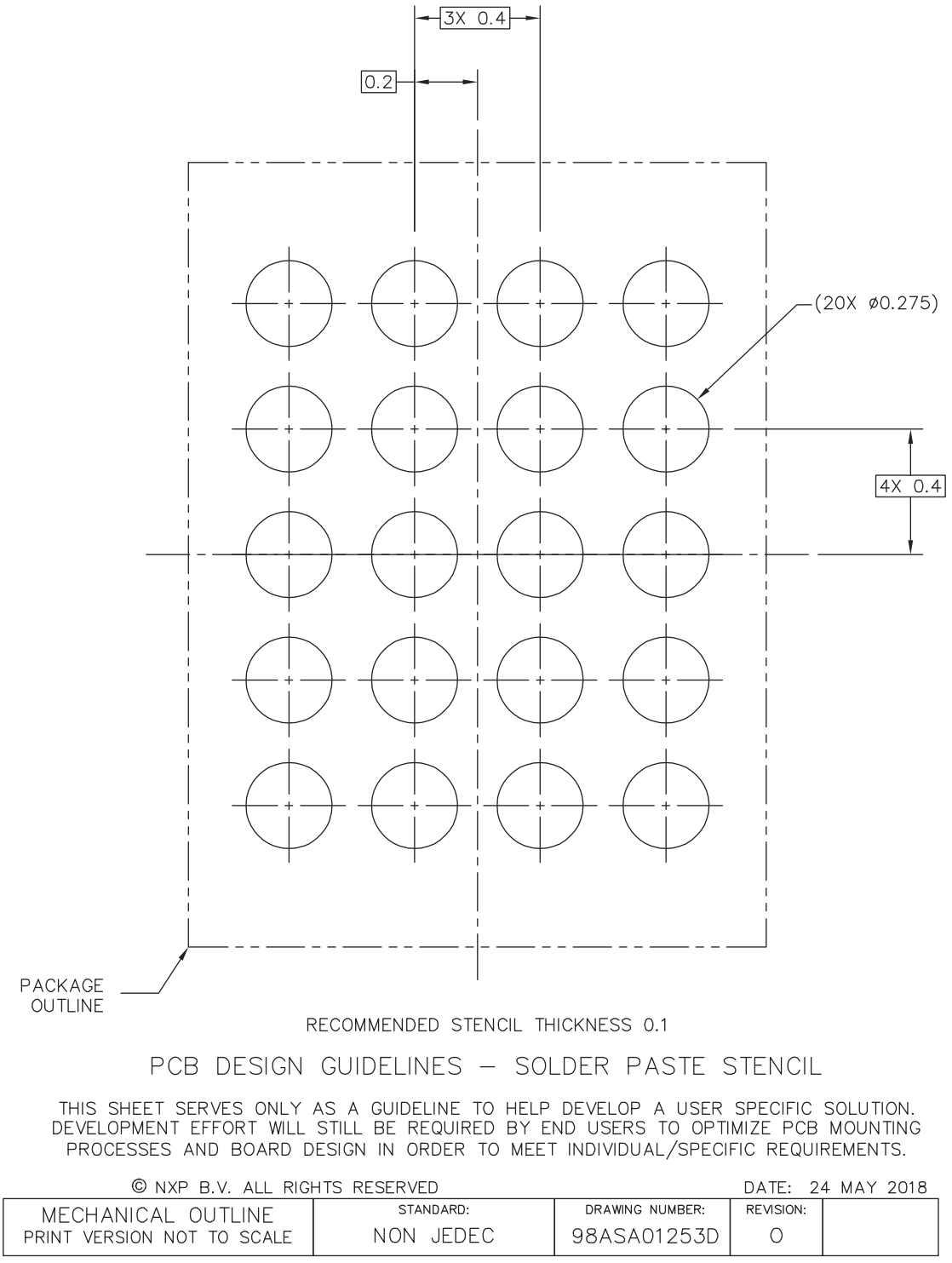


Fig 44. Reflow soldering for the WLCSP20 package (3 of 3)

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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