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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	15MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	24-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc804m111jdh24j

- First line: LPC804
- Second line: xxxx
- Third line: ywwx[R]
  - yww: Date code with y = year and ww = week.
  - xR = Boot code version and device revision.
- Fourth line: M1y1J
  - y: 0 or 1

The LPC804 WLCSP20 packages have the following top-side marking:

- First line: LPC804
- Second line: xxxxx
- Third line: xyywwx[R]
  - yyww: Date code with ww = week and yy = year.
  - xR = Boot code version and device revision.
- Fourth line: xxx - yyy

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 13.1
1B	Initial device revision with Boot ROM version 13.1

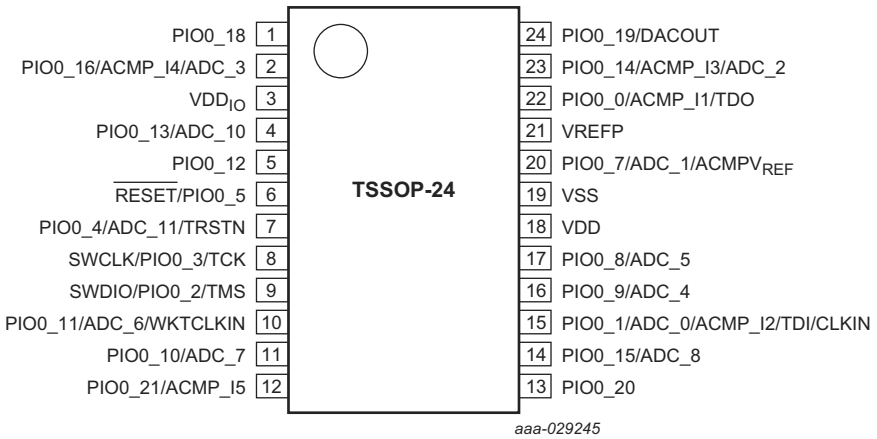
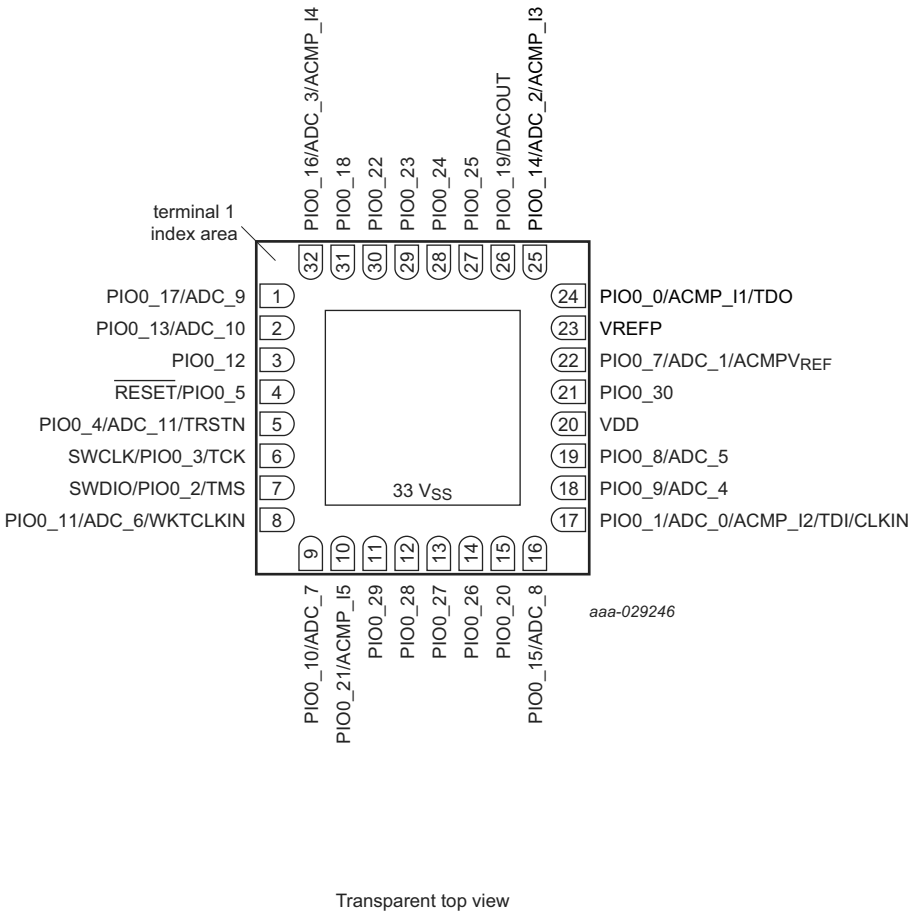


Fig 7. Pin configuration TSSOP24 - 2 package with VDDIO (LPC804M111JDH20 - dual supply device)



Transparent top view

Fig 8. Pin configuration HVQFN33 package

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_0/ACMP_I1/TDO	22	22	19	24	D3	[2]	I; PU	IO	**PIO0_0 —** General-purpose port 0 input/output 0. In ISP mode, this is the U0_RXD pin (for single supply devices). In boundary scan mode: TDO (Test Data Out).
								A	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ADC_0/ACMP_I2/ TDI/CLKIN	15	15	12	17	A4	[2]	I; PU	IO	**PIO0_1 —** General-purpose port 0 input/output 1. In boundary scan mode: TDI (Test Data In).
								A	**ACMP_I2 —** Analog comparator input 2.
								I	**CLKIN —** External clock input.
SWDIO/PIO0_2/ TMS	9	9	8	7	B2	[3]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
								I/O	**PIO0_2 —** General-purpose port 0 input/output 2.
SWCLK/PIO0_3/ TCK	8	8	7	6	B1	[3]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
								IO	**PIO0_3 —** General-purpose port 0 input/output 3.
PIO0_4/ADC_11/ TRSTN	7	7	6	5	C2	[2]	I; PU	IO	**PIO0_4 —** General-purpose port 0 input/output 4. In ISP mode, this pin is the U0_TXD pin (for single supply devices). In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset).
								A	**ADC_11 —** ADC input 11.
$\overline{\text{RESET}}$/PIO0_5	6	6	5	4	C1	[5]	I; PU	IO	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed.
								I	**PIO0_5 —** General-purpose port 0 input/output 5.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_7/ADC_1/ $ACMPV_{REF}$	20	20	17	22	D4	[2]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7.
								A	**ADC_1 —** ADC input 1.
									$ACMPV_{REF}$ — Alternate reference voltage for the analog comparator.
PIO0_8/ADC_5	17	17	14	19	C3	[2]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8. In ISP mode, this is the U0_RXD pin (for dual supply devices).
								A	**ADC_5 —** ADC input 5.
PIO0_9/ADC_4	16	16	13	18	B3	[2]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9. In ISP mode, this is the U0_TXD pin (for dual supply devices).
								A	**ADC_4 —** ADC input 4.
PIO0_10/ADC_7	11	11	10	9	A2	[2]	Inactive	I; F	**PIO0_10 —** General-purpose port 0 input/output 10.
									ADC_7 — ADC input 7.
PIO0_11/ADC_6/ WKTCLKIN	10	10	9	8	A1	[2]	Inactive	I; F	**PIO0_11 —** General-purpose port 0 input/output 11.
									ADC_6 — ADC input 6.
									WKTCKLKIN — This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in sleep, deep-sleep, and power-down modes.
PIO0_12	5	5	4	3	D1	[3]	I; PU	IO	**PIO0_12 —** General-purpose port 0 input/output 12. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler.
PIO0_13/ADC_10	4	4	3	2	D2	[2]	I; PU	IO	**PIO0_13 —** General-purpose port 0 input/output 13.
								A	**ADC_10 —** ADC input 10.
PIO0_14/ACMP_3/ ADC_2	23	23	20	25	E3	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
								A	**ACMP_I3 —** Analog comparator common input 3.
								A	**ADC_2 —** ADC input 2.
PIO0_15/ADC_8	14	14	11	16	A3	[4]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
									ADC_8 — ADC input 8.

8. Movable functions

Movable functions for the I2C, USART, SPI, CTimer pins, Capacitive Touch, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the fixed functions of the pin.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_5, PIO0_7 to PIO0_30 through switch matrix)

Function name	Type	Description
Ux_TXD	O	Transmitter output for USART0 to USART1.
Ux_RXD	I	Receiver input for USART0 to USART1.
$\overline{\text{Ux\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{Ux\_CTS}}$	I	Clear To Send input for USART0.
Ux_SCLK	I/O	Serial clock input/output for USART0 to USART1 in synchronous mode.
SPIx_SCK	I/O	Serial clock for SPI0.
SPIx_MOSI	I/O	Master Out Slave In for SPI0.
SPIx_MISO	I/O	Master In Slave Out for SPI0.
SPIx_SSEL0	I/O	Slave select 0 for SPI0.
SPIx_SSEL1	I/O	Slave select 1 for SPI0.
I2Cx_SDA	I/O	I^2C0 and I^2C1 bus data input/output.
I2Cx_SCL	I/O	I^2C0 and I^2C1 bus clock input/output.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.
T0_MAT0	O	Timer Match channel 0.
T0_MAT1	O	Timer Match channel 1.
T0_MAT2	O	Timer Match channel 2.
T0_MAT3	O	Timer Match channel 3.
T0_CAP0	I	Timer Capture channel 0.
T0_CAP1	I	Timer Capture channel 1.
T0_CAP2	I	Timer Capture channel 2.
CAPT_X0	O	CAPT_X0 function.
CAPT_X1	O	CAPT_X1 function.
CAPT_X2	O	CAPT_X2 function.
CAPT_X3	O	CAPT_X3 function.
CAPT_X4	O	CAPT_X4 function.
CAPT_YL	O	CAPT_YL function.
CAPT_YH	O	CAPT_YH function.
LVLSHFT_IN0	I	Level shift input 0.
LVLSHFT_IN1	I	Level shift input 1.
LVLSHFT_OUT0	O	Level shift output 0.
LVLSHFT_OUT1	O	Level shift output 1.

9. Functional description

9.1 Arm Cortex-M0+ core

The Arm Cortex-M0+ core runs at an operating frequency of up to 15 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The Arm Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

9.2 On-chip flash program memory

The LPC804 contain up to 32 KB of on-chip EEPROM based flash program memory.

9.3 On-chip SRAM

The LPC804 contain a total of 4 KB on-chip static RAM data memory.

9.4 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART.
- On-chip ROM APIs for integer divide.
- Free Running Oscillator (FRO) API.

9.5 Memory map

The LPC804 incorporates several distinct memory regions. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The Arm private peripheral bus includes the Arm core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

9.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

9.6.1 Features

- Nested Vectored Interrupt Controller is a part of the Arm Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC804, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the Arm exceptions SVCall and PendSV.
- Supports NMI.

9.6.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

9.7 System tick timer

The Arm Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

9.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 12 “LPC804 clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.
- The LPC804 uses a dual voltage I/O feature. The pins on one side of the package are supplied by VDDIO and the pins on the other side are supplied by VDD. Each of these two supplies can be connected to different voltages within the allowed Vdd range. This feature allows the device to level-shift signals from one off-chip voltage domain to another.

9.13.1 Features

- Maximum data rates of up to 15 Mbit/s in master mode and up to 20 Mbit/s in slave mode for SPI functions connected to all digital pins.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

9.14 I^2C-bus interface (I^2C0 and I^2C1)

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master.

9.14.1 Features

- I^2C0 and I^2C1 support standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

9.15 Capacitive Touch Interface

The Capacitive Touch interface is designed to handle up to five capacitive buttons in different sensor configurations, such as slider, and button matrix. It operates in sleep, deep sleep, and power-down modes, allowing very low power performance.

The Capacitive Touch module measures the change in capacitance of an electrode plate when an earth-ground connected object (for example, finger) is brought within close proximity.

9.16 CTimer

9.16.1 General-purpose 32-bit timers/external event counter

The LPC804 has one general-purpose 32-bit timer/counter.

9.18 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

9.18.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

9.19 Self-Wake-up Timer (WKT)

The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

9.19.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the FRO. The low-power oscillator can be used as the clock source in sleep, deep-sleep, and power-down modes.
- The WKT can be used for waking up the part from any reduced power mode or for general-purpose timing.

9.20 Programmable Logic Unit (PLU)

The PLU is comprised of 26 5-input LUT elements. Each LUT element contains a 32-bit truth table (look-up table) register and a 32:1 multiplexer. During operation, the five LUT inputs control the select lines of the multiplexer. This structure allows any desired logical combination of the five LUT inputs.

9.24 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

9.24.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1’s complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

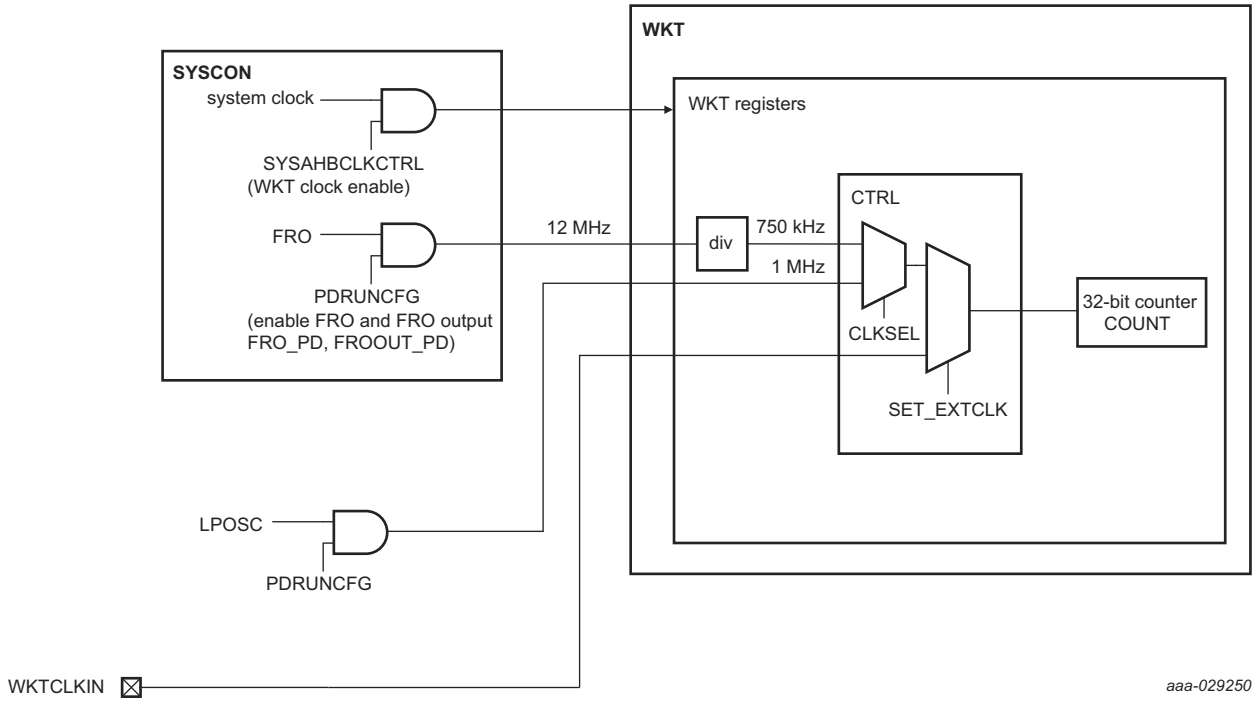


Fig 14. LPC804 WKT clocking

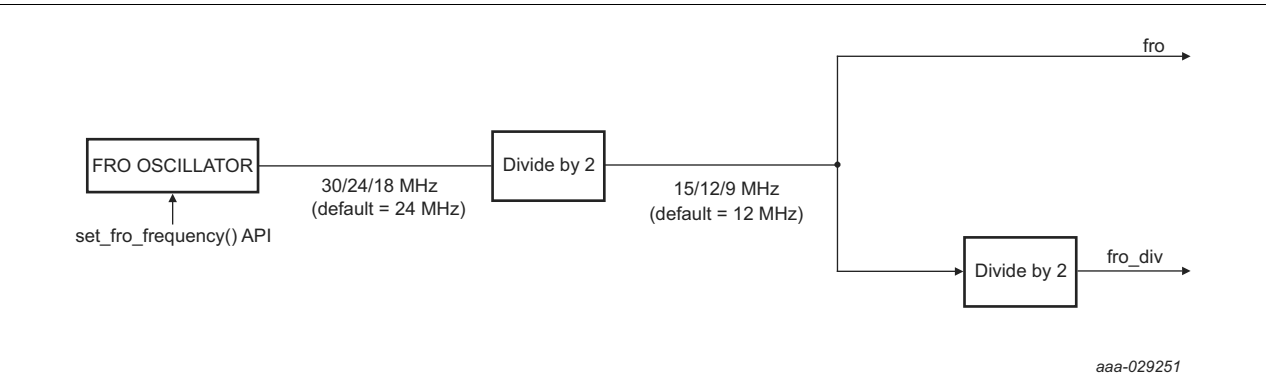


Fig 15. LPC804 FRO subsystem

Table 6. Clocking diagram signal name descriptions

Name	Description
clk_in	The internal clock that comes from the main CLK_IN pin function. That function must be connected to the pin by selecting it in the SWM block.
frg_clk	The output of the Fractional Rate Generator. The FRG and its source selection are shown in Figure 13.
fro_div	Divided output of the currently selected on-chip FRO oscillator. See Figure 15.
fro	The output of the currently selected on-chip FRO oscillator. See Figure 15.

Table 6. Clocking diagram signal name descriptions

Name	Description
main_clk	The main clock used by the CPU and AHB bus, and potentially many others. The main clock and its source selection are shown in Figure 12.
“none”	A tied-off source that should be selected to save power when the output of the related multiplexer is not used.
lposc_clk	The output of the 1 MHz low power oscillator. It must also be enabled in the PDRUNCFG0 register.

9.25.1 Internal oscillators

The LPC804 include two independent oscillators:

1. Free Running Oscillator.
2. Low power oscillator.

Following reset, the LPC804 operates from the FRO until switched by software allowing the part to run without any external clock and the bootloader code to operate at a known frequency.

See Figure 12 for an overview of the LPC804 clock generation.

9.25.1.1 Free Running Oscillator (FRO)

The FRO provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- This oscillator provides a selectable 15 MHz, 12 MHz, and 9 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 7.5 MHz, 6 MHz, and 4.5 MHz for system clock.
- The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- By default, the FRO output frequency is default system (CPU) clock frequency of 12 MHz.

9.25.1.2 Low Power Oscillator (LPOsc)

The LPOsc is an independent oscillator which can be used as a system clock. The frequency of the LPCOsc is 1 MHz.

9.25.2 Clock input

An external clock source can be supplied on the selected CLKIN pin. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 12 “Static characteristics, supply pins” and Table 18 “Dynamic characteristics: I/O pins[1]”.

The maximum frequency for both clock signals is 15 MHz.

9.25.3 Clock output

The LPC804 features a clock output function that routes any oscillator or the main clock can be selected to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

9.27 Emulation and debugging

Debug functions are integrated into the Arm Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The Arm Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the Arm SWD debug ($\overline{\text{RESET}}$ = HIGH). The Arm SWD debug port is disabled while the LPC804 is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode. See Table 4.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 12) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except the 3 V tolerant pin PIO0_7.

[4] Including the voltage on outputs in 3-state mode.

[5] V_{DD} present or not present.

[6] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[7] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[8] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[9] Dependent on package type.

[10] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[11] JEDEC (4.5 in × 4 in); still air.

[12] Single layer (4.5 in × 3 in); still air.

12. Static characteristics

12.1 General operating conditions

Table 11. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	15	MHz
V_{DD}	supply voltage (core and external rail)			1.71	-	3.6	V
		For ADC operations		2.5	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{DDIO}	I/O rail			1.71	-	3.6	V
		For ADC operations		2.5	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{ref}	ADC positive reference voltage	on pin VREFP		2.5	-	V_{DD}	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		pins with digital functions only	[2]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

12.2 Power consumption

Power measurements in active, sleep, deep-sleep, and power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.

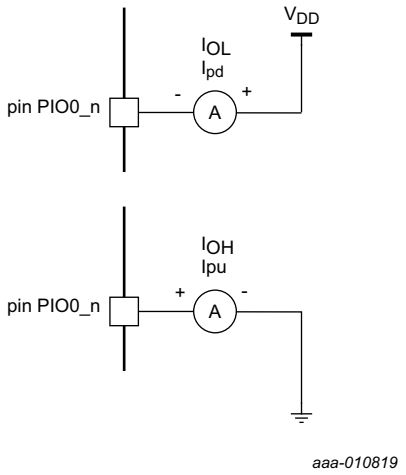
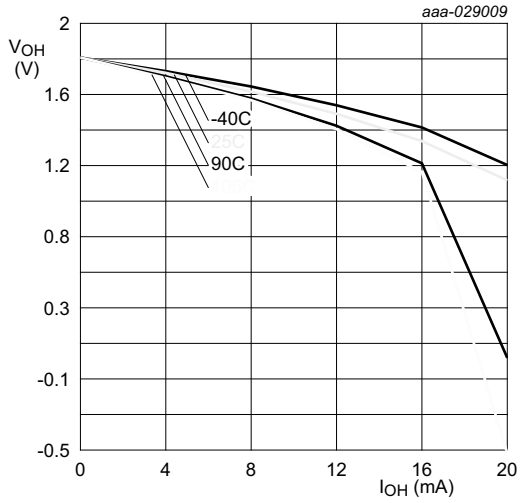
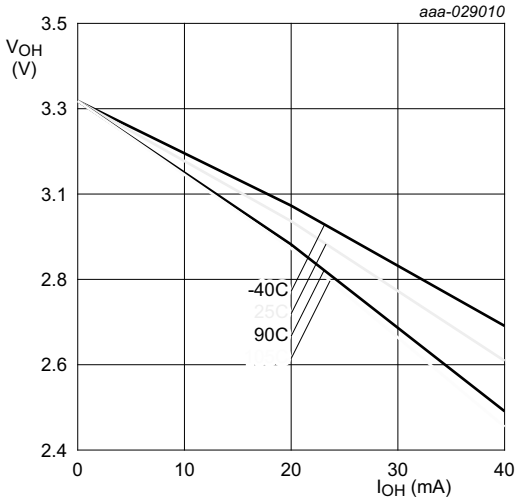


Fig 20. Pin input/output current measurement

12.3.1 Electrical pin characteristics

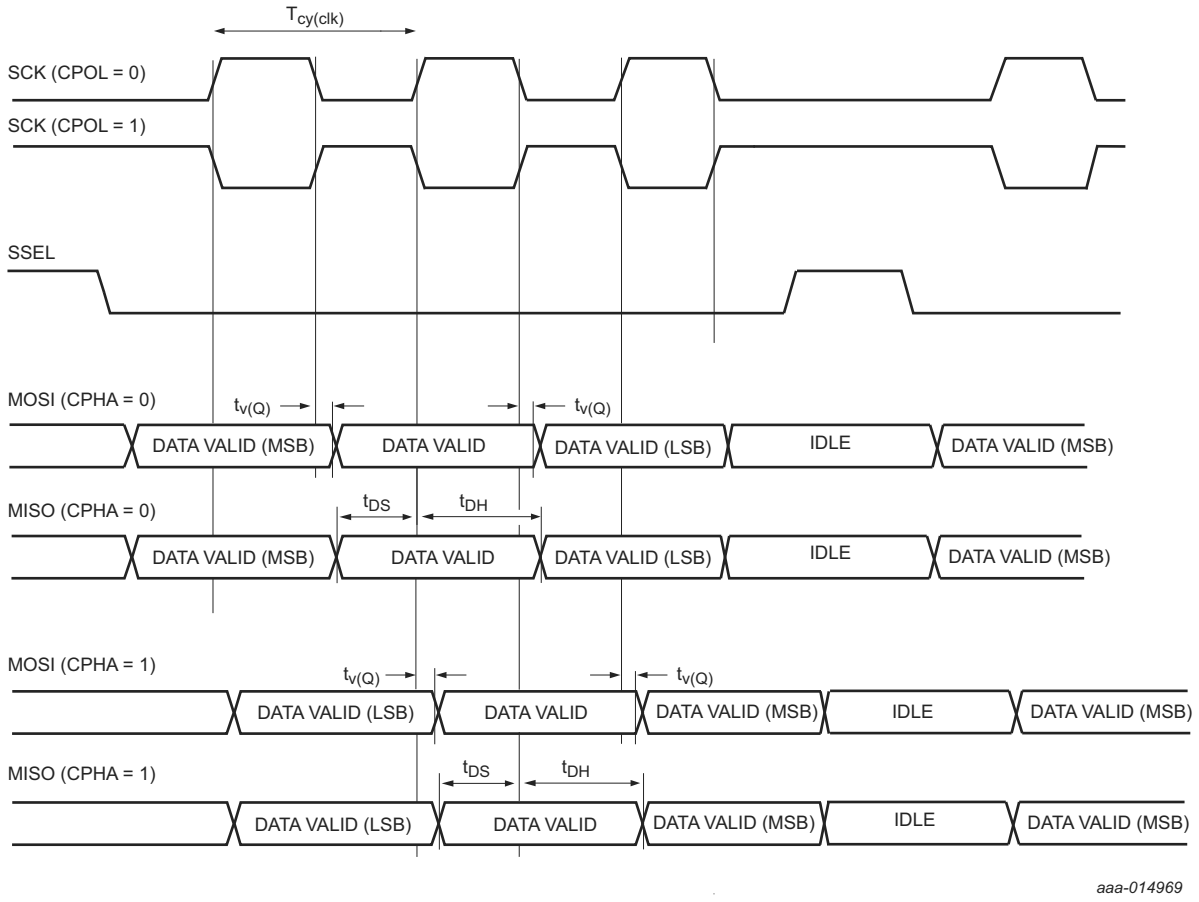


Conditions: V_{DD} = 1.8 V; on pin PIO0_12.



Conditions: V_{DD} = 3.3 V; on pin PIO0_12.

Fig 21. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the LPC804 *User manual*.

Fig 27. SPI master timing

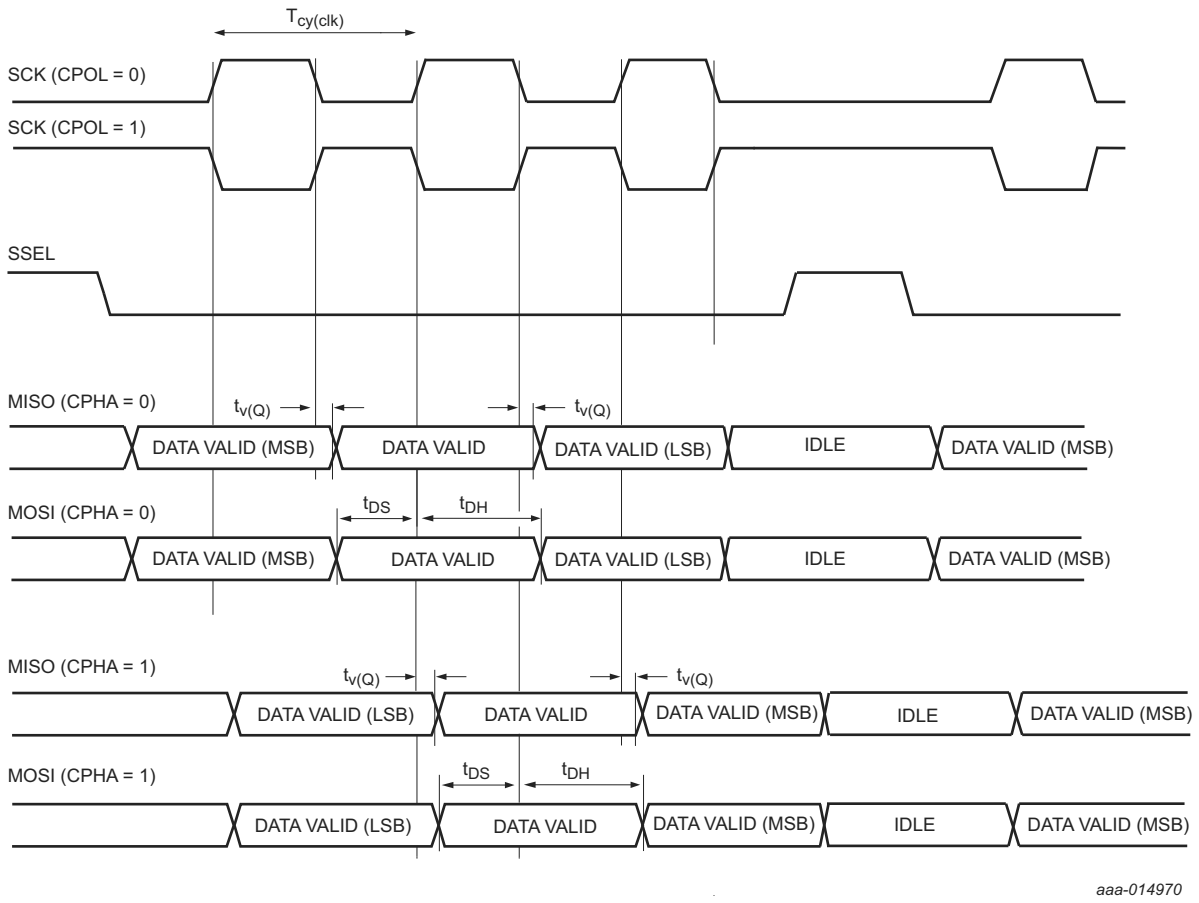


Fig 28. SPI slave timing

14.2 ADC

Table 25. 12-bit ADC static characteristics

T_{amb} = −25 °C to +105 °C unless noted otherwise; V_{DD} = 2.5 V to 3.6 V; VREFP = V_{DD}; VREFN = V_{SS}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DD}	V
V_{ref}	reference voltage	on pin VREFP		2.5	-	V_{DD}	V
C_{ia}	analog input capacitance			-	-	26	pF
$f_{clk(ADC)}$	ADC clock frequency		[2]	-	-	15	MHz
f_s	sampling frequency		[2]	-	-	480	Ksamples/s
E_D	differential linearity error		[5][4]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[6][4]	-	±4	-	LSB
E_O	offset error		[7][4]	-	±3	-	LSB
$V_{err(fs)}$	full-scale error voltage		[8][4]	-	0.1	-	%
Z_i	input impedance	f_s = 480 Ksamples/s	[1][9][10]	0.1	-	-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels. See Figure 30.

[2] In the ADC TRM register, set VRANGE = 0 (default).

[3] In the ADC TRM register, set VRANGE = 1 (default).

[4] Based on characterization. Not tested in production.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 30.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 30.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 30. For device revision 1B, typical offset value is ±3 LSB. For device revision 1A, the typical offset value is ±8 LSB.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 30.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 480 Ksamples/s and analog input capacitance C_{ia} = 26 pF.

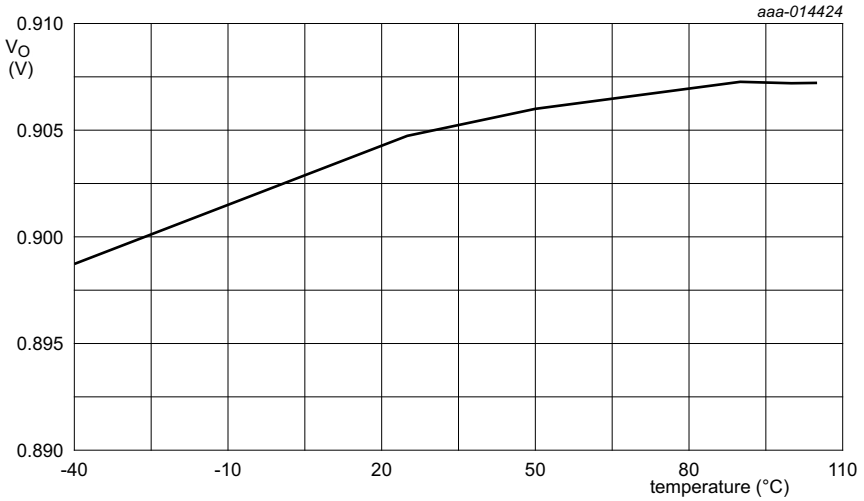
[10] Input impedance Z_i (see Section 14.2.1) is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 12 for C_{io}.

14.3 Comparator and internal voltage reference

Table 26. Internal voltage reference static and dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 3.3 V; hysteresis disabled in the comparator CTRL register.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = 25 °C to 105°C		860	-	940	mV
		T_{amb} = 25 °C			904		mV



V_{DD} = 3.3 V; characterized through bench measurements on typical samples.

Fig 32. Typical internal voltage reference output voltage

Table 27. Comparator characteristics

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.71 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin $ACMPV_{REF}$		1.5	-	3.6	V
I_{DD}	supply current	VP > VM; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	90	-	μA
		VM > VP; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	60	-	μA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V; V_{DD} = 3.0 V	[2]	-	4	-	mV
		V_{IC} = 1.5 V; V_{DD} = 3.0 V	[2]	-	6	-	mV
		V_{IC} = 2.9 V; V_{DD} = 3.0V	[2]	-	6	-	mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	13	-	μs