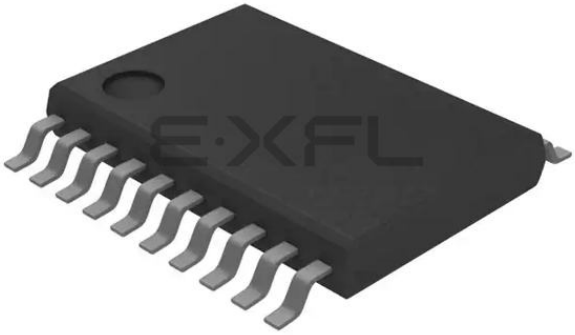

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	86MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	9
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-20
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc864l-1fri-5v-aa

2 General Device Information

2.1 Block Diagram

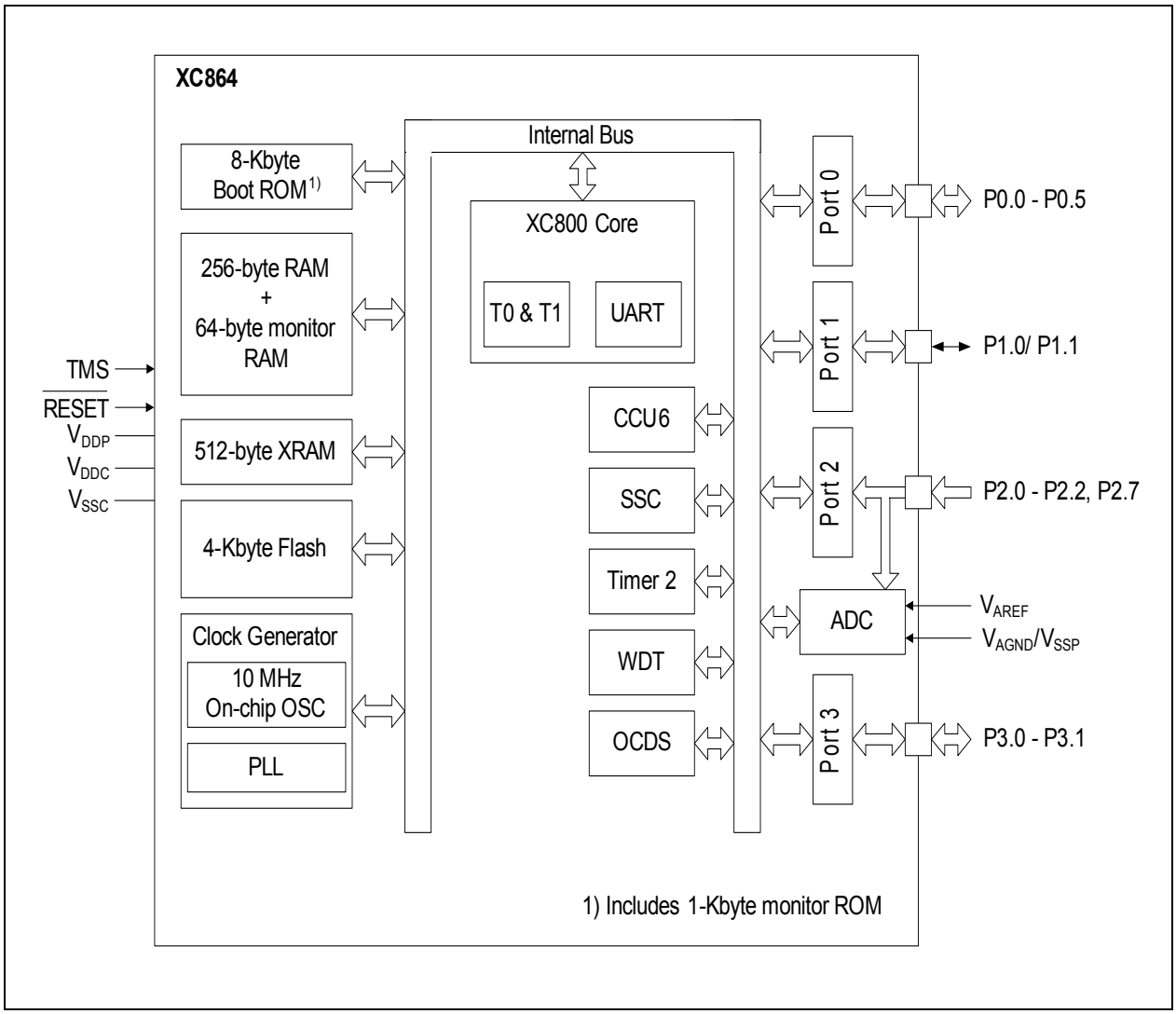

Figure 2 XC864 Block Diagram

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P1		I/O		**Port 1** Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 2 and SSC.
P1.0/ P1.1	15		PU	RXD_0 UART Receive Data Input T2EX Timer 2 External Trigger Input EXINT3 External Interrupt Input 3 T0 Timer 0 Input TDO_1 JTAG Serial Data Output TXD_0 UART Transmit Data Output/ Clock Output *Note: Pin 15 is bonded to both P1.0 and P1.1 port pins. See **Section 2.3** on the types of port pin configuration to be avoided to prevent permanent damage.*

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P3		I/O		**Port 3** Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6.
P3.0	16		Hi-Z	CCPOS1_2 CCU6 Hall Input 1 CC60_0 Input/Output of Capture/ Compare channel 0
P3.1	17		Hi-Z	CCPOS0_2 CCU6 Hall Input 0 CC61_2 Input/Output of Capture/ Compare channel 1 COUT60_0 Output of Capture/Compare channel 0
V_{DDP}	11	–	–	**I/O Port Supply (3.3 or 5.0 V)** Also used by EVR and analog modules. All pins must be connected.
V_{DDC}	3	–	–	**Core Supply Monitor (2.5 V)**
V_{SSC}	2	–	–	**Core Supply Ground**
V_{AREF}	13	–	–	**ADC Reference Voltage**
V_{AGND}/ V_{SSP}	12	–	–	**ADC Reference Ground/ I/O Ground** All pins must be connected.
TMS	4	I	PD	**Test Mode Select**
RESET	18	I	PU	**Reset Input**

Field	Bits	Type	Description
0	3	r	**Reserved** Returns 0 if read; should be written with 0.

Table 8 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CB_H	**ADC_RCR1** **Reset: 00_H** Result Control Register 1	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CC_H	**ADC_RCR2** **Reset: 00_H** Result Control Register 2	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CD_H	**ADC_RCR3** **Reset: 00_H** Result Control Register 3	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CE_H	**ADC_VFCR** **Reset: 00_H** Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, Page 5										
CA_H	**ADC_CHINFR** **Reset: 00_H** Channel Interrupt Flag Register	Bit Field	CHINF7	0				CHINF2	CHINF1	CHINF0
		Type	rh	rh				rh	rh	rh
CB_H	**ADC_CHINCR** **Reset: 00_H** Channel Interrupt Clear Register	Bit Field	CHINC7	0				CHINC2	CHINC1	CHINC0
		Type	w	w				w	w	w
CC_H	**ADC_CHINSR** **Reset: 00_H** Channel Interrupt Set Register	Bit Field	CHINS7	0				CHINS2	CHINS1	CHINS0
		Type	w	w				w	w	w
CD_H	**ADC_CHINPR** **Reset: 00_H** Channel Interrupt Node Pointer Register	Bit Field	CHINP7	0				CHINP2	CHINP1	CHINP0
		Type	rw	rw				rw	rw	rw
CE_H	**ADC_EVINFR** **Reset: 00_H** Event Interrupt Flag Register	Bit Field	EVINF7	EVINF6	EVINF5	EVINF4	0		EVINF1	EVINF0
		Type	rh	rh	rh	rh	r		rh	rh
CF_H	**ADC_EVINCR** **Reset: 00_H** Event Interrupt Clear Flag Register	Bit Field	EVINC7	EVINC6	EVINC5	EVINC4	0		EVINC1	EVINC0
		Type	w	w	w	w	r		w	w
$D2_H$	**ADC_EVINSR** **Reset: 00_H** Event Interrupt Set Flag Register	Bit Field	EVINS7	EVINS6	EVINS5	EVINS4	0		EVINS1	EVINS0
		Type	w	w	w	w	r		w	w
$D3_H$	**ADC_EVINPR** **Reset: 00_H** Event Interrupt Node Pointer Register	Bit Field	EVINP7	EVINP6	EVINP5	EVINP4	0		EVINP1	EVINP0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, Page 6										
CA_H	**ADC_CRCR1** **Reset: 00_H** Conversion Request Control Register 1	Bit Field	CH7	0			0			
		Type	rwh	rwh			r			
CB_H	**ADC_CRPR1** **Reset: 00_H** Conversion Request Pending Register 1	Bit Field	CHP7	0			0			
		Type	rwh	rwh			r			
CC_H	**ADC_CRMR1** **Reset: 00_H** Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLR PND	SCAN	ENSI	ENTR	0	ENGT
		Type	r	w	w	rw	rw	rw	r	rw
CD_H	**ADC_QMR0** **Reset: 00_H** Queue Mode Register 0	Bit Field	CEV	TREV	FLUSH	CLRV	TRMD	ENTR	0	ENGT
		Type	w	w	w	w	rw	rw	r	rw
CE_H	**ADC_QSR0** **Reset: 20_H** Queue Status Register 0	Bit Field	Rsv	0	EMPTY	EV	0			
		Type	r	r	rh	rh	r			
CF_H	**ADC_Q0R0** **Reset: 00_H** Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QBUR0** **Reset: 00_H** Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		

Table 12 OCDS Register Summary (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$F4_H$	**MMICR** **Reset: 00_H** Monitor Mode Interrupt Control Register	Bit Field	DVECT	DRETR	COMRST	MSTSEL	MMUIE_P	MMUIE	RRIE_P	RRIE
		Type	rwh	rwh	rwh	rh	w	rw	w	rw
$F5_H$	**MMDR** **Reset: 00_H** Monitor Mode Data Transfer Register *Receive*	Bit Field	MMRR							
		Type	rh							
$F6_H$	**HWBPSR** **Reset: 00_H** Hardware Breakpoints Select Register	Bit Field	0			BPSEL_P	BPSEL			
		Type	r			w	rw			
$F7_H$	**HWBPDR** **Reset: 00_H** Hardware Breakpoints Data Register	Bit Field	HWBPxx							
		Type	rw							

3.3.3 In-Application Programming

In some applications, the Flash contents may need to be modified during program execution. In-Application Programming (IAP) is supported so that users can program or erase the Flash memory from their Flash user program by calling some special subroutines. The Flash subroutines will first perform some checks and an initialization sequence before starting the program or erase operation. A manual check on the Flash data is necessary to determine if the programming or erasing was successful via using the 'MOVC' instruction to read out the Flash contents. Other special subroutines include aborting the Flash erase operation and checking the Flash bank ready-to-read status.

3.3.3.1 Flash Programming

Each call of the Flash program subroutine allows the programming of 32 bytes of data into the selected wordline (WL) of the Flash bank. Before calling the Flash program subroutine, the user must ensure that required inputs (**Table 14** and **Table 15**) are provided.

Flash Program Subroutine Type 1

If valid inputs have been set up, calling the subroutine begins flash programming. The subroutine exits and returns to the user code, while the target Flash bank is still in program mode, and is not accessible by user code.

The user code continues execution until the Flash NMI event is generated; bit FNMIFLASH in register NMISR is set, and if enabled via NMIFLASH, an NMI to the CPU is triggered to enter the Flash NMI service routine. At this point, the Flash bank is in ready-to-read mode.

Table 14 Flash Program Subroutin Type 1

Subroutine	$DFF6_H$: FSM_PROG
Input	DPTR (DPH, DPL[1]): Flash WL address
	R0 of Register Bank 3 (IRAM address 18_H): IRAM start address for 32-byte Flash data
	32-byte Flash data
	Flash NMI (NMICON.NMIFLASH) is enabled (1) or disabled (0)
Output	PSW.CY: 0 = Flash programming is in progress 1 = Flash programming is not started Flag FNMIFLASH will be set when Flash programming has successfully completed.
	DPTR is incremented by 20_H[2]

Table 14 Flash Program Subroutin Type 1 (cont'd)

Stack size required	12
Resource used/ destroyed	ACC, B, SCU_PAGE
	R0 – R7 of Register Bank 3 (IRAM address 18_H – $1F_H$) (8 bytes) IRAM address 36_H – $3D_H$ (8 bytes)

1) The last 5 LSB of the DPL is 0 for an aligned WL address, for e.g. 00_H, 20_H, 40_H, 60_H, 80_H, $A0_H$, $C0_H$ and $E0_H$..

2) DPTR is only incremented by 20_H when PSW.CY is 0.

Flash Program Subroutine Type 2

This routine will wait until Flash programming is completed before the user code can continue its execution. Therefore, background programming is not supported. This type of routine can be used to program the Flash bank where the user code is in execution. The Flash cannot be in both program mode and read mode at the same time. It can also be used for programming the Flash bank where the interrupt vectors are defined as interrupts cannot be handled when the Flash is in program mode.

Note: For the Flash programming of XC864 device, Flash Program Subroutine Type 2 is allowed. The users can also use Flash Program Subroutine Type 1 if it is called from XRAM.

Table 15 Flash Program Subroutine Type 2

Subroutine	$DFDB_H$: FSM_PROG_NO_BG
Input	DPTR (DPH, DPL[1]): Flash WL address
	R0 of Register Bank 3 (IRAM address 18_H): IRAM start address for 32-byte Flash data
	32-byte Flash data
	All interrupts including NMI must be disabled (0) Set SFR NMISR = 00_H
Output	PSW.CY: 0 = Flash programming is successful 1 = Flash programming is not successful due to: Flash Protection Mode 1 is enabled, or NMI has occurred Flag FNMIFLASH is cleared by this routine before return to user code.
	DPTR is incremented by 20_H[2]
Stack size required	15

3.4.2 Interrupt Source and Vector

Each interrupt source has an associated interrupt vector address. This vector is accessed to service the corresponding interrupt source request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC864 interrupt sources to the interrupt vector addresses and the corresponding interrupt source enable bits are summarized in **Table 18**.

Table 18 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC864	Enable Bit	SFR
NMI	0073_H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash NMI	NMIFLASH	
		VDDC Prewarning NMI	NMIVDD	
		VDDP Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003_H	External Interrupt 0	EX0	IEN0
XINTR1	$000B_H$	Timer 0	ET0	
XINTR2	0013_H	External Interrupt 1	EX1	
XINTR3	$001B_H$	Timer 1	ET1	
XINTR4	0023_H	UART	ES	
XINTR5	$002B_H$	T2	ET2	
		Fractional Divider (Normal Divider Overflow)		
		LIN		
XINTR6	0033_H	ADC	EADC	IEN1
XINTR7	$003B_H$	SSC	ESSC	
XINTR8	0043_H	External Interrupt 2	EX2	
XINTR9	$004B_H$	External Interrupt 3	EXM	
XINTR10	0053_H	CCU6 INP0	ECCIP0	
XINTR11	$005B_H$	CCU6 INP1	ECCIP1	
XINTR12	0063_H	CCU6 INP2	ECCIP2	
XINTR13	$006B_H$	CCU6 INP3	ECCIP3	

3.6 Power Supply System with Embedded Voltage Regulator

The XC864 microcontroller requires two different levels of power supply:

- 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 19 shows the XC864 power supply system. A power supply of 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

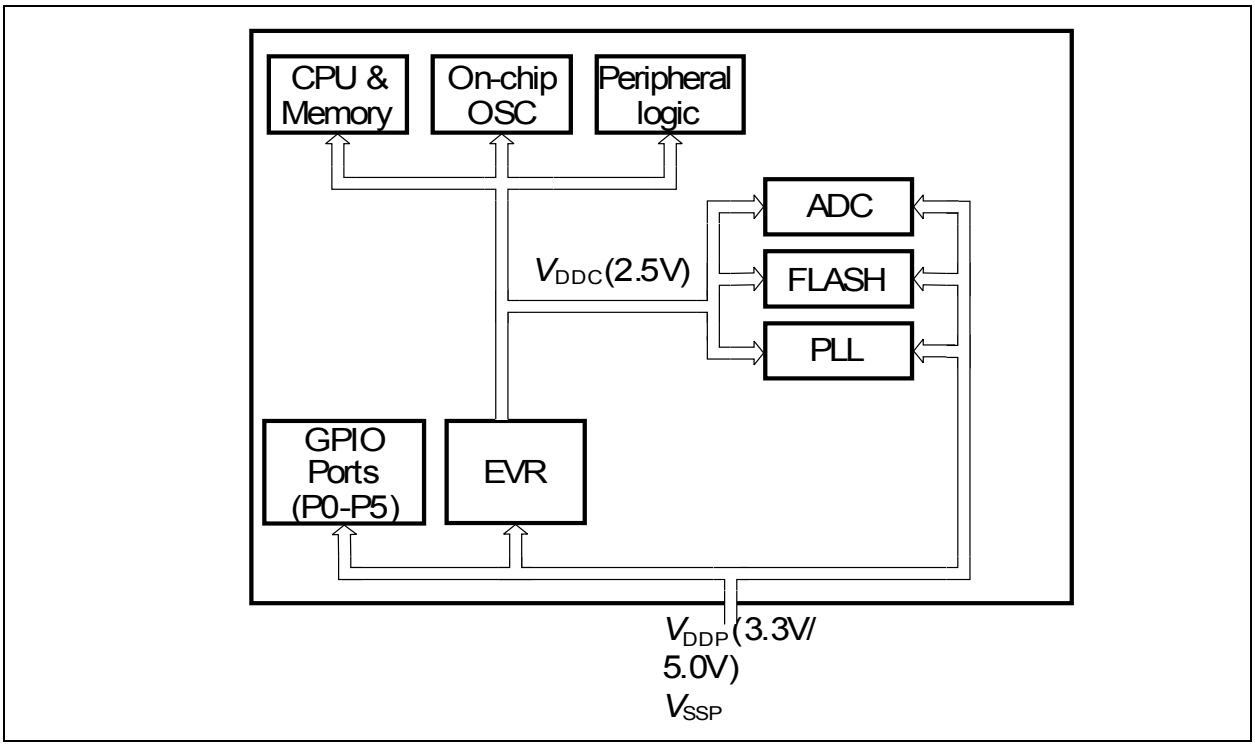

Figure 19 XC864 Power Supply System

EVR Features:

- Input voltage (V_{DDP}): 5.0 V
- Output voltage (V_{DDC}): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode
- V_{DDC} and V_{DDP} prewarning detection
- V_{DDC} brownout detection

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert WDTTO) and the reset prewarning is entered. The prewarning period lasts for 30_H count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from 0000_H to the value obtained from the concatenation of WDTWINB and 00_H.

After being serviced, the WDT continues counting up from the value (<WDTREL> * 2^8). The time period for an overflow of the WDT is programmable in two ways:

- the input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- the reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, P_{WDT}, between servicing the WDT and the next overflow can be determined by the following formula:

[4]

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}}$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period P_{WDT} between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 26**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB should not be smaller than WDTREL.

3.11.1 Baud-Rate Generator

The baud-rate generator is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 27**.

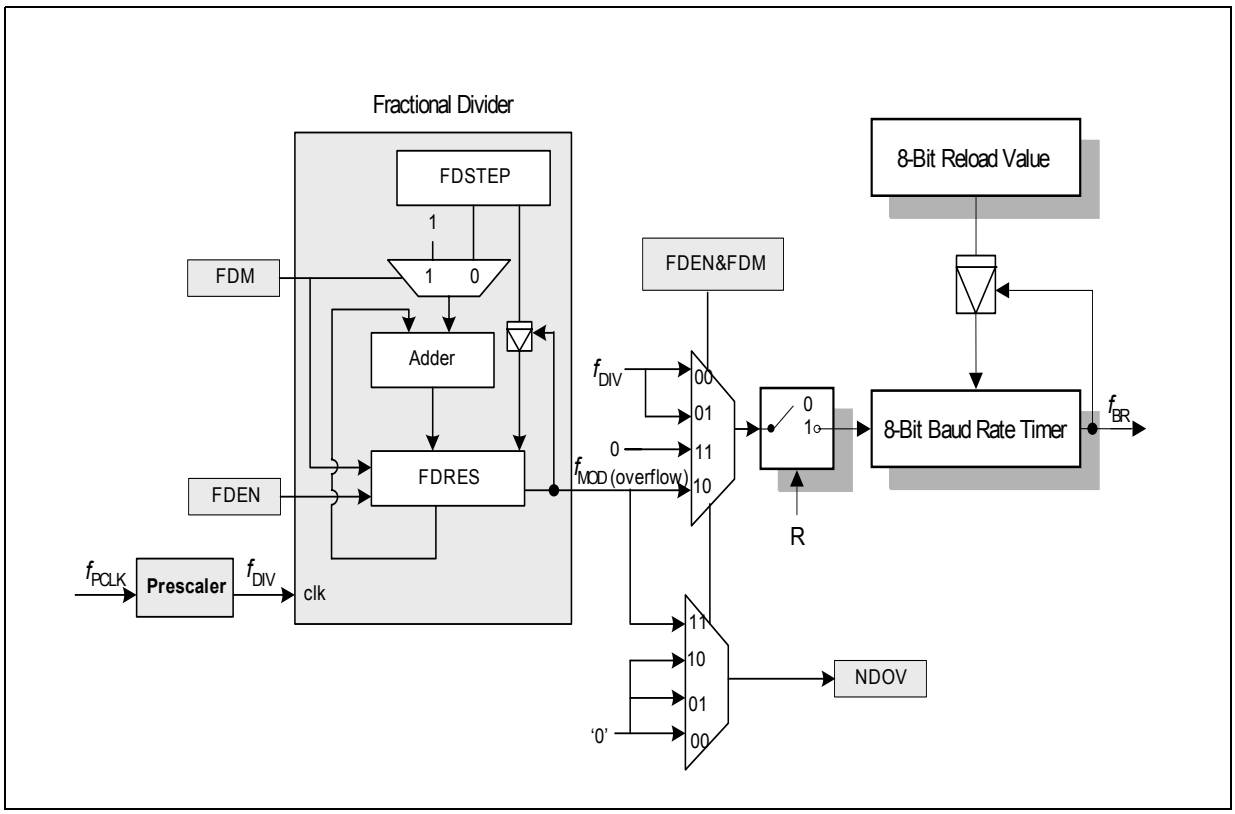

Figure 27 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.12**.

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP
  (to be considered only if fractional divider is enabled and operating in fractional divider mode)

3.18.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

The internal clock for the analog part f_{ADCI} is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures f_{ADCI} does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

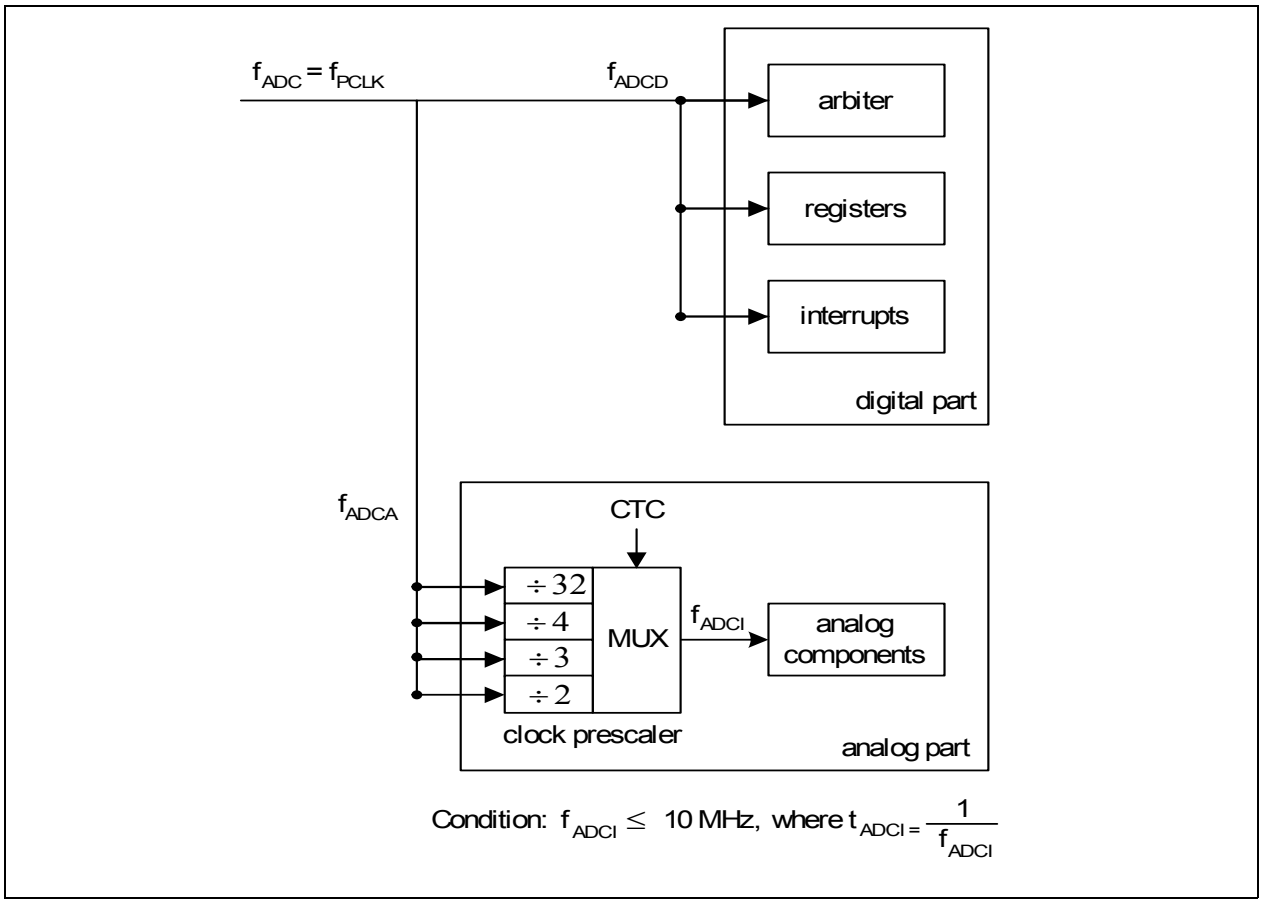

Figure 31 ADC Clocking Scheme

For module clock f_{ADC} = 26.7 MHz, the analog clock f_{ADCI} frequency can be selected as shown in **Table 30**.

Table 30 f_{ADCI} Frequency Selection

Module Clock f_{ADC}	CTC	Prescaling Ratio	Analog Clock f_{ADCI}
26.7 MHz	00_B	÷ 2	13.3 MHz (N.A)
	01_B	÷ 3	8.9 MHz
	10_B	÷ 4	6.7 MHz
	11_B (default)	÷ 32	833.3 kHz

As f_{ADCI} cannot exceed 10 MHz, bit field CTC should not be set to 00_B when f_{ADC} is 26.7 MHz. During slow-down mode where f_{ADC} may be reduced to 13.3 MHz, 6.7 MHz etc., CTC can be set to 00_B as long as the divided analog clock f_{ADCI} does not exceed 10 MHz. However, it is important to note that the conversion error could increase due to loss of charges on the capacitors, if f_{ADC} becomes too low during slow-down mode.

3.18.2 ADC Conversion Sequence

The analog-to-digital conversion procedure consists of the following phases:

- Synchronization phase (t_{SYN})
- Sample phase (t_S)
- Conversion phase
- Write result phase (t_{WR})

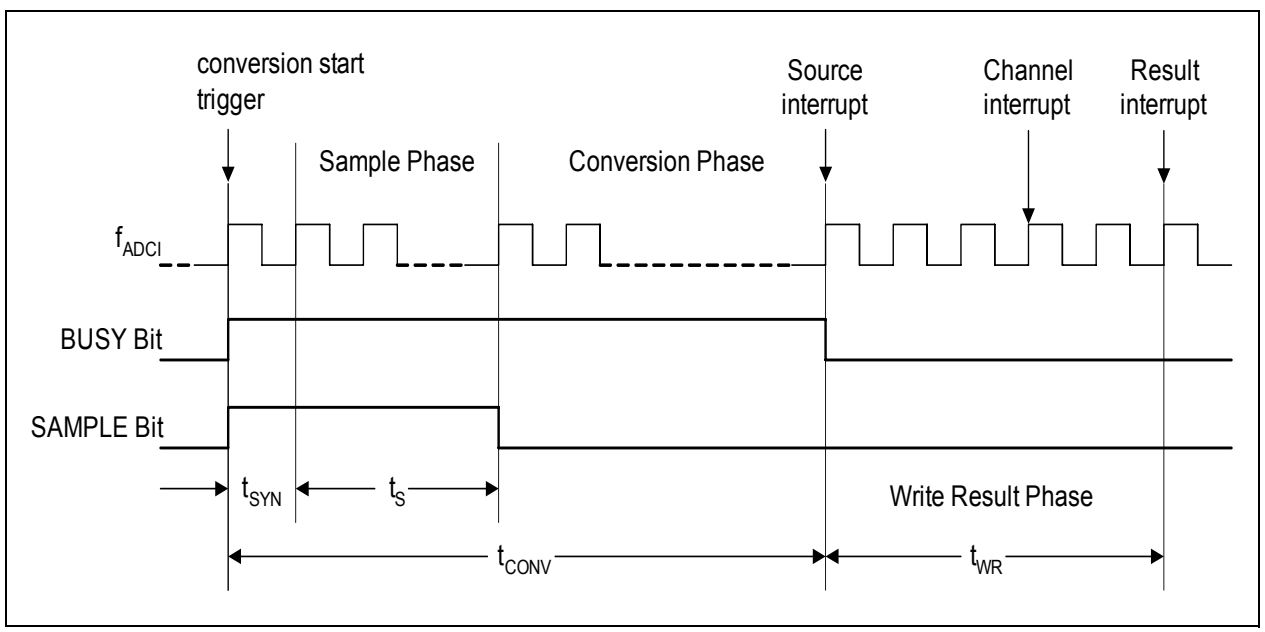

Figure 32 ADC Conversion Timing

3.20 Chip Identification Number

The XC864 identity (ID) register is located at Page 1 of address $B3_H$. The value of ID register is $1B_H$. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product, variant type and device step information.

The Chip Identification Numbers associated with XC864 are $1B810C00_H$ for 5V device and $1B010C00_H$ for 3.3V device.

Two methods are provided to read a device's Chip Identification Number:

- In-application subroutine, GET_CHIP_INFO
- Bootstrap loader (BSL) mode A

4.2 DC Parameters

4.2.1 Input/Output Characteristics

Table 33 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
V_{DDP} = 5V Range						
Output low voltage	V_{OL}	CC	–	1.0	V	I_{OL} = 15 mA
			–	0.4	V	I_{OL} = 5 mA
Output high voltage	V_{OH}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -15 mA
			V_{DDP} - 0.4	–	V	I_{OH} = -5 mA
Input low voltage on port pins (all except P0.0 & P0.1)	V_{ILP}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on P0.0 & P0.1	V_{ILP0}	SR	-0.2	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on RESET pin	V_{ILR}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on TMS pin	V_{ILT}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input high voltage on port pins (all except P0.0 & P0.1)	V_{IHP}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input high voltage on P0.0 & P0.1	V_{IHP0}	SR	0.7 × V_{DDP}	V_{DDP}	V	CMOS Mode
Input high voltage on RESET pin	V_{IHR}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input high voltage on TMS pin	V_{IHT}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input Hysteresis[1)]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode
Pull-up current[2)]	I_{PU}	SR	–	-10	µA	$V_{IH,min}$
			-150	–	µA	$V_{IL,max}$

Table 33 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Maximum current into V_{DDP}	I_{MVDDP} SR	–	80	mA	
Maximum current out of V_{SS}	I_{MVSS} SR	–	80	mA	

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) Single pull device is enabled for the measurement of P0.0/P1.0.

3) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and RESET pin have internal pull devices and are not included in the input leakage current characteristic.

4) Not subjected to production test, verified by design/characterization.

5) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Table 35 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol	Limit Values			Unit	Test Conditions/ Remarks
		min.	typ .	max.		
Switched capacitance at the analog voltage inputs	C_{AINSW} CC	–	5	7	pF	2)4)
Input resistance of the reference input	R_{AREF}CC	–	1	2	kΩ	2)
Input resistance of the selected analog channel	R_{AIN} CC	–	1	1.5	kΩ	2)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V , V_{DDP} = 5.0 V.

2) Not subject to production test, verified by design/characterization.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

4) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.

Table 38 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 3.3V range)

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ.[1]	max.[2]		
V_{DDP} = 3.3V Range					
Active Mode	I_{DDP}	21.6	23.3	mA	[3]
Idle Mode	I_{DDP}	12	13.5	mA	[4]
Active Mode with slow-down enabled	I_{DDP}	5.7	7.3	mA	[5]
Idle Mode with slow-down enabled	I_{DDP}	5.4	6.9	mA	[6]

1) The typical I_{DDP} values are periodically measured at T_A = + 25 °C and V_{DDP} = 3.3 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 125 °C and V_{DDP} = 3.6 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 26.7 MHz (set by on-chip oscillator of 10 MHz and NDIV in PLL_CON to 0010_B), $\overline{RESET}$ = V_{DDP}, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 26.7 MHz, $\overline{RESET}$ = V_{DDP}, no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 833 KHz by setting CLKREL in CMCON to 0101_B, $\overline{RESET}$ = V_{DDP}, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enable and running at 833 KHz by setting CLKREL in CMCON to 0101_B,, $\overline{RESET}$ = V_{DDP}, no load on ports.

Table 39 Power Down Current (Operating Conditions apply; V_{DDP} = 3.3V range)

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ.[1]	max.[2]		
V_{DDP} = 3.3V Range					
Power-Down Mode[3]	I_{PDP}	1	10	µA	T_A = + 25 °C.[4]
		-	35	µA	T_A = + 85 °C.[4][5]

1) The typical I_{PDP} values are measured at V_{DDP} = 3.3 V.

2) The maximum I_{PDP} values are measured at V_{DDP} = 3.6 V.

3) I_{PDP} (power-down mode) has a maximum value of 200 µA at T_A = + 125 °C.

4) I_{PDP} (power-down mode) is measured with: $\overline{RESET}$ = V_{DDP}, V_{AGND}= V_{SS}, RXD/INT0= V_{DDP}; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

5) Not subject to production test, verified by design/characterization.

4.3.5 JTAG Timing

Table 43 TCK Clock Timing (Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TCK clock period	t_{TCK}	SR	50	–	ns
TCK high time	t_1	SR	20	–	ns
TCK low time	t_2	SR	20	–	ns
TCK clock rise time	t_3	SR	–	4	ns
TCK clock fall time	t_4	SR	–	4	ns

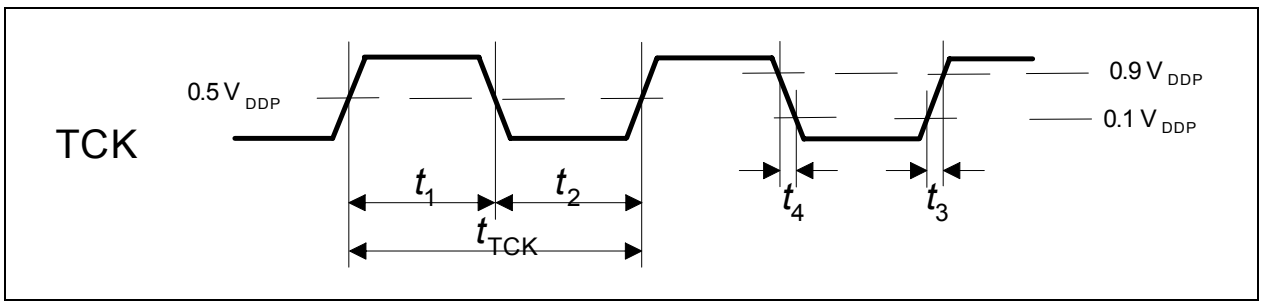

Figure 41 TCK Clock Timing