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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	112MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k142uft0vllt

Table of Contents

1 Block diagram....4
2 Feature comparison....5
3 Ordering parts....7
3.1 Determining valid orderable parts....7
3.2 Ordering information....8
4 General....9
4.1 Absolute maximum ratings....9
4.2 Voltage and current operating requirements....10
4.3 Thermal operating characteristics....11
4.4 Power and ground pins....12
4.5 LVR, LVD and POR operating requirements....13
4.6 Power mode transition operating behaviors....14
4.7 Power consumption....15
4.7.1 Modes configuration....18
4.8 ESD handling ratings....18
4.9 EMC radiated emissions operating behaviors....18
5 I/O parameters....18
5.1 AC electrical characteristics....18
5.2 General AC specifications....19
5.3 DC electrical specifications at 3.3 V Range....19
5.4 DC electrical specifications at 5.0 V Range....20
5.5 AC electrical specifications at 3.3 V range....21
5.6 AC electrical specifications at 5 V range....22
5.7 Standard input pin capacitance....22
5.8 Device clock specifications....22
6 Peripheral operating requirements and behaviors....23
6.1 System modules....23
6.2 Clock interface modules....23
6.2.1 External System Oscillator electrical specifications....23
6.2.2 External System Oscillator frequency specifications....25
6.2.3 System Clock Generation (SCG) specifications....26
6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications....26
6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications....26
6.2.4 Low Power Oscillator (LPO) electrical specifications....27
6.2.5 SPLL electrical specifications....27
6.3 Memory and memory interfaces....27
6.3.1 Flash memory module (FTFC) electrical specifications....27
6.3.1.1 Flash timing specifications — commands....27
6.3.1.2 Reliability specifications....29
6.3.2 QuadSPI AC specifications....30
6.4 Analog modules....34
6.4.1 ADC electrical specifications....34
6.4.1.1 12-bit ADC operating conditions....34
6.4.1.2 12-bit ADC electrical characteristics....36
6.4.2 CMP with 8-bit DAC electrical specifications....37
6.5 Communication modules....41
6.5.1 LPUART electrical specifications....41
6.5.2 LPSPI electrical specifications....41
6.5.3 LPI2C electrical specifications....48
6.5.4 FlexCAN electical specifications....49
6.5.5 SAI electrical specifications....49
6.5.6 Ethernet AC specifications....51
6.5.7 Clockout frequency....54
6.6 Debug modules....54
6.6.1 SWD electrical specofications....54
6.6.2 Trace electrical specifications....56
6.6.3 JTAG electrical specifications....57
7 Thermal attributes....60
7.1 Description....60
7.2 Thermal characteristics....60
7.3 General notes for specifications at maximum junction temperature....64
8 Dimensions....65
8.1 Obtaining package dimensions....65
9 Pinouts....66
9.1 Package pinouts and signal descriptions....66
10 Revision History....66

1 Block diagram

Following figures show superset high level architecture block diagrams of S32K14x series and S32K11x series respectively. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.

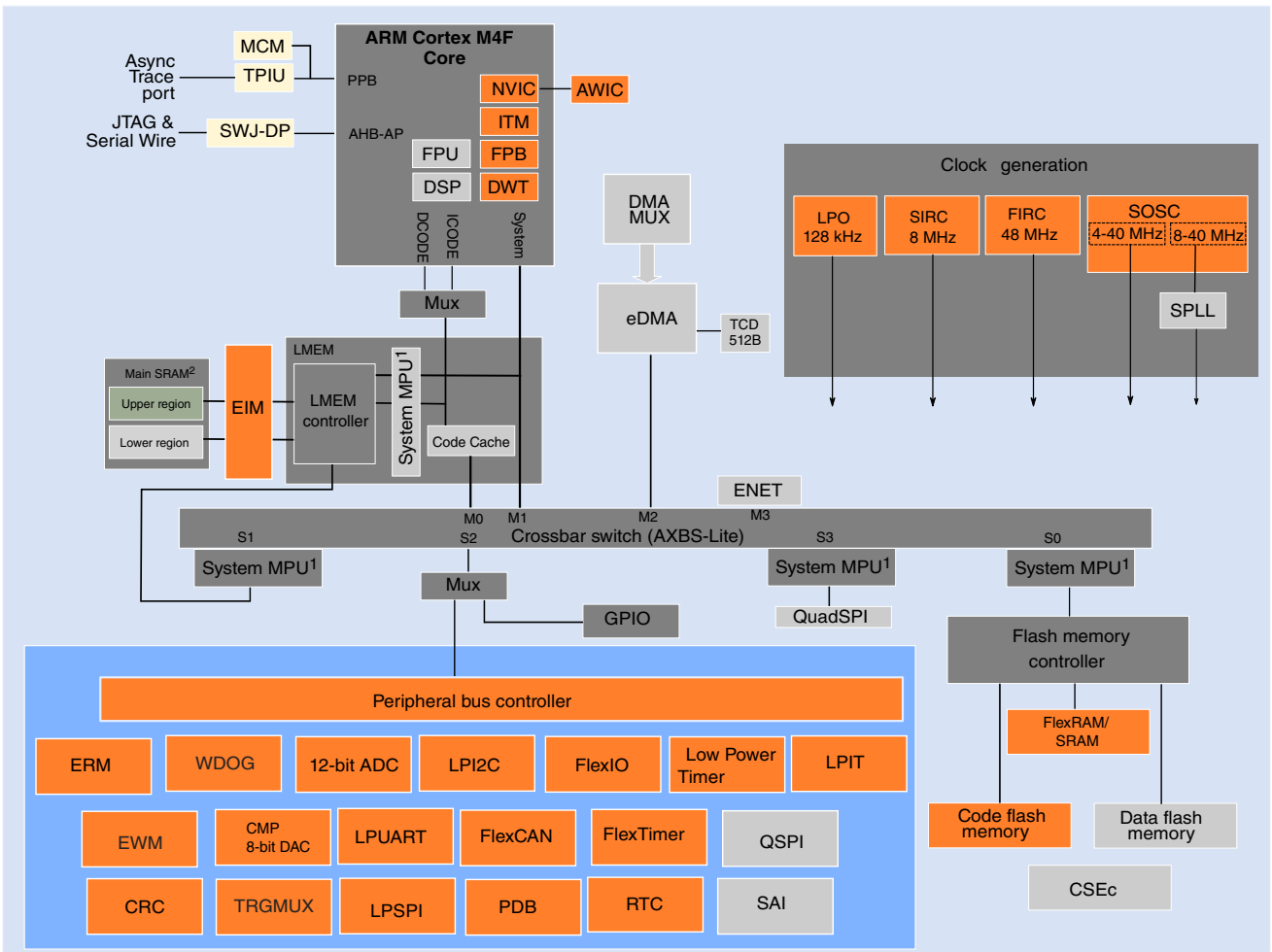
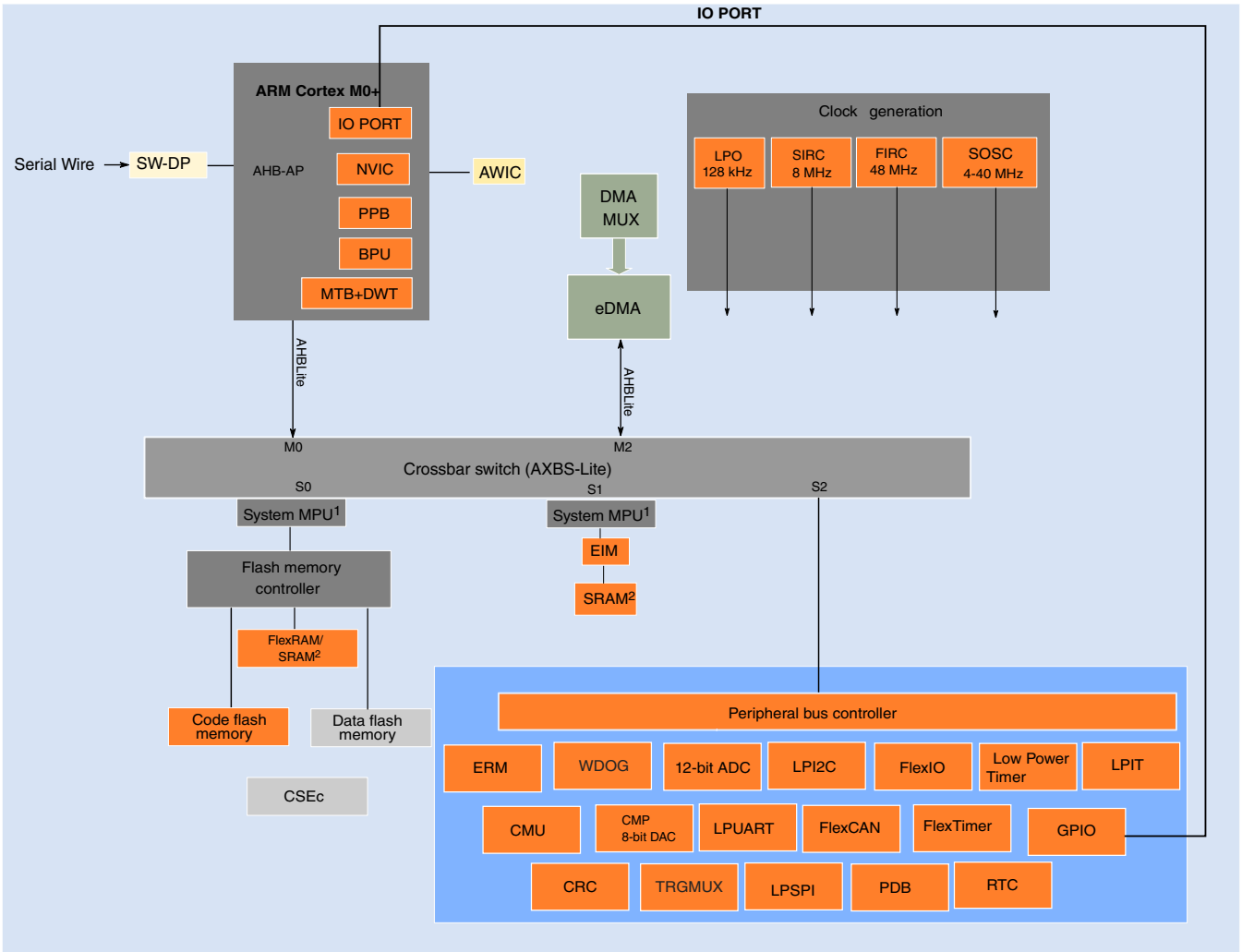


Figure 1. High-level architecture diagram for the S32K14x family



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Crossbar master (Core, DMA) can be assigned different access rights to each protected memory region. The ARM M0+ core version in this family does not integrate the ARM Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

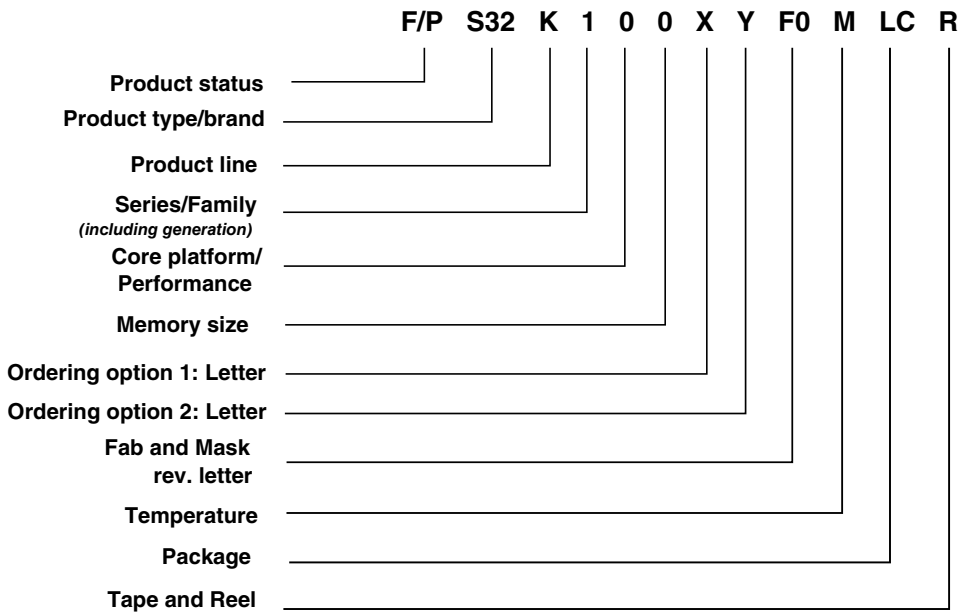
Key:
- Device architectural IP on all S32K devices
- Peripherals present on all S32K devices
- Peripherals present on selected S32K devices (see the "Feature Comparison" section in the RM)

Figure 2. High-level architecture diagram for the S32K11x family

2 Feature comparison

The following figure summarizes the memory and package options for the S32K product series and demonstrates where this device fits within the overall series. All devices which share a common package are pin-to-pin compatible.

3.2 Ordering information



Product status
P: Prototype
F: Qualified ordering P/N

Product type/brand
S32: Automotive 32-bit MCU

Product line
K: ARM Cortex MCUs
M: MagniV/Mixed Signal

Series/Family
1: 1st product series
2: 2nd product series

Core platform/Performance
1: ARM Cortex M0+
4: ARM Cortex M4F

Memory size

	2	4	6	8
M0+	32 K	64 K	128 K	256 K
M4F	256 K	512 K	1 M	2 M

Ordering option
X: Speed
B: 48 MHz without DMA (only for S32K11x)
L: 48 MHz with DMA (only for S32K11x)
M: 64 MHz
H: 80 MHz
U: 112 MHz

Y: Optional feature
N: No/None
R: Max. RAM
F: CAN-FD and FlexIO including max. RAM
S: Security including max. RAM
A: CAN-FD, FlexIO, and Security including max. RAM
E: Ethernet and audio including max. RAM
J: CAN FD, FlexIO, Security, Ethernet and audio including max. RAM

Fab and Mask rev. letter
Fx: ATMC
Tx: GF
XX: Flex #

x0: 1st fab revision
x1: 2nd fab revision

Temperature
C: -40C to 85C
V: -40C to 105C
M: -40C to 125C

Package

Pins	LQFP	LQFP -EP	QFN	BGA
32	LC	-	FM	-
48	LF	KF	FT	-
64	LH	KH	-	-
100	LL	-	-	MH
144	LQ	-	-	-
176	LU	-	-	-

Tape and Reel
T: Trays and Tubes
R: Tape and Reel

Figure 4. Ordering information

4.4 Power and ground pins

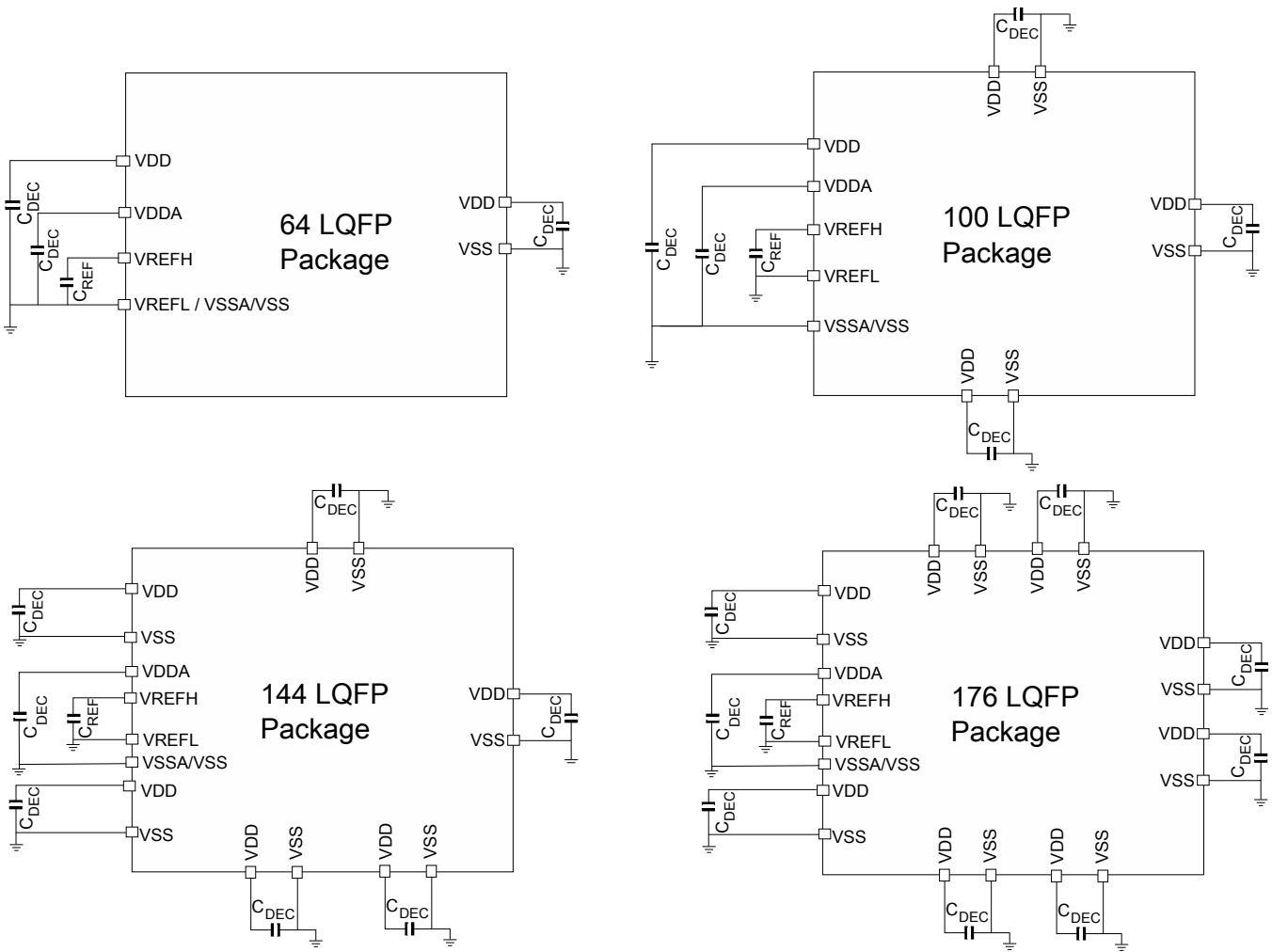


Figure 5. Pinout decoupling

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. 3	Typ.	Max.	Unit
C_{REF}, 4, 5	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} 5, 6, 7	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
   - The protection/decoupling capacitors must be on the path of the trace connected to that component.

Table 7. Power consumption (Typicals unless stated otherwise) 1 (continued)

	Ambient Temperature (°C)		VLPS (µA)[2, 3]		VLPR (mA)		STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [4]		Idd/MHz (µA/MHz)[5]
	85	Typ	150	159	1.72	1.85	7.2	8.1	20.4	27.1	26.1	33.5	30.5	40	43.9	56.1	381
		Max	359	384	2.60	2.65	8.3	9.2	21.9	28.5	27.8	34.4	32.9	41.5	45.5	57.5	411
	105	Typ	256	273	1.80	2.10	7.8	8.5	20.6	27.4	26.6	33.8	31.2	40.5	44.8	57.1	390
		Max	850	900	2.65	2.70	10.3	10.6	22.7	30	28.3	36.5	33.4	43.3	47.9	61.3	418
	125	Max	1960	1998	3.18	3.25	12.2	13	25.3	32.7	35	39.8	37.1	46.5	NA	NA	464
S32K146	25	Typ	40	55	5	6	15	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	95	110	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	70	80	NA	NA	TBD
S32K148[7, 8]	25	Typ	40	60	5	6	15	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	120	125	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	100	110	NA	NA	TBD

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration.
2. This is an average based on the use case described in the Comparator section, whereby the analog sampling is taking place periodically, with a mechanism to only enable the DAC as required. The numbers quoted assumes that only a single ANLCMP is active and the others are disabled
3. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
4. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
5. Values mentioned are measured at 25 ℃ at RUN@80 MHz with peripherals disabled.
6. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
7. Above S32K148 data is preliminary targets only
8. The S32K148 data points assume that ENET/QuadSPI/SAI etc. are active. If the same configuration is selected as per the S32K144, then the two devices will have very similar IDD.

Table 10. DC electrical specifications at 5.0 V Range (continued)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
Ioh_Strong	I/O current source capability measured when pad = V_{DDE} - 0.8 V	20	—	—	mA	3, 4
Iol_Strong	I/O current sink capability measured when pad = 0.8 V	20	—	—	mA	4, 5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	7
R_{PD}	Internal pulldown resistors	20		50	kΩ	8

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
4. The strong pad I/O pin is capable of switching a 50 pF load at up to 40 MHz.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. Measured at input V = V_{SS}
8. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 11. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
Standard	NA	4.6	14.5	3.9	15.7	25
		7.2	23.7	6.2	26.2	50
		24.0	75.4	20.8	88.4	200
Strong	0	4.6	14.5	3.9	15.7	25
		7.2	23.7	6.2	26.2	50
		24.0	75.4	20.8	88.4	200
	1	2.0	5.8	1.8	6.1	25
		2.8	8.0	2.6	8.3	50
		7.0	20.7	6.0	22.4	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

Table 14. Device clock specifications 1 (continued)

Symbol	Description	Min.	Max.	Unit
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) [3]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode[4]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

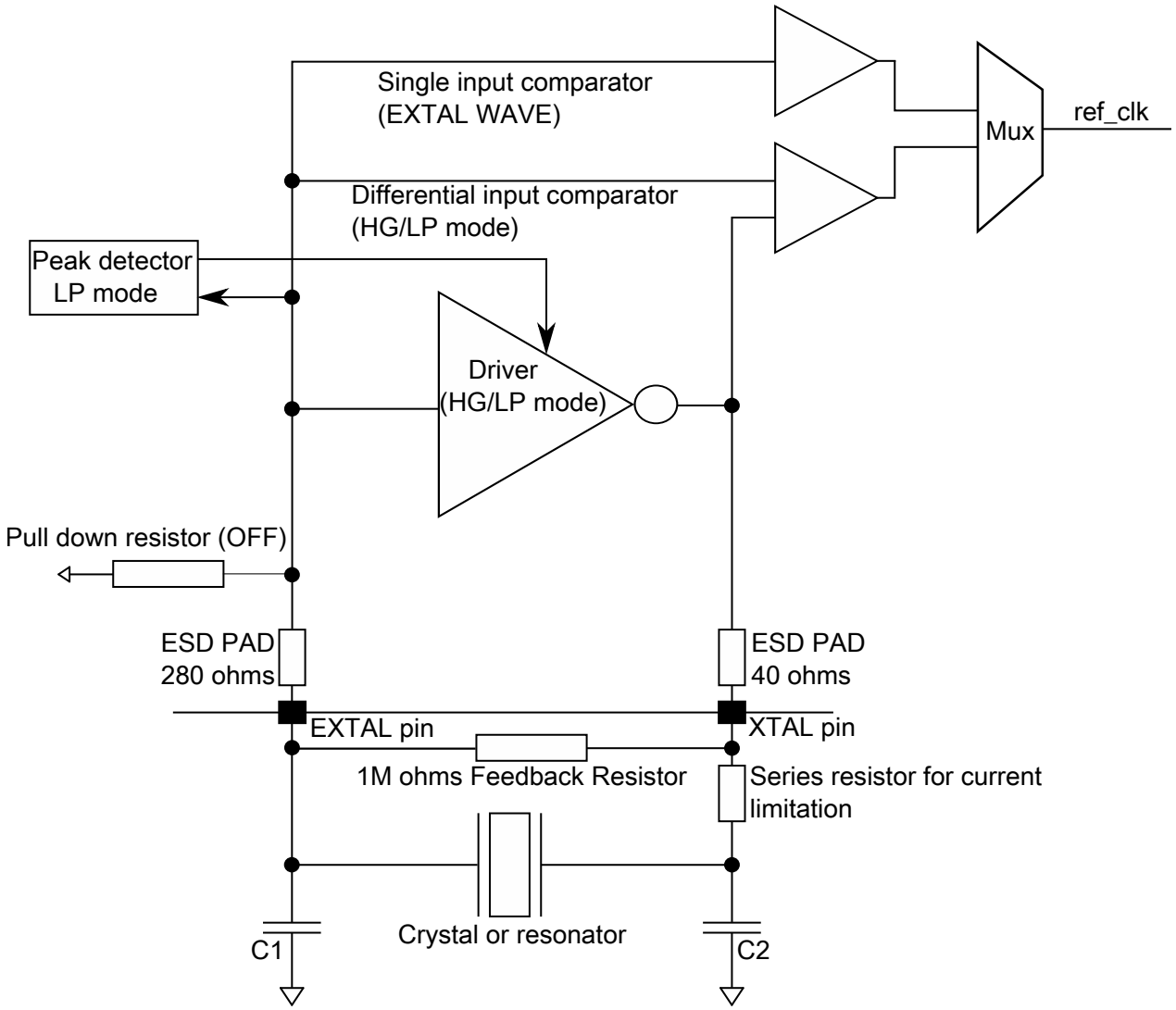


Figure 8. Oscillator connections scheme

Table 15. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	4-8 MHz	2.2	—	13.7	mA/V	
	8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	0.35 * V_{DD}	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

Symbol	Description[1]	Min.	Typ.	Max.	Unit	Notes
$t_{eewr16b64k}$	• 48 KB EEPROM backup • 64 KB EEPROM backup	—	475	2000	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	µs	
$t_{eewr32b32k}$ $t_{eewr32b48k}$ $t_{eewr32b64k}$	32-bit write to FlexRAM execution time: • 32 KB EEPROM backup • 48 KB EEPROM backup • 64 KB EEPROM backup	— — —	630 720 810	2000 2125 2250	µs µs µs	3, 4
$t_{quickwr}$	32-bit Quick Write execution time : Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)					
	• 1st 32-bit write • 2nd through Next to Last (Nth-1) 32-bit write • Last (Nth) 32-bit write (time for write only, not cleanup)	— — —	200 150 200	550 550 550	µs µs µs	5, 6
$t_{quickwrClnup}$	Quick Write Cleanup execution time	—	—	(Number of Quick Writes) * 2.0	ms	7

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record clean up has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 'First time' EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. For 'Typ.', only after the Nth write completes will any data will be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power or reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write may take up to 550 µs as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

6.3.1.2 Reliability specifications

Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						

Table continues on the next page...

Table 23. QuadSPI electrical specifications

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		Extrenal DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Register Settings																		
MCR[DDR_EN]		-	0		0		0		0		0		0		0		1	
MCR[DQS_EN]		-	0		1		1		0		1		1		0		1	
MCR[SCLKCFG[0]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[1]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[2]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[3]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[5]]		-	-		-		-		-		-		-		-		1	
SMPR[FSPHS]		-	0		1		0		0		1		0		0		0	
SMPR[FSDLY]		-	0		0		0		0		0		0		0		0	
SOCCR [SOCCFG[7:0]]			-		0		23		-		0		30		-		-	
SOCCR[SOCCFG[15:8]]		-	-		-		-		-		-		-		-		30	
FLSHCR[TDH]		-	0x00		0x00		0x00		0x00		0x00		0x00		0x00		0x01	
Timing Parameters																		
SCK Clock Frequency	f_{SCK}	MHz	-	38	-	64	-	48	-	40	-	80	-	50	-	20	-	20[4]
SCK Clock Period	t_{SCK}	ns	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	50.0	-	50.0[4]	-

Table continues on the next page...

6.4.1.2 12-bit ADC electrical characteristics

NOTE

ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.

Table 25. 12-bit ADC characteristics (2.7 V to 3 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC		—	0.6	1.5	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±2.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to half the ADC clock frequency.
2. Typical values assume V_{DDA} = 3 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF, 100 LQFP package unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

Table 26. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	2.1	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	

Table continues on the next page...

Table 29. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_v	Data valid (after SPSCK edge)	Slave	-	30	-	39	-	26	-	36	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback[5]	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow) [6]	-	8	-	10	-	7	-	9	-	44	-	44	
11	t_{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback[5]	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	
			Master Loopback(slow) [6]	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	$t_{RI/FI}$	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		
			Master Loopback[5]	-		-		-		-		-		-		
			Master Loopback(slow) [6]	-		-		-		-		-		-		
13	$t_{RO/FO}$	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		
			Master Loopback [5]	-		-		-		-		-		-		
			Master Loopback(slow) [6]	-		-		-		-		-		-		

1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. f_{periph} = LPSPI peripheral clock

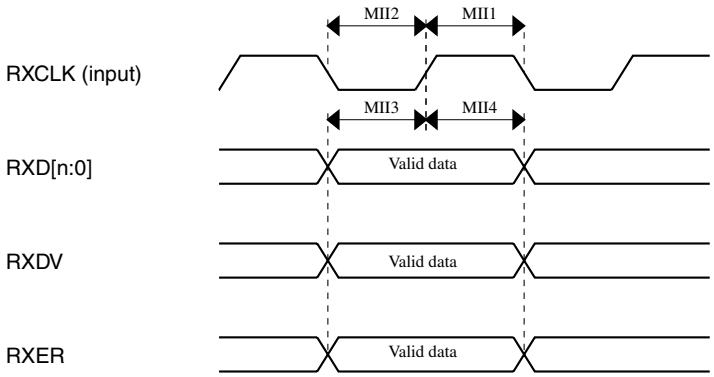


Figure 24. MII receive diagram

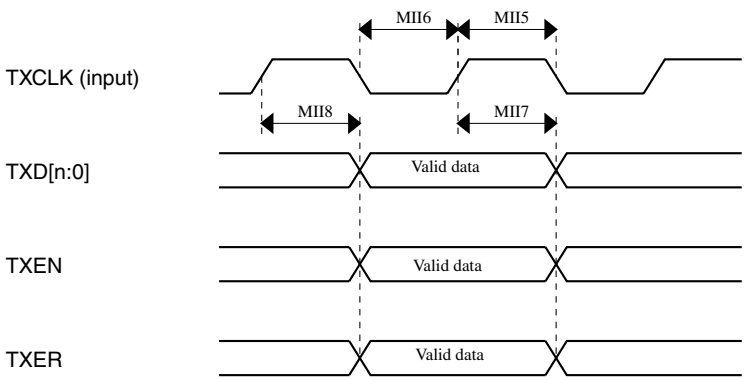


Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 33. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

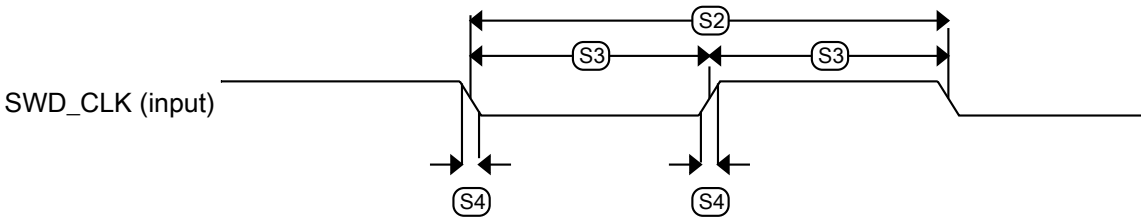


Figure 29. Serial wire clock input timing

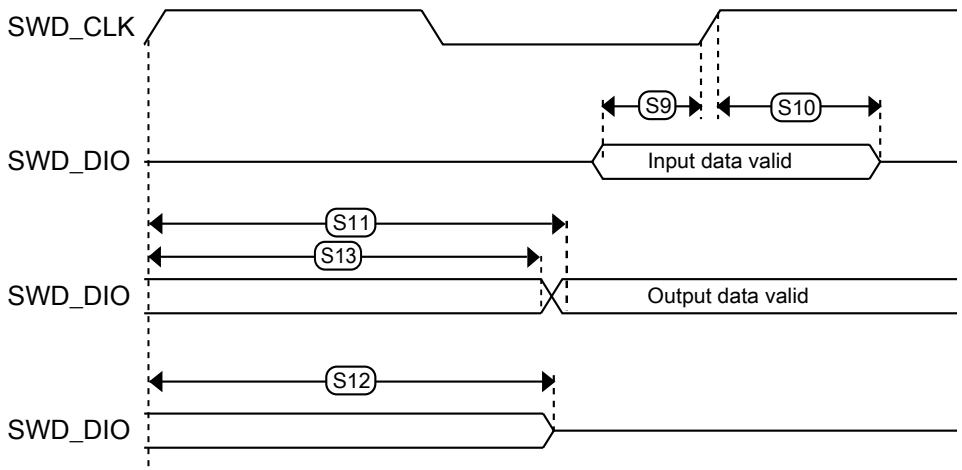


Figure 30. Serial wire data timing

6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. Trace specifications

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
—	Fsys	System frequency	80	48	40	112	80	4	MHz

Table continues on the next page...

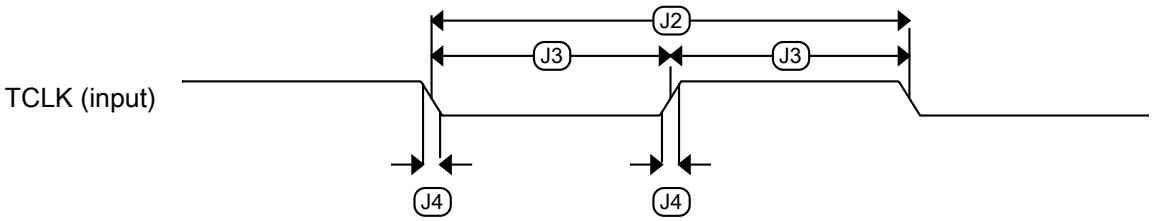


Figure 32. Test clock input timing

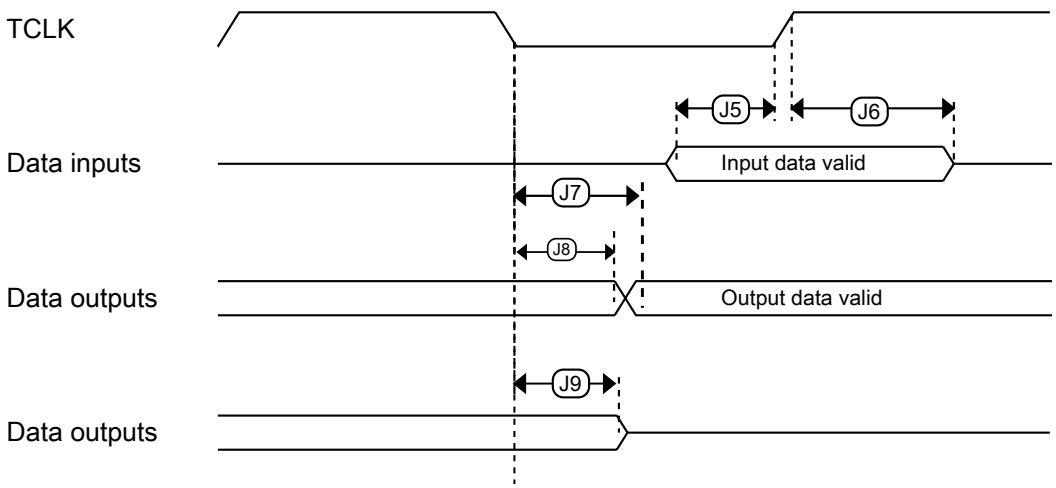


Figure 33. Boundary scan (JTAG) timing

Table 38. Thermal characteristics for the 64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Packages	Values					Unit
				S32K11x	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	64	TBD	13	12	11	NA	°C/W
			100	TBD	13	12	11	NA	°C/W
			144	TBD	NA	NA	12	9	°C/W
			176	TBD	NA	NA	NA	9	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	Ψ_{JT}	64	TBD	2	2	2	NA	°C/W
			100	TBD	2	2	2	NA	°C/W
			144	TBD	NA	NA	2	1	°C/W
			176	TBD	NA	NA	NA	1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number
32-pin QFN	SOT617-3 [1]
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W
100 MAP BGA	98ASA00802D
144-pin LQFP	98ASS23177W
176-pin LQFP	98ASS23479W

1. 5x5 mm package

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 40. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release

2	03 March 2017	• Updated descpition of QSPI and Clock interfaces in Key Features section
		• Updated figure: High-level architecture diagram for the S32K1xx family
		• Updated figure: S32K1xx product series comparison
		• Added note in section Determining valid orderable parts
		• Updated figure: Ordering information
		• In table: Absolute maximum ratings :
		  • Added footnote to I_{INJPAD_DC}
		  • Updated min and max value of I_{INJPAD_DC}
		  • Updated description, max and min values for I_{INJSUM}
		  • Updated $V_{IN\_TRANSIENT}$
		• In table: Voltage and current operating requirements :
		  • Renamed V_{SUP_OFF}
		  • Updated max value of V_{DD_OFF}
		  • Removed V_{INA} and V_{IN}
		  • Added V_{REFH} and V_{REFL}
		  • Updated footnote "Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V ...
		  • Removed I_{NJSUM_AF}
		• Updated footnotes in table Table 4
		• Updated section Power mode transition operating behaviors
		• In table: Power consumption
		  • Added footnote "With PMC_REGSC[CLKBIASDIS] ... "
		  • Updated conditions for VLPR
		  • Removed Idd/MHz for S32K144
		  • Updated numbers for S32K142 and S32K148
		  • Removed use case footnotes
		• In section Modes configuration :
		  • Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes _Master_configuration_sheet'
		• In table: DC electrical specifications at 3.3 V Range :
		  • Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		  • Added footnote to High drive port pins
		• In table: DC electrical specifications at 5.0 V Range :

Table continues on the next page...