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What is "Embedded - Microcontrollers"?

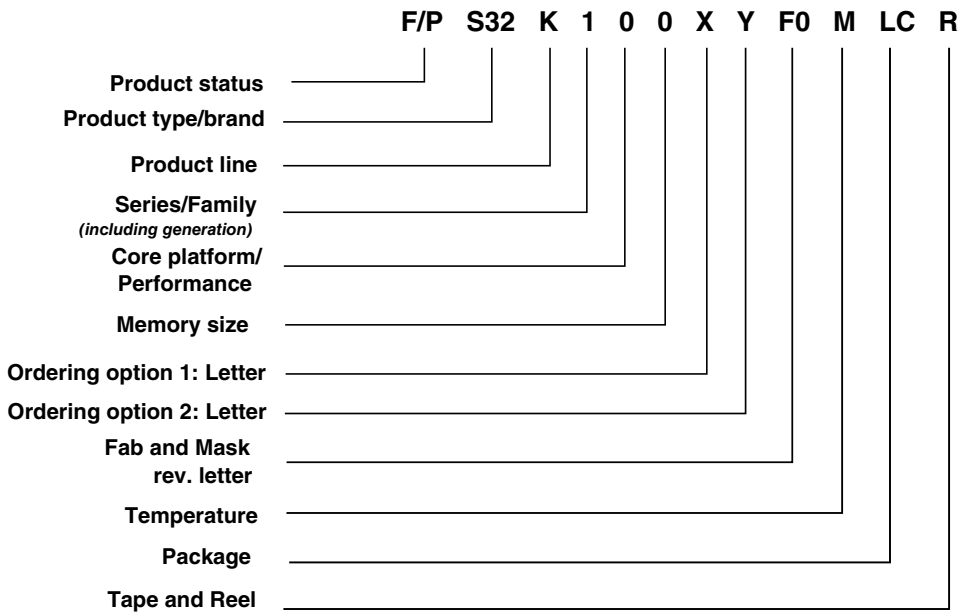
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mst0clht

- Reliability, safety and security
  - HW Security Engine (CSEc)
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - Cyclic Redundancy Check (CRC) module
  - 128-bit Unique Identification (ID) number
  - System Memory Protection Unit (System MPU)
- Timing and control
  - Up eight independent 16-bit FlexTimers (FTM) module, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- I/O and package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, MAPBGA-100, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

3.2 Ordering information



Product status
P: Prototype
F: Qualified ordering P/N

Product type/brand
S32: Automotive 32-bit MCU

Product line
K: ARM Cortex MCUs
M: MagniV/Mixed Signal

Series/Family
1: 1st product series
2: 2nd product series

Core platform/Performance
1: ARM Cortex M0+
4: ARM Cortex M4F

Memory size

	2	4	6	8
M0+	32 K	64 K	128 K	256 K
M4F	256 K	512 K	1 M	2 M

Ordering option
X: Speed
B: 48 MHz without DMA (only for S32K11x)
L: 48 MHz with DMA (only for S32K11x)
M: 64 MHz
H: 80 MHz
U: 112 MHz

Y: Optional feature
N: No/None
R: Max. RAM
F: CAN-FD and FlexIO including max. RAM
S: Security including max. RAM
A: CAN-FD, FlexIO, and Security including max. RAM
E: Ethernet and audio including max. RAM
J: CAN FD, FlexIO, Security, Ethernet and audio including max. RAM

Fab and Mask rev. letter
Fx: ATMC
Tx: GF
XX: Flex #

x0: 1st fab revision
x1: 2nd fab revision

Temperature
C: -40C to 85C
V: -40C to 105C
M: -40C to 125C

Package

Pins	LQFP	LQFP -EP	QFN	BGA
32	LC	-	FM	-
48	LF	KF	FT	-
64	LH	KH	-	-
100	LL	-	-	MH
144	LQ	-	-	-
176	LU	-	-	-

Tape and Reel
T: Trays and Tubes
R: Tape and Reel

Figure 4. Ordering information

5.6 AC electrical specifications at 5 V range

Table 12. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
Standard	NA	3.2	9.4	3.6	10.7	25
		5.4	15.7	5.1	17.4	50
		18.5	52.6	17.6	59.7	200
Strong	0	4.0	9.4	3.6	10.7	25
		5.8	15.7	5.1	17.4	50
		18.1	52.6	17.6	59.7	200
	1	1.6	4.6	1.5	5.0	25
		2.2	5.7	2.2	5.8	50
		5.6	14.6	5.0	15.4	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 13. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 14. Device clock specifications [1]

Symbol	Description	Min.	Max.	Unit
High Speed run mode[2]				
f_{SYS}	System and core clock	—	112	MHz
f_{BUS}	Bus clock	—	56	MHz
f_{FLASH}	Flash clock	—	28	MHz
Normal run mode (S32K11x series)				

Table continues on the next page...

6.3.1.1 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description[1]	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk64k}$ $t_{rd1blk512k}$	Read 1s Block execution time • 64 KB data flash • 512 KB program flash	— —	— —	0.5 1.8	ms ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	
t_{pgmchk}	Program Check execution time	—	—	95	µs	
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
$t_{ersblk64k}$ $t_{ersblk512k}$	Erase Flash Block execution time • 64 KB data flash • 512 KB program flash	— —	55 435	475 3700	ms ms	2
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	ms	
$t_{rd1allx}$	Read 1s All Blocks execution time	— — —	— — —	2.2 4.4 6.6	ms ms ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	500	4200	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	500	4200	ms	2
$t_{pgmpart32k}$ $t_{pgmpart64k}$	Program Partition for EEPROM execution time • 32 KB EEPROM backup • 64 KB EEPROM backup (Non-Interleaved DFlash) • 64 KB EEPROM backup (Interleaved DFlash)	— —	70 71 250	— —	ms ms ms	3, 4
$t_{setramff}$ $t_{setram32k}$ $t_{setram48k}$ $t_{setram64k}$	Set FlexRAM Function execution time: • Control Code 0xFF • 32 KB EEPROM backup • 48 KB EEPROM backup • 64 KB EEPROM backup	— — — —	70 0.8 1.0 1.3	— 1.2 1.5 1.9	µs ms ms ms	3, 4
$t_{eewr8b32k}$ $t_{eewr8b48k}$ $t_{eewr8b64k}$	Byte-write to FlexRAM execution time: • 32 KB EEPROM backup • 48 KB EEPROM backup • 64 KB EEPROM backup	— — —	385 430 475	1700 1850 2000	µs µs µs	3, 4
$t_{eewr16b32k}$ $t_{eewr16b48k}$	16-bit write to FlexRAM execution time: • 32 KB EEPROM backup	— —	385 430	1700 1850	µs µs	3, 4

Table continues on the next page...

Table 22. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	—	—	years	
$n_{nvmcycp}$	Cycling endurance	1 K	—	—	cycles	2, 1
When using FlexMemory feature: FlexRAM as Emulated EEPROM						
$t_{nvmretee}$	Data retention	5	—	—	years	
$n_{nvmwree16}$ $n_{nvmwree256}$	Write endurance • EEPROM backup to FlexRAM ratio = 16 • EEPROM backup to FlexRAM ratio = 256	100 K 1.6 M	— —	— —	writes writes	3, 4, 5

1. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
2. Cycling endurance is per DFlash or PFlash Sector.
3. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across standard temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
4. For usage of any other EEE driver other than the FlexMemory feature, the endurance specification will fall back to the specified endurance value of the D-Flash specification (1 K).
5. EEE calculator tool is available at NXP web site to help estimate the maximum write endurance achievable at specific EEPROM/FlexRAM ratio. The “In Spec” portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- For non-Quad mode of operation if external device doesn’t have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

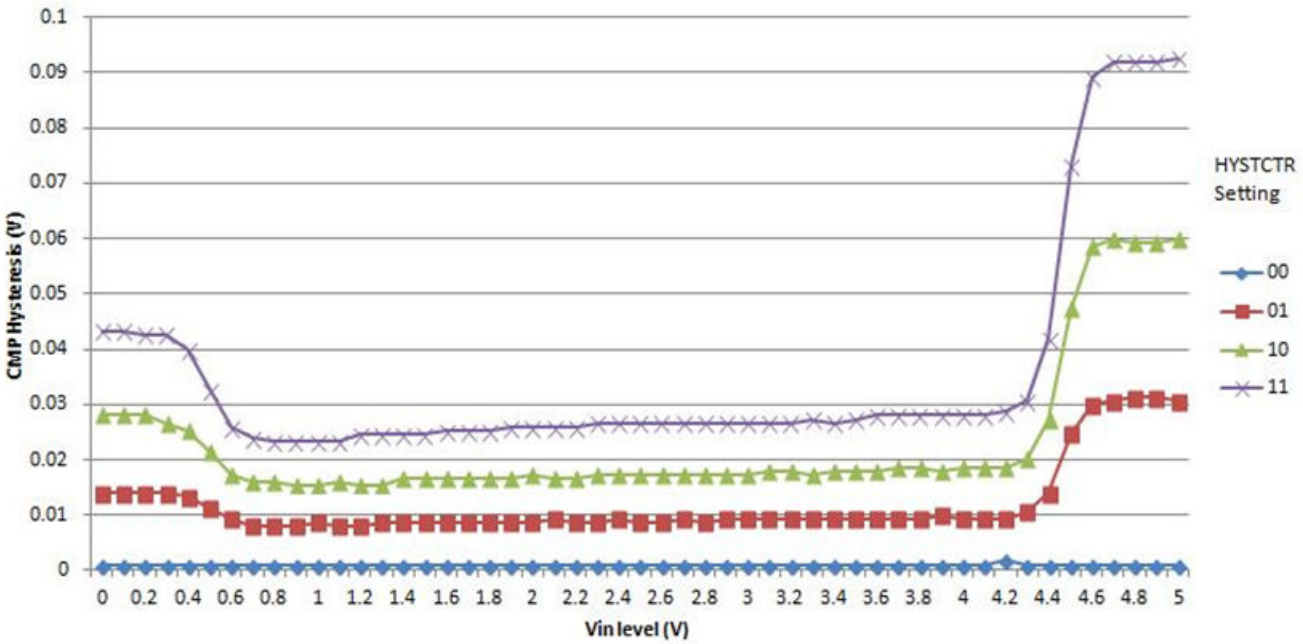


Figure 17. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 1)

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 29. LPSPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	f_{periph} [3, 4]	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	8	-	8	MHz
			Master	-	40	-	40	-	56	-	56	-	8	-	8	
			Master Loopback [5]	-	40	-	48	-	48	-	48	-	8	-	8	
			Master Loopback(Slow) [6]	-	48	-	48	-	48	-	48	-	8	-	8	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14	-	4	-	4	MHz
			Master	-	10	-	10	-	14	-	14	-	4	-	4	
			Master Loopback[5]	-	20	-	12	-	24	-	12	-	4	-	4	
			Master Loopback(slow) [6]	-	12	-	12	-	12	-	12	-	4	-	4	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	250	-	250	-	ns
			Master	100	-	100	-	72	-	72	-	250	-	250	-	
			Master Loopback[5]	50	-	83	-	42	-	83	-	250	-	250	-	
			Master Loopback(slow) [6]	83	-	83	-	83	-	83	-	250	-	250	-	
3	t_{Lead}[7]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns

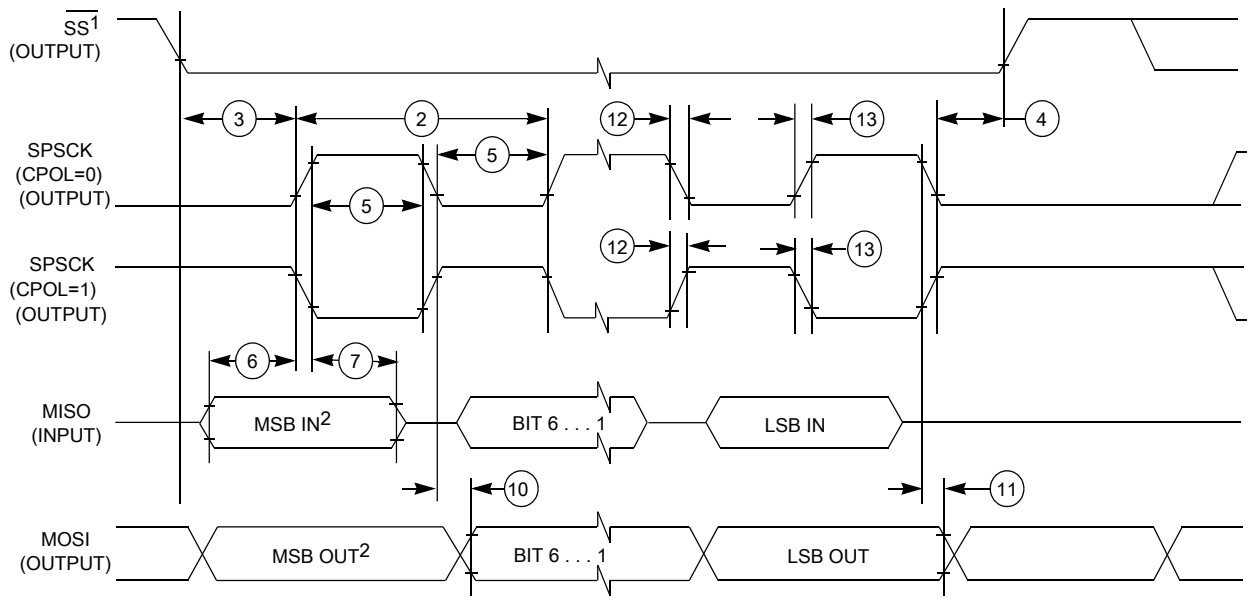
Table continues on the next page...

Table 29. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
			Master	(PCSSCK + 1)*t_{SPSCK} - 25	-	(PCSSCK + 1)*t_{SPSCK} - 25	-	(PCSSCK + 1)*t_{SPSCK} - 25	-	(PCSSCK + 1)*t_{SPSCK} - 25	-	(PCSSCK + 1)*t_{SPSCK} - 50	-	(PCSSCK + 1)*t_{SPSCK} - 50	-	
			Master Loopback[5]													
			Master Loopback(slow) [6]													
4	t_{Lag}[8]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS + 1)*t_{SPSCK} - 25	-	(SCKPCS + 1)*t_{SPSCK} - 25	-	(SCKPCS + 1)*t_{SPSCK} - 25	-	(SCKPCS + 1)*t_{SPSCK} - 25	-	(SCKPCS + 1)*t_{SPSCK} - 50	-	(SCKPCS + 1)*t_{SPSCK} - 50	-	
			Master Loopback[5]													
			Master Loopback(slow) [6]													

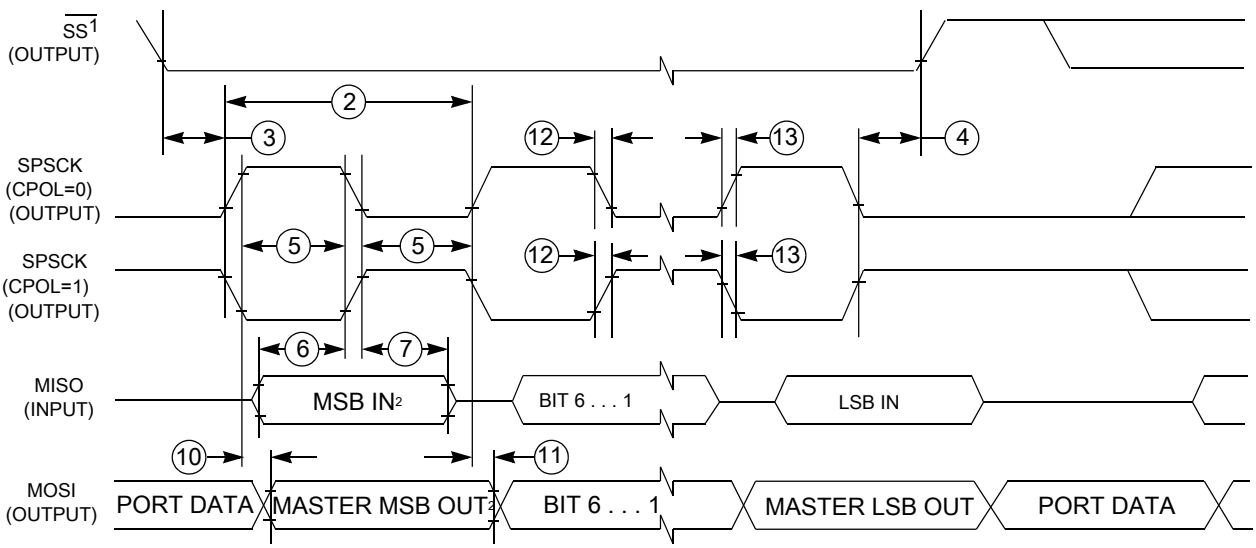
Table continues on the next page...

4. $t_{periph} = 1/f_{periph}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
7. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
8. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. LPSPI master mode timing (CPHA = 1)

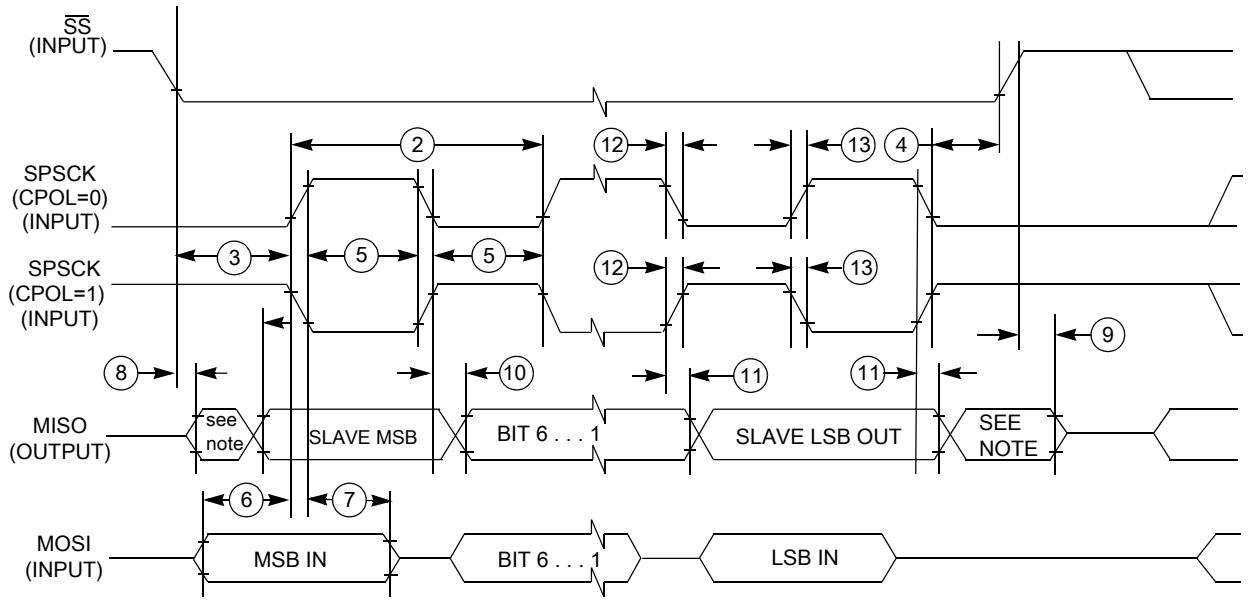


Figure 20. LPSPI slave mode timing (CPHA = 0)

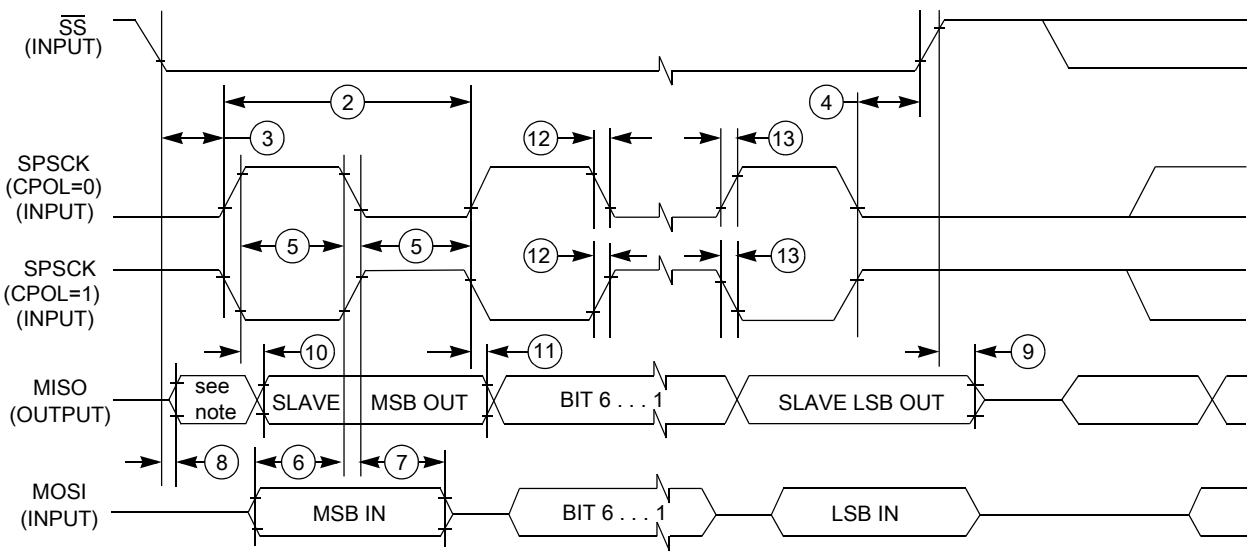


Figure 21. LPSPI slave mode timing (CPHA = 1)

6.5.3 LPI2C electrical specifications

See General AC specifications for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual.*

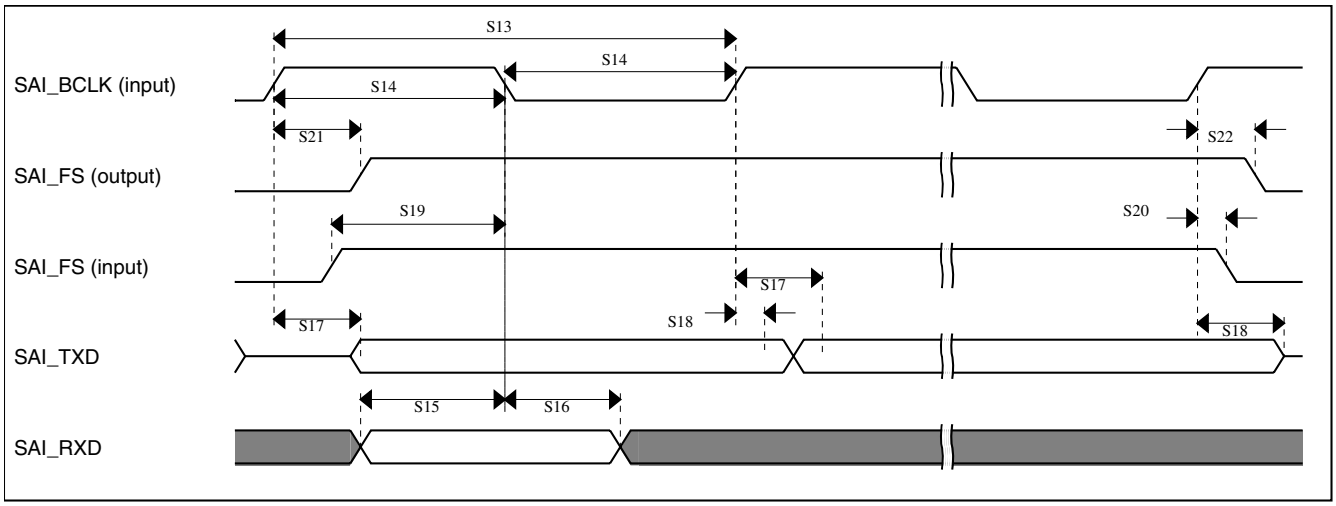


Figure 23. SAI Timing — Slave modes

6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 32. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

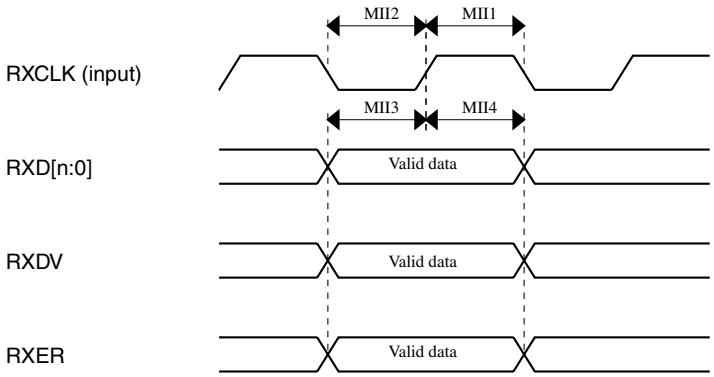


Figure 24. MII receive diagram

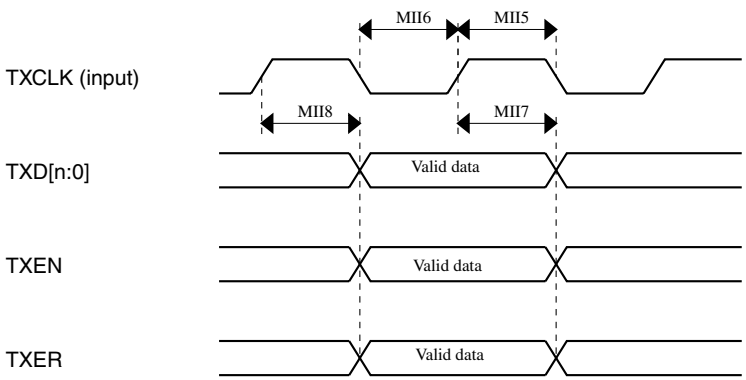


Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 33. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 35. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

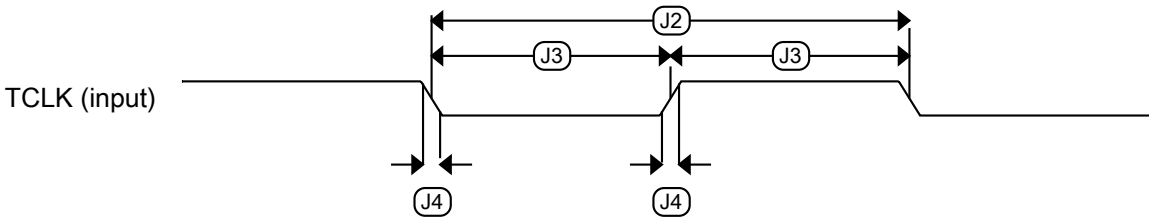


Figure 32. Test clock input timing

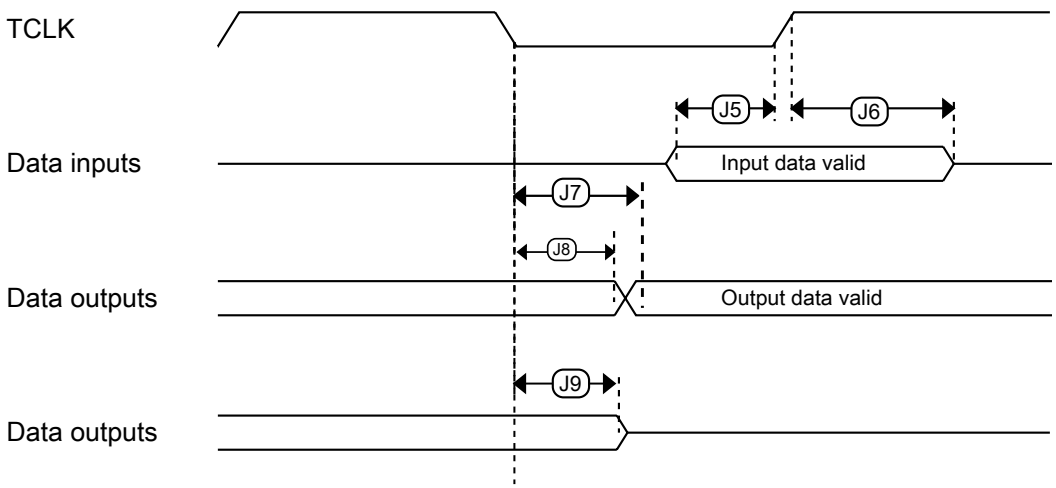


Figure 33. Boundary scan (JTAG) timing

Table 38. Thermal characteristics for the 64/100/144/176-pin LQFP package

Rating	Conditions	Symbol	Packages	Values					Unit
				S32K11x	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	64	TBD	61	61	59	NA	°C/W
			100	TBD	53	52	21	NA	°C/W
			144	TBD	NA	NA	51	44	°C/W
			176	TBD	NA	NA	NA	42	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Two layer board (1s1p)	$R_{\theta JA}$	64	TBD	45	45	44	NA	°C/W
			100	TBD	42	42	40	NA	°C/W
			144	TBD	NA	NA	44	37	°C/W
			176	TBD	NA	NA	NA	36	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	64	TBD	43	43	41	NA	°C/W
			100	TBD	40	40	39	NA	°C/W
			144	TBD	NA	NA	42	36	°C/W
			176	TBD	NA	NA	NA	35	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	64	TBD	49	49	48	NA	°C/W
			100	TBD	43	42	41	NA	°C/W
			144	TBD	NA	NA	42	36	°C/W
			176	TBD	NA	NA	NA	34	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1]	Two layer board (1s1p)	$R_{\theta JMA}$	64	TBD	38	38	37	NA	°C/W
			100	TBD	35	35	34	NA	°C/W
			144	TBD	NA	NA	37	31	°C/W
			176	TBD	NA	NA	NA	30	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	64	TBD	36	36	35	NA	°C/W
			100	TBD	34	34	33	NA	°C/W
			144	TBD	NA	NA	36	30	°C/W
			176	TBD	NA	NA	NA	29	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	64	TBD	25	25	23	NA	°C/W
			100	TBD	25	25	24	NA	°C/W
			144	TBD	NA	NA	30	24	°C/W
			176	TBD	NA	NA	NA	24	°C/W

Table continues on the next page...

Table 38. Thermal characteristics for the 64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Packages	Values					Unit
				S32K11x	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	64	TBD	13	12	11	NA	°C/W
			100	TBD	13	12	11	NA	°C/W
			144	TBD	NA	NA	12	9	°C/W
			176	TBD	NA	NA	NA	9	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	Ψ_{JT}	64	TBD	2	2	2	NA	°C/W
			100	TBD	2	2	2	NA	°C/W
			144	TBD	NA	NA	2	1	°C/W
			176	TBD	NA	NA	NA	1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 40. Revision History

Rev. No.	Date	Substantial Changes

		• Added footnotes V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		• Updated table: AC electrical specifications at 3.3 V range
		• Updated table: AC electrical specifications at 5 V range
		• In table: Standard input pin capacitance
		  • Added footnote to Normal run mode (S32K14x series)
		• Removed note from 1M ohms Feedback Resistor in figure Oscillator connections scheme
		• In table: External System Oscillator electrical specifications
		  • Updated typical of I_{DDOSC} Supply current — low-gain mode (low-power mode) (HGO=0) 1 for 4 and 8 MHz
		  • Removed rows for I_{lk_ext} EXTAL/XTAL impedence High-frequency, low-gain mode (low-power mode) and high-frequency, high-gain mode and V_{EXTAL}
		  • Updated Typ. of R_S low-gain mode
		  • Updated description of R_F, R_S, and V_{PP}
		  • Removed footnote from R_F Feedback resistor
		  • Updated footnote for C_1 C_2 and R_F
		• In table: Table 16
		  • Removed mention of high-frequency
		  • Added HGO 0, 1 information
		• In table: Fast internal RC Oscillator electrical specifications
		  • Updated F_{FIRC}
		  • Updated description of ΔF
		  • Updated typ and max values of T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Added footnotes to T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Updated naming convention of I_{DDFIRC} Supply current
		  • Added footnote to I_{DDFIRC} Supply current
		  • Added footnote to column Parameter
		• In table: Slow internal RC oscillator (SIRC) electrical specifications
		  • Removed V_{DD} Supply current in 2 MHz Mode
		  • Removed footnote and updated description of ΔF
		  • Updated footnote to F_{SIRC} and I_{DDSIRC}
		• In table: SPLL electrical specifications
		  • Added row for F_{SPLL_REF} PLL Reference
		  • Updated naming convention throughout the table
		  • Updated the max value of T_{SPLL_LOCK} Lock detector detection time
		• In table: Table 21
		  • Added footnotes:
		  • All command times assumes ...
		  • For all EEPROM Emulation terms ...
		  • 'First time' EERAM writes after a POR ...
		  • Removed footnote 'Assumes 25 MHz or ...'
		  • Updated Max of $t_{eewr32bers}$
		  • Added parameters $t_{quickwr}$ and $t_{quickwrClnup}$
		• In table: Table 22
		  • Removed Typ. values for all parameters
		  • Removed footnote 'Typical values represent ... '
		  • Added footnote 'Any other EEE driver usage ... '
		• Updated QuadSPI AC specifications
		• Removed topic: Reliability, Safety and Security modules
		• In table: 12-bit ADC operating conditions
		  • Updated V_{DDA}

Table continues on the next page...

Table 40. Revision History

Rev. No.	Date	Substantial Changes
		• Updated note 'All the limits defined ... ' • Updated parameter '$I_{INJPAD\_DC\_ABS}$', 'V_{IN_DC}', $I_{INJSUM\_DC\_ABS}$. • In Table 2, • Updated parameter $I_{INJPAD\_DC\_OP}$ and $I_{INJSUM\_DC\_OP}$. • In Table 5, updated TBDs for V_{LVR_HYST}, V_{LVD_HYST}, and $_{VLVW\_HYST}$ • In Table 6, • Added VLPR → VLPS • Added VLPS → VLPR • Updated TBDs for VLPS → Asynchronous DMA Wakeup, STOP1 → Asynchronous DMA Wakeup, and STOP2 → Asynchronous DMA Wakeup • In Table 7, updated the specifications for S32K144. • Updated the attachment *S32K1xx_Power_Modes _Configuration.xlsx*. • In Table 13, removed C_{IN_A}. • In Table 15, • Updated specificatins for g_{mXOSC}. • Removed I_{DDOSC} • In Table 17, • Added parameter ΔF125. • Removed I_{DDFIRC} • In Table 18, • Added parameter ΔF125. • Removed I_{DDSIRC} • In Table 19, removed I_{LPO} • Updated section: Flash memory module (FTFC) electrical specifications • In section: 12-bit ADC operating conditions, • Updated TBDs for I_{DDA_ADC} and TUE in Table 25 • Updated TBDs for I_{DDA_ADC} and TUE in Table 26 • In section: QuadSPI AC specifications, updated figure 'QuadSPI output timing (HyperRAM mode) diagram'. • In section: 12-bit ADC operating conditions, updated Table 24. • In section: CMP with 8-bit DAC electrical specifications, added note 'For comparator IN signals adjacent ... ' • In table: Table 29, minor update in footnote 6. • In table: Table 38, updated specifications for S32K146.

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Document Number S32K1XX
Revision 4, 06/2017