**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

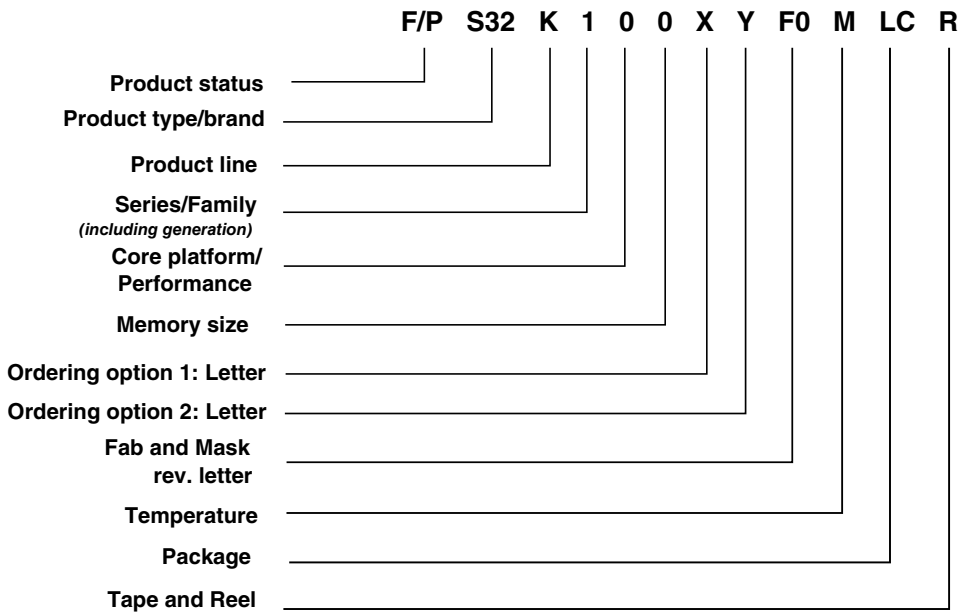
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 112MHz |
| Connectivity | CANbus, FlexIO, I²C, LINbus, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 89 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x12b SAR; D/A1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144uft0cllt |

- Reliability, safety and security
  - HW Security Engine (CSEc)
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - Cyclic Redundancy Check (CRC) module
  - 128-bit Unique Identification (ID) number
  - System Memory Protection Unit (System MPU)
- Timing and control
  - Up eight independent 16-bit FlexTimers (FTM) module, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- I/O and package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, MAPBGA-100, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

# Table of Contents

## 3.2 Ordering information




**Product status**
P: Prototype
F: Qualified ordering P/N

**Product type/brand**
S32: Automotive 32-bit MCU

**Product line**
K: ARM Cortex MCUs
M: MagniV/Mixed Signal

**Series/Family**
1: 1st product series
2: 2nd product series

**Core platform/Performance**
1: ARM Cortex M0+
4: ARM Cortex M4F

**Memory size**

| | 2 | 4 | 6 | 8 |
|---|---|---|---|---|
| M0+ | 32 K | 64 K | 128 K | 256 K |
| M4F | 256 K | 512 K | 1 M | 2 M |

**Ordering option**
X: Speed
B: 48 MHz without DMA (only for S32K11x)
L: 48 MHz with DMA (only for S32K11x)
M: 64 MHz
H: 80 MHz
U: 112 MHz

Y: Optional feature
N: No/None
R: Max. RAM
F: CAN-FD and FlexIO including max. RAM
S: Security including max. RAM
A: CAN-FD, FlexIO, and Security including max. RAM
E: Ethernet and audio including max. RAM
J: CAN FD, FlexIO, Security, Ethernet and audio including max. RAM

**Fab and Mask rev. letter**
Fx: ATMC
Tx: GF
XX: Flex #

x0: 1st fab revision
x1: 2nd fab revision

**Temperature**
C: -40C to 85C
V: -40C to 105C
M: -40C to 125C

**Package**

| Pins | LQFP | LQFP -EP | QFN | BGA |
|---|---|---|---|---|
| 32 | LC | - | FM | - |
| 48 | LF | KF | FT | - |
| 64 | LH | KH | - | - |
| 100 | LL | - | - | MH |
| 144 | LQ | - | - | - |
| 176 | LU | - | - | - |

**Tape and Reel**
T: Trays and Tubes
R: Tape and Reel

**Figure 4. Ordering information**

## Table 7. Power consumption (Typicals unless stated otherwise) 1

| | Ambient Temperature (°C) | | VLPS (µA)[2, 3] | | VLPR (mA) | | STOP1 (mA) | STOP2 (mA) | RUN@48 MHz (mA) | | RUN@64 MHz (mA) | | RUN@80 MHz (mA) | | HSRUN@112 MHz (mA) [4] | | Idd/MHz (µA/MHz)[5] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Peripherals disabled [6] | Peripherals enabled | Peripherals disabled | Peripherals enabled | | | Peripherals disabled | Peripherals enabled | Peripherals disabled | Peripherals enabled | Peripherals disabled | Peripherals enabled | Peripherals disabled | Peripherals enabled | |
| **S32K116** | 25 | Typ | 26 | 38 | 1.9 | 2.5 | 7 | 12 | TBD | TBD | NA | | | | | | TBD |
| | 105 | Typ | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | | | | | | | TBD |
| | | Max | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | | | | | | | TBD |
| | 125 | Max | TBD | TBD | TBD | TBD | TBD | TBD | TBD | 40 | | | | | | | TBD |
| **S32K118** | 25 | Typ | 26 | 38 | 1.9 | 2.5 | 7 | 12 | TBD | TBD | NA | | | | | | TBD |
| | 105 | Typ | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | | | | | | | TBD |
| | | Max | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | | | | | | | TBD |
| | 125 | Max | TBD | TBD | TBD | TBD | TBD | TBD | TBD | 42 | | | | | | | TBD |
| **S32K142** | 25 | Typ | 29 | 42 | 1.9 | 2.5 | 10 | 15 | TBD | TBD | NA | | TBD | TBD | TBD | TBD | TBD |
| | 105 | Typ | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | | | 48 | 57 | 65 | 75 | TBD |
| | | Max | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | | | TBD | TBD | 85 | 90 | TBD |
| | 125 | Max | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | | | 60 | 65 | NA | | TBD |
| **S32K144** | 25 | Typ | 29.8 | 39.1 | 1.48 | 1.50 | 7 | 7.7 | 19.7 | 26.9 | 25.1 | 33.3 | 30.2 | 39.6 | 43.3 | 55.6 | 378 |

*Table continues on the next page...*

**Table 14. Device clock specifications 1 (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $f_{SYS}$ | System and core clock | — | 48 | MHz |
| $f_{BUS}$ | Bus clock | — | 24 | MHz |
| $f_{FLASH}$ | Flash clock | — | 24 | MHz |
| Normal run mode (S32K14x series) [3] | | | | |
| $f_{SYS}$ | System and core clock | — | 80 | MHz |
| $f_{BUS}$ | Bus clock | — | 40 | MHz |
| $f_{FLASH}$ | Flash clock | — | 26.67 | MHz |
| VLPR mode[4] | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz |
| $f_{BUS}$ | Bus clock | — | 4 | MHz |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz |

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

# 6 Peripheral operating requirements and behaviors

## 6.1 System modules

There are no electrical specifications necessary for the device's system modules.

## 6.2 Clock interface modules

### 6.2.1 External System Oscillator electrical specifications

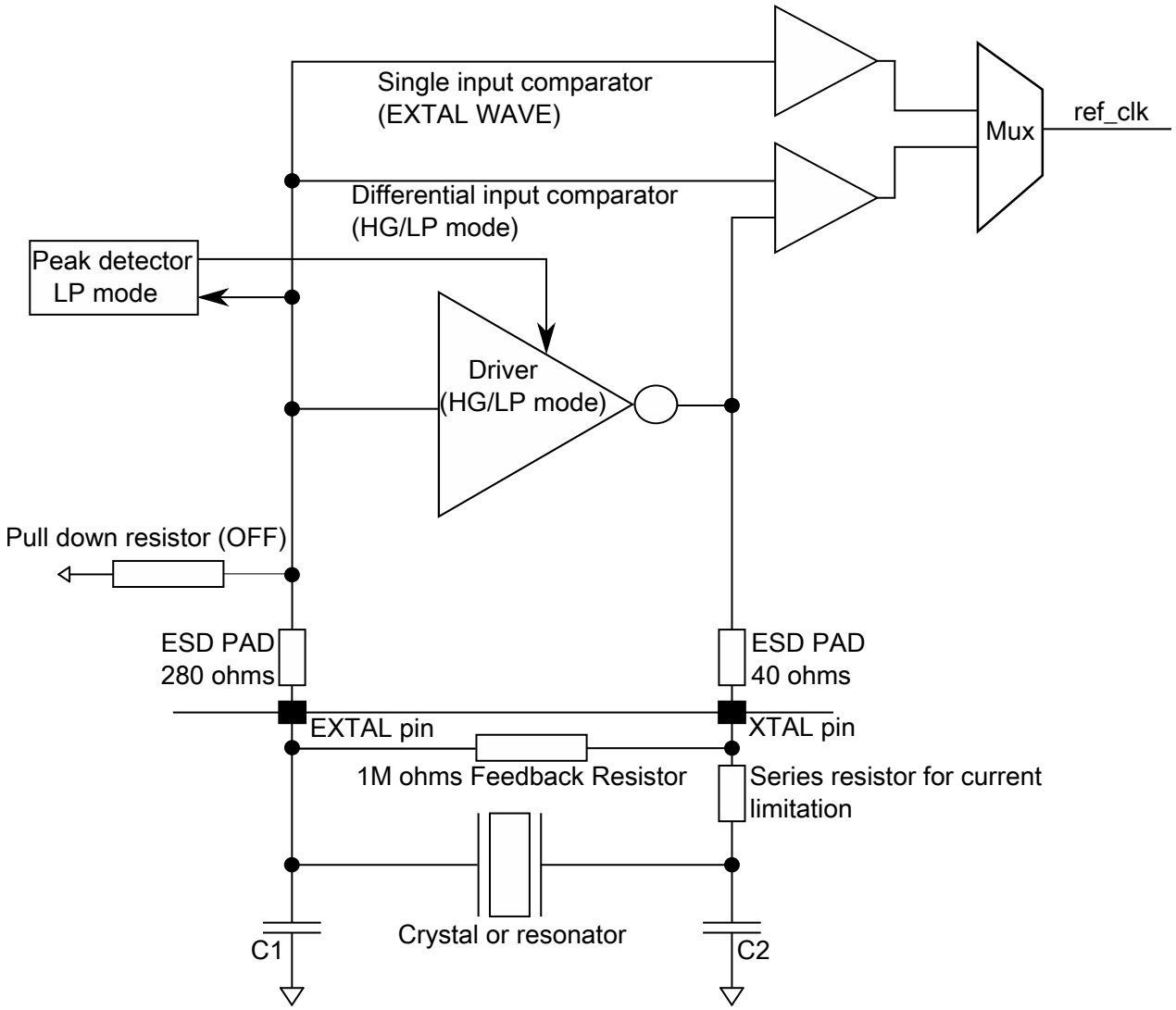



**Figure 8. Oscillator connections scheme**

**Table 15. External System Oscillator electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $g_{mXOSC}$ | Crystal oscillator transconductance | | | | | |
| | 4-8 MHz | 2.2 | — | 13.7 | mA/V | |
| | 8-40 MHz | 16 | — | 47 | mA/V | |
| $V_{IL}$ | Input low voltage — EXTAL pin in external clock mode | $V_{SS}$ | — | 0.35 * $V_{DD}$ | V | |
| $V_{IH}$ | Input high voltage — EXTAL pin in external clock mode | 0.7 * $V_{DD}$ | — | $V_{DD}$ | V | |
| $C_1$ | EXTAL load capacitance | — | — | — | | 1 |
| $C_2$ | XTAL load capacitance | — | — | — | | 1 |
| $R_F$ | Feedback resistor | | | | | 2 |
| | Low-gain mode (HGO=0) | — | — | — | MΩ | |

*Table continues on the next page...*

**Table 15. External System Oscillator electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | High-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor | | | | | |
| | Low-gain mode (HGO=0) | — | 0 | — | kΩ | |
| | High-gain mode (HGO=1) | — | 0 | — | kΩ | |
| $V_{pp}$ | Peak-to-peak amplitude of oscillation (oscillator mode) | | | | | 3 |
| | Low-gain mode (HGO=0) | — | 1.0 | — | V | |
| | High-gain mode (HGO=1) | — | 3.3 | — | V | |

1. Crystal oscillator circuit provides stable oscillations when $g_{mXOSC}$ > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - $g_{mXOSC}$ is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - $C_0$ is the shunt capacitance of the external crystal
   - $C_L$ is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - $C_s$ is stray or parasitic capacitance on the pin due to any PCB traces
   - $C_1$, $C_2$ external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal $R_F$ will be selected and external $R_F$ should not be attached.
   - When high-gain is selected, external $R_F$ (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

## 6.2.2 External System Oscillator frequency specifications

**Table 16. External System Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_hi}$ | Oscillator crystal or resonator frequency | 4 | — | 40 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal Start-up Time | | | | | |
| | 8 MHz low-gain mode (HGO=0) | — | 1.5 | — | ms | 1 |
| | 8 MHz high-gain mode (HGO=1) | — | 2.5 | — | | |
| | 40 MHz low-gain mode (HGO=0) | — | 2 | — | | |
| | 40 MHz high-gain mode (HGO=1) | — | 2 | — | | |

1. Proper PC board layout procedures must be followed to achieve specifications.

### 6.2.4 Low Power Oscillator (LPO) electrical specifications

**Table 19. Low Power Oscillator (LPO) electrical specifications**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{LPO}$ | Internal low power oscillator frequency | 113 | 128 | 139 | kHz |
| $T_{startup}$ | Startup Time | — | — | 20 | µs |

### 6.2.5 SPLL electrical specifications

**Table 20. SPLL electrical specifications**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{SPLL\_REF}$[1] | PLL Reference Frequency Range | 8 | — | 16 | MHz |
| $F_{SPLL\_Input}$[2] | PLL Input Frequency | 8 | — | 40 | MHz |
| $F_{VCO\_CLK}$ | VCO output frequency | 180 | — | 320 | MHz |
| $F_{SPLL\_CLK}$ | PLL output frequency | 90 | — | 160 | MHz |
| $J_{CYC\_SPLL}$ | PLL Period Jitter (RMS)[3] | | | | |
| | at $F_{VCO\_CLK}$ 180 MHz | — | 120 | — | ps |
| | at $F_{VCO\_CLK}$ 320 MHz | — | 75 | — | ps |
| $J_{ACC\_SPLL}$ | PLL accumulated jitter over 1µs (RMS)[3] | | | | |
| | at $F_{VCO\_CLK}$ 180 MHz | — | 1350 | — | ps |
| | at $F_{VCO\_CLK}$ 320 MHz | — | 600 | — | ps |
| $D_{UNL}$ | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % |
| $T_{SPLL\_LOCK}$ | Lock detector detection time[4] | — | — | $150 \times 10^{-6} + 1075(1/F_{SPLL\_REF})$ | s |

1. $F_{SPLL\_REF}$ is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLLCFG register of Reference Manual.
2. $F_{SPLL\_Input}$ is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

## 6.3 Memory and memory interfaces

### 6.3.1 Flash memory module (FTFC) electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 6.3.1.1 Flash timing specifications — commands

**Table 21. Flash command timing specifications**

| Symbol | Description[1] | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{rd1blk64k}$<br>$t_{rd1blk512k}$ | Read 1s Block execution time<br>• 64 KB data flash<br>• 512 KB program flash | —<br>— | —<br>— | 0.5<br>1.8 | ms<br>ms | |
| $t_{rd1sec2k}$ | Read 1s Section execution time (2 KB flash) | — | — | 75 | µs | |
| $t_{rd1sec4k}$ | Read 1s Section execution time (4 KB flash) | — | — | 100 | µs | |
| $t_{pgmchk}$ | Program Check execution time | — | — | 95 | µs | |
| $t_{pgm8}$ | Program Phrase execution time | — | 90 | 150 | µs | |
| $t_{ersblk64k}$<br>$t_{ersblk512k}$ | Erase Flash Block execution time<br>• 64 KB data flash<br>• 512 KB program flash | —<br>— | 55<br>435 | 475<br>3700 | ms<br>ms | 2 |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 15 | 115 | ms | 2 |
| $t_{pgmsec1k}$ | Program Section execution time (1KB flash) | — | 5 | — | ms | |
| $t_{rd1allx}$ | Read 1s All Blocks execution time | —<br>—<br>— | —<br>—<br>— | 2.2<br>4.4<br>6.6 | ms<br>ms<br>ms | |
| $t_{rdonce}$ | Read Once execution time | — | — | 30 | µs | |
| $t_{pgmonce}$ | Program Once execution time | — | 90 | — | µs | |
| $t_{ersall}$ | Erase All Blocks execution time | — | 500 | 4200 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 35 | µs | |
| $t_{ersallu}$ | Erase All Blocks Unsecure execution time | — | 500 | 4200 | ms | 2 |
| $t_{pgmpart32k}$<br>$t_{pgmpart64k}$ | Program Partition for EEPROM execution time<br>• 32 KB EEPROM backup<br>• 64 KB EEPROM backup (Non-Interleaved DFlash)<br>• 64 KB EEPROM backup (Interleaved DFlash) | —<br>— | 70<br>71<br>250 | —<br>— | ms<br>ms<br>ms | 3, 4 |
| $t_{setramff}$<br>$t_{setram32k}$<br>$t_{setram48k}$<br>$t_{setram64k}$ | Set FlexRAM Function execution time:<br>• Control Code 0xFF<br>• 32 KB EEPROM backup<br>• 48 KB EEPROM backup<br>• 64 KB EEPROM backup | —<br>—<br>—<br>— | 70<br>0.8<br>1.0<br>1.3 | —<br>1.2<br>1.5<br>1.9 | µs<br>ms<br>ms<br>ms | 3, 4 |
| $t_{eewr8b32k}$<br>$t_{eewr8b48k}$<br>$t_{eewr8b64k}$ | Byte-write to FlexRAM execution time:<br>• 32 KB EEPROM backup<br>• 48 KB EEPROM backup<br>• 64 KB EEPROM backup | —<br>—<br>— | 385<br>430<br>475 | 1700<br>1850<br>2000 | µs<br>µs<br>µs | 3, 4 |
| $t_{eewr16b32k}$<br>$t_{eewr16b48k}$ | 16-bit write to FlexRAM execution time:<br>• 32 KB EEPROM backup | —<br>— | 385<br>430 | 1700<br>1850 | µs<br>µs | 3, 4 |

*Table continues on the next page...*

**Table 22. NVM reliability specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | — | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 1 K | — | — | cycles | 2, 1 |
| When using FlexMemory feature: FlexRAM as Emulated EEPROM | | | | | | |
| $t_{nvmretee}$ | Data retention | 5 | — | — | years | |
| $n_{nvmwree16}$<br>$n_{nvmwree256}$ | Write endurance<br>• EEPROM backup to FlexRAM ratio = 16<br>• EEPROM backup to FlexRAM ratio = 256 | 100 K<br>1.6 M | —<br>— | —<br>— | writes<br>writes | 3, 4, 5 |

1. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
2. Cycling endurance is per DFlash or PFlash Sector.
3. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across standard temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
4. For usage of any other EEE driver other than the FlexMemory feature, the endurance specification will fall back to the specified endurance value of the D-Flash specification (1 K).
5. EEE calculator tool is available at NXP web site to help estimate the maximum write endurance achievable at specific EEPROM/FlexRAM ratio. The “In Spec” portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

## 6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN ), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- For non-Quad mode of operation if external device doesn’t have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

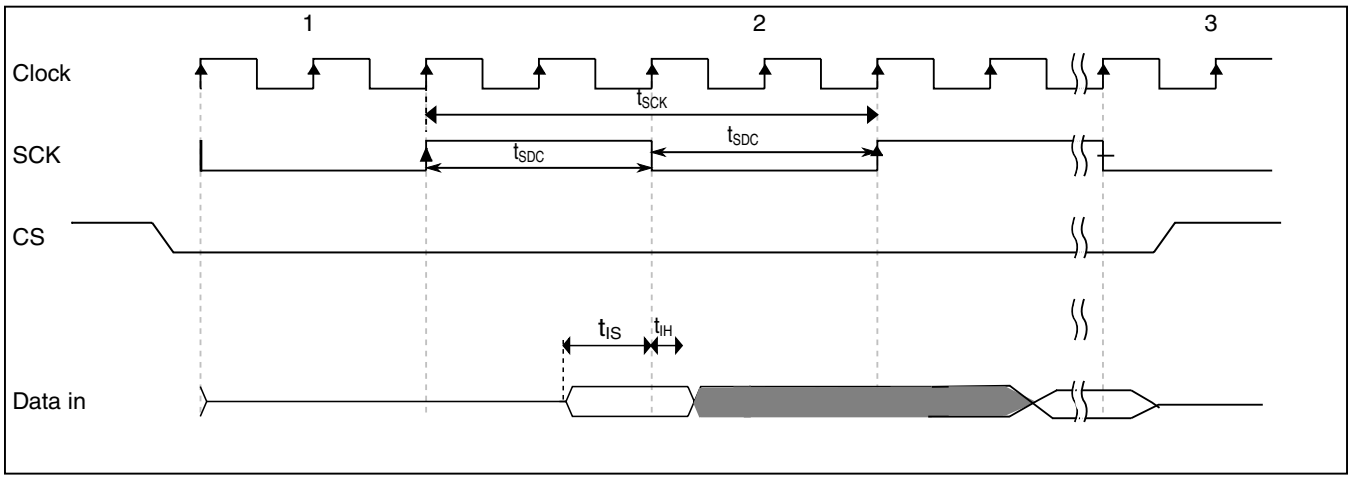



**Figure 9. QuadSPI input timing (SDR mode) diagram**

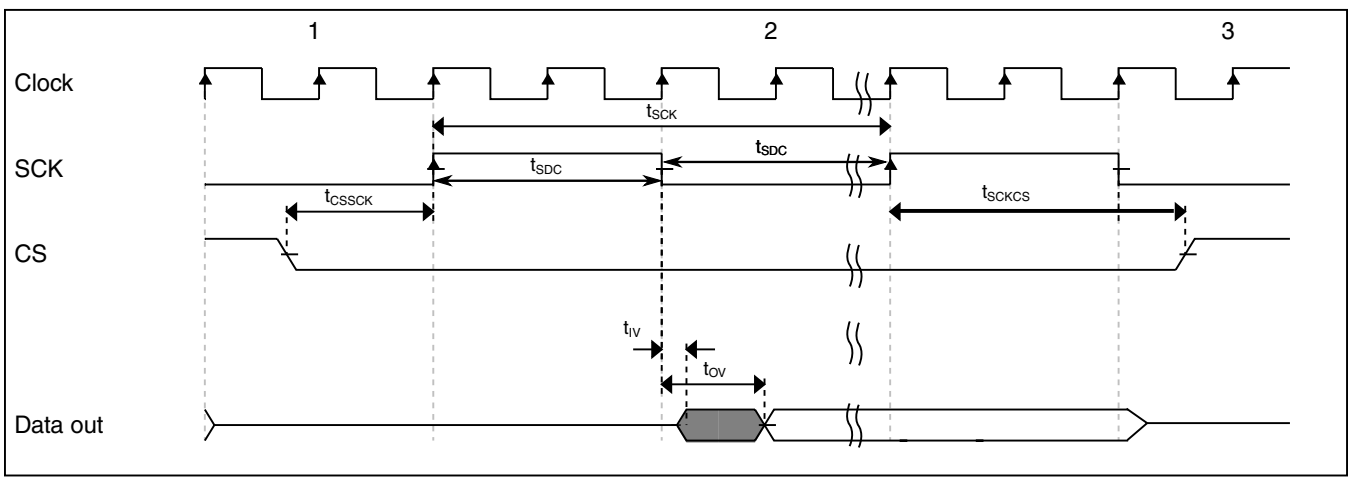



**Figure 10. QuadSPI output timing (SDR mode) diagram**

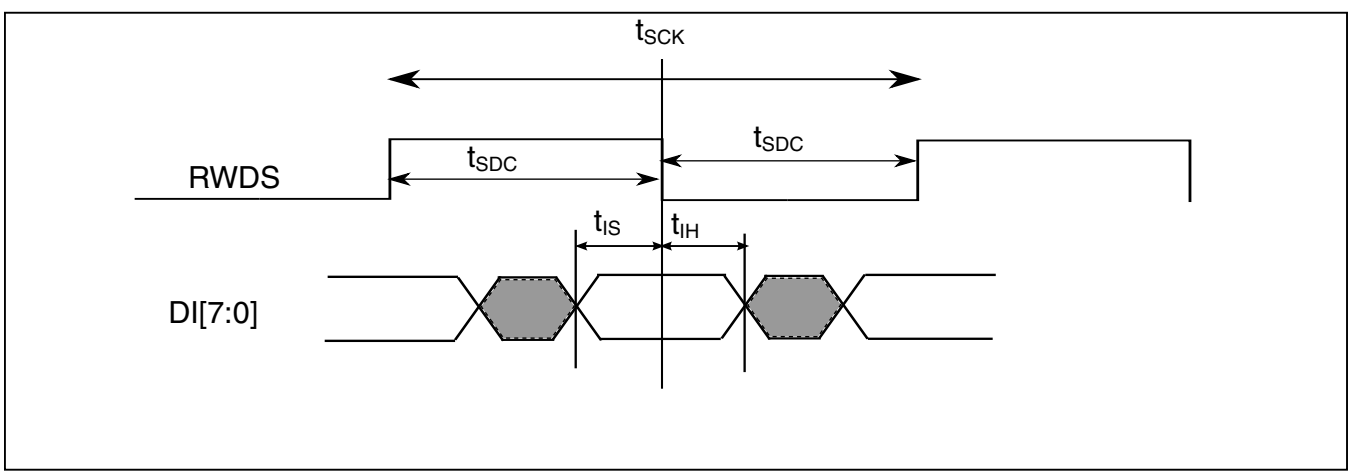



**Figure 11. QuadSPI input timing (HyperRAM mode) diagram**

### 6.4.1.2 12-bit ADC electrical characteristics

**NOTE**

ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.

**Table 25. 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SS}$)**

| Symbol | Description | Conditions [1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 2.7 | — | 3 | V | |
| $I_{DDA\_ADC}$ | Supply current per ADC | | — | 0.6 | 1.5 | mA | 3 |
| SMPLTS | Sample Time | | 275 | — | Refer to the *Reference Manual* | ns | |
| TUE[4] | Total unadjusted error | | — | ±4 | ±8 | LSB[5] | 6, 7, 8, 9 |
| DNL | Differential non-linearity | | — | ±1.0 | — | LSB[5] | 6, 7, 8, 9 |
| INL | Integral non-linearity | | — | ±2.0 | — | LSB[5] | 6, 7, 8, 9 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$=$V_{DDA}$=$V_{DD}$, with the calibration frequency set to half the ADC clock frequency.
2. Typical values assume $V_{DDA}$ = 3 V, Temp = 25 °C, $f_{ADCK}$ = 40 MHz, $R_{AS}$=20 Ω, and $C_{AS}$=10 nF, 100 LQFP package unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/$2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to $V_{DD}$/$V_{SS}$ or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

**Table 26. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SS}$)**

| Symbol | Description | Conditions [1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 3 | — | 5.5 | V | |
| $I_{DDA\_ADC}$ | Supply current per ADC | | — | 1 | 2.1 | mA | 3 |
| SMPLTS | Sample Time | | 275 | — | Refer to the *Reference Manual* | ns | |

*Table continues on the next page...*

**Table 26. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SS}$) (continued)**

| Symbol | Description | Conditions [1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| TUE[4] | Total unadjusted error | | — | ±4 | ±8 | LSB[5] | 6, 7, 8, 9 |
| DNL | Differential non-linearity | | — | ±0.7 | — | LSB[5] | 6, 7, 8, 9 |
| INL | Integral non-linearity | | — | ±1.0 | — | LSB[5] | 6, 7, 8, 9 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$=$V_{DDA}$=$V_{DD}$, with the calibration frequency set to half the ADC clock frequency.
2. Typical values assume $V_{DDA}$ = 5.0 V, Temp = 25 °C, $f_{ADCK}$ = 40 MHz, $R_{AS}$=20 Ω, and $C_{AS}$=10 nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/$2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to $V_{DD}$/$V_{SS}$ or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

**NOTE**

When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

| Pin name | TGATE purpose |
|---|---|
| PTE8 | CMP0_IN3 |
| PTC3 | ADC0_SE11/CMP0_IN4 |
| PTC2 | ADC0_SE10/CMP0_IN5 |
| PTD7 | CMP0_IN6 |
| PTD6 | CMP0_IN7 |
| PTD28 | ADC1_SE22 |
| PTD27 | ADC1_SE21 |

## 6.4.2 CMP with 8-bit DAC electrical specifications

**Table 28. Comparator with 8-bit DAC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DDHS}$ | Supply current, High-speed mode[1] | | | | µA |
| | -40 - 125 °C | — | 230 | 300 | |
| $I_{DDLS}$ | Supply current, Low-speed mode[1] | | | | µA |
| | -40 - 105 °C | — | 5 | 10 | |
| | -40 - 125 °C | | 5 | 13 | |

*Table continues on the next page...*

## Table 29. LPSPI electrical specifications[1] (continued)

| Num | Symbol | Description | Conditions | Run Mode[2] | | | | HSRUN Mode[2] | | | | VLPR Mode | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | |
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 5 | $t_{WSPSCK}$ | Clock(SPSCK) high or low time (SPSCK duty cycle) | Slave | $t_{SPSCK}/2 - 3$ | $t_{SPSCK}/2 + 3$ | $t_{SPSCK}/2 - 3$ | $t_{SPSCK}/2 + 3$ | $t_{SPSCK}/2 - 3$ | $t_{SPSCK}/2 + 3$ | $t_{SPSCK}/2 - 3$ | $t_{SPSCK}/2 + 3$ | $t_{SPSCK}/2 - 5$ | $t_{SPSCK}/2 + 5$ | $t_{SPSCK}/2 - 5$ | $t_{SPSCK}/2 + 5$ | ns |
| | | | Master | | | | | | | | | | | | | |
| | | | Master Loopback[5] | | | | | | | | | | | | | |
| | | | Master Loopback(slow) [6] | | | | | | | | | | | | | |
| 6 | $t_{SU}$ | Data setup time(inputs) | Slave | 3 | - | 5 | - | 3 | - | 5 | - | 18 | - | 18 | - | ns |
| | | | Master | 29 | - | 38 | - | 26 | - | 37 | - | 72 | - | 78 | - | |
| | | | Master Loopback[5] | 7 | - | 8 | - | 5 | - | 7 | - | 20 | - | 20 | - | |
| | | | Master Loopback(slow) [6] | 8 | - | 10 | - | 7 | - | 9 | - | 20 | - | 20 | - | |
| 7 | $t_{HI}$ | Data hold time(inputs) | Slave | 3 | - | 3 | - | 3 | - | 3 | - | 14 | - | 14 | - | ns |
| | | | Master | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | |
| | | | Master Loopback[5] | 3 | - | 3 | - | 2 | - | 3 | - | 11 | - | 11 | - | |
| | | | Master Loopback(slow) [6] | 3 | - | 3 | - | 3 | - | 3 | - | 12 | - | 12 | - | |
| 8 | $t_a$ | Slave access time | Slave | - | 50 | - | 50 | - | 50 | - | 50 | - | 100 | - | 100 | ns |
| 9 | $t_{dis}$ | Slave MISO (SOUT) disable time | Slave | - | 50 | - | 50 | - | 50 | - | 50 | - | 100 | - | 100 | ns |

*Table continues on the next page...*

## Table 29. LPSPI electrical specifications[1] (continued)

| Num | Symbol | Description | Conditions | Run Mode[2] | | | | HSRUN Mode[2] | | | | VLPR Mode | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | |
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 10 | $t_v$ | Data valid (after SPSCK edge) | Slave | - | 30 | - | 39 | - | 26 | - | 36 | - | 92 | - | 96 | ns |
| | | | Master | - | 12 | - | 16 | - | 11 | - | 15 | - | 47 | - | 48 | |
| | | | Master Loopback[5] | - | 12 | - | 16 | - | 11 | - | 15 | - | 47 | - | 48 | |
| | | | Master Loopback(slow) [6] | - | 8 | - | 10 | - | 7 | - | 9 | - | 44 | - | 44 | |
| 11 | $t_{HO}$ | Data hold time(outputs) | Slave | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | ns |
| | | | Master | -15 | - | -22 | - | -15 | - | -23 | - | -22 | - | -29 | - | |
| | | | Master Loopback[5] | -10 | - | -14 | - | -10 | - | -14 | - | -14 | - | -19 | - | |
| | | | Master Loopback(slow) [6] | -15 | - | -22 | - | -15 | - | -22 | - | -21 | - | -27 | - | |
| 12 | $t_{RI/FI}$ | Rise/Fall time input | Slave | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | ns |
| | | | Master | - | | - | | - | | - | | - | | - | | |
| | | | Master Loopback[5] | - | | - | | - | | - | | - | | - | | |
| | | | Master Loopback(slow) [6] | - | | - | | - | | - | | - | | - | | |
| 13 | $t_{RO/FO}$ | Rise/Fall time output | Slave | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | ns |
| | | | Master | - | | - | | - | | - | | - | | - | | |
| | | | Master Loopback [5] | - | | - | | - | | - | | - | | - | | |
| | | | Master Loopback(slow) [6] | - | | - | | - | | - | | - | | - | | |

1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. $f_{periph}$ = LPSPI peripheral clock

4. $t_{periph} = 1/f_{periph}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
7. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
8. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.

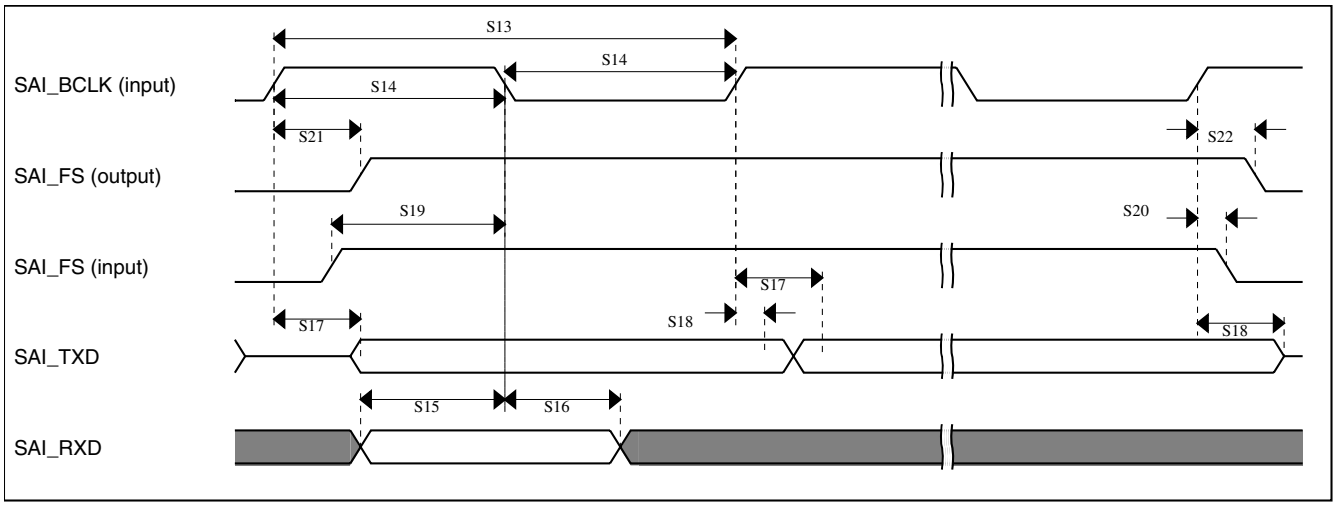



**Figure 23. SAI Timing — Slave modes**

## 6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN ), the interface should be OFF.

**Table 32. MII signal switching specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | RXCLK frequency | — | 25 | MHz |
| MII1 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| MII2 | RXCLK pulse width low | 35% | 65% | RXCLK period |
| MII3 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| MII4 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| — | TXCLK frequency | — | 25 | MHz |
| MII5 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| MII6 | TXCLK pulse width low | 35% | 65% | TXCLK period |
| MII7 | TXCLK to TXD[3:0], TXEN, TXER invalid | 2 | — | ns |
| MII8 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |

## Table 35. SWD electrical specifications

| Symbol | Description | Run Mode | | | | HSRUN Mode | | | | VLPR Mode | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| S1 | SWD_CLK frequency of operation | - | 25 | - | 25 | - | 25 | - | 25 | - | 10 | - | 10 | MHz |
| S2 | SWD_CLK cycle period | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | ns |
| S3 | SWD_CLK clock pulse width | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | ns |
| S4 | SWD_CLK rise and fall times | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | ns |
| S9 | SWD_DIO input data setup time to SWD_CLK rise | 4 | - | 4 | - | 4 | - | 4 | - | 16 | - | 16 | - | ns |
| S10 | SWD_DIO input data hold time after SWD_CLK rise | 3 | - | 3 | - | 3 | - | 3 | - | 10 | - | 10 | - | ns |
| S11 | SWD_CLK high to SWD_DIO data valid | - | 28 | - | 38 | - | 28 | - | 38 | - | 70 | - | 77 | ns |
| S12 | SWD_CLK high to SWD_DIO high-Z | - | 28 | - | 38 | - | 28 | - | 38 | - | 70 | - | 77 | ns |
| S13 | SWD_CLK high to SWD_DIO data invalid | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns |

# 9 Pinouts

## 9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

# 10 Revision History

The following table provides a revision history for this document.

**Table 40. Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 1 | 12 Aug 2016 | Initial release |
| 2 | 03 March 2017 | • Updated descpition of QSPI and Clock interfaces in Key Features section<br>• Updated figure: High-level architecture diagram for the S32K1xx family<br>• Updated figure: S32K1xx product series comparison<br>• Added note in section Determining valid orderable parts<br>• Updated figure: Ordering information<br>• In table: Absolute maximum ratings :<br>  • Added footnote to $I_{INJPAD\_DC}$<br>  • Updated min and max value of $I_{INJPAD\_DC}$<br>  • Updated description, max and min values for $I_{INJSUM}$<br>  • Updated $V_{IN\_TRANSIENT}$<br>• In table: Voltage and current operating requirements :<br>  • Renamed $V_{SUP\_OFF}$<br>  • Updated max value of $V_{DD\_OFF}$<br>  • Removed $V_{INA}$ and $V_{IN}$<br>  • Added $V_{REFH}$ and $V_{REFL}$<br>  • Updated footnote "Typical conditions assumes $V_{DD}$ = $V_{DDA}$ = $V_{REFH}$ = 5 V ...<br>  • Removed $I_{NJSUM\_AF}$<br>• Updated footnotes in table Table 4<br>• Updated section Power mode transition operating behaviors<br>• In table: Power consumption<br>  • Added footnote "With PMC_REGSC[CLKBIASDIS] ... "<br>  • Updated conditions for VLPR<br>  • Removed Idd/MHz for S32K144<br>  • Updated numbers for S32K142 and S32K148<br>  • Removed use case footnotes<br>• In section Modes configuration :<br>  • Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes _Master_configuration_sheet'<br>• In table: DC electrical specifications at 3.3 V Range :<br>  • Added footnotes to $V_{ih}$ Input Buffer High Voltage and $V_{ih}$ Input Buffer Low Voltage<br>  • Added footnote to High drive port pins<br>• In table: DC electrical specifications at 5.0 V Range : |

*Table continues on the next page...*

## Table 40. Revision History

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • Added footnotes $V_{ih}$ Input Buffer High Voltage and $V_{ih}$ Input Buffer Low Voltage<br>• Updated table: AC electrical specifications at 3.3 V range<br>• Updated table: AC electrical specifications at 5 V range<br>• In table: Standard input pin capacitance<br>  • Added footnote to Normal run mode (S32K14x series)<br>• Removed note from 1M ohms Feedback Resistor in figure Oscillator connections scheme<br>• In table: External System Oscillator electrical specifications<br>  • Updated typical of $I_{DDOSC}$ Supply current — low-gain mode (low-power mode) (HGO=0) 1 for 4 and 8 MHz<br>  • Removed rows for $I_{lk\_ext}$ EXTAL/XTAL impedence High-frequency, low-gain mode (low-power mode) and high-frequency, high-gain mode and $V_{EXTAL}$<br>  • Updated Typ. of $R_S$ low-gain mode<br>  • Updated description of $R_F$, $R_S$, and $V_{PP}$<br>  • Removed footnote from $R_F$ Feedback resistor<br>  • Updated footnote for $C_1$ $C_2$ and $R_F$<br>• In table: Table 16<br>  • Removed mention of high-frequency<br>  • Added HGO 0, 1 information<br>• In table: Fast internal RC Oscillator electrical specifications<br>  • Updated $F_{FIRC}$<br>  • Updated description of ΔF<br>  • Updated typ and max values of $T_{JIT}$ cycle-to-cycle jitter and $T_{JIT}$ Long term jitter over 1000 cycles<br>  • Added footnotes to $T_{JIT}$ cycle-to-cycle jitter and $T_{JIT}$ Long term jitter over 1000 cycles<br>  • Updated naming convention of $I_{DDFIRC}$ Supply current<br>  • Added footnote to $I_{DDFIRC}$ Supply current<br>  • Added footnote to column Parameter<br>• In table: Slow internal RC oscillator (SIRC) electrical specifications<br>  • Removed $V_{DD}$ Supply current in 2 MHz Mode<br>  • Removed footnote and updated description of ΔF<br>  • Updated footnote to $F_{SIRC}$ and $I_{DDSIRC}$<br>• In table: SPLL electrical specifications<br>  • Added row for $F_{SPLL\_REF}$ PLL Reference<br>  • Updated naming convention throughout the table<br>  • Updated the max value of $T_{SPLL\_LOCK}$ Lock detector detection time<br>• In table: Table 21<br>  • Added footnotes:<br>  • All command times assumes ...<br>  • For all EEPROM Emulation terms ...<br>  • 'First time' EERAM writes after a POR ...<br>  • Removed footnote 'Assumes 25 MHz or ...'<br>  • Updated Max of $t_{eewr32bers}$<br>  • Added parameters $t_{quickwr}$ and $t_{quickwrClnup}$<br>• In table: Table 22<br>  • Removed Typ. values for all parameters<br>  • Removed footnote 'Typical values represent ... '<br>  • Added footnote 'Any other EEE driver usage ... '<br>• Updated QuadSPI AC specifications<br>• Removed topic: Reliability, Safety and Security modules<br>• In table: 12-bit ADC operating conditions<br>  • Updated $V_{DDA}$ |

*Table continues on the next page...*