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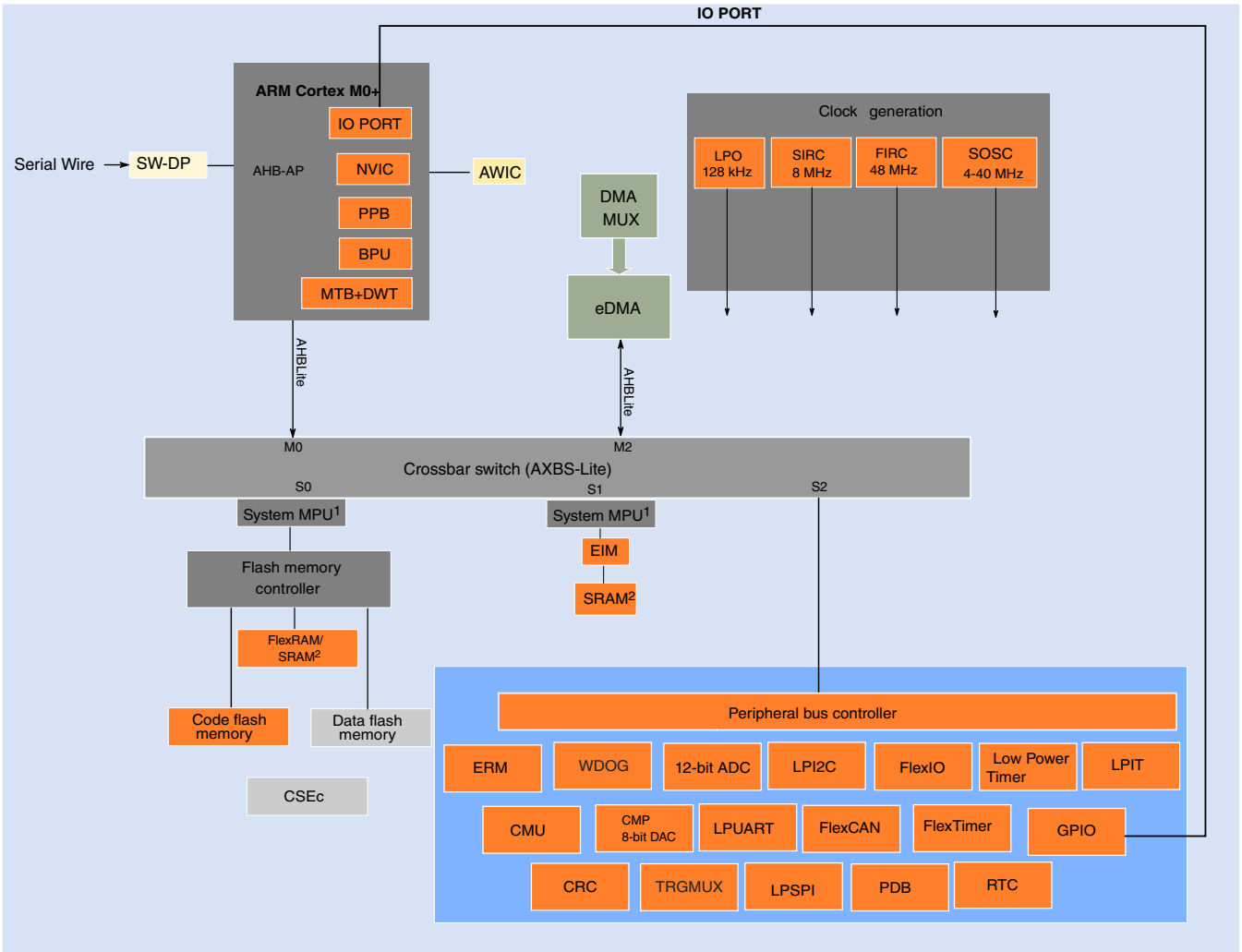
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	112MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144ust0vlht



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Crossbar master (Core, DMA) can be assigned different access rights to each protected memory region. The ARM M0+ core version in this family does not integrate the ARM Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

Key:
- Device architectural IP on all S32K devices
- Peripherals present on all S32K devices
- Peripherals present on selected S32K devices (see the "Feature Comparison" section in the RM)

Figure 2. High-level architecture diagram for the S32K11x family

2 Feature comparison

The following figure summarizes the memory and package options for the S32K product series and demonstrates where this device fits within the overall series. All devices which share a common package are pin-to-pin compatible.

Feature comparison

		S32K11x		S32K14x			
	Parameter	**K116**	**K118**	**K142**	**K144**	**K146**	**K148**
	Core	ARM® Cortex™-M0+		ARM® Cortex™-M4F			
	Frequency	48 MHz		up to 112 MHz (HSRUN)			
System	IEEE-754 FPU	o		●			
System	HW security module (CSEc)[1]	●		●			
System	CRC module	1x		1x			
System	ISO 26262	capable up to ASIL-B		capable up to ASIL-B			
System	Peripheral speed	up to 48 MHz		up to 112 MHz (HSRUN)			
System	Crossbar	●		●			
System	DMA	●		●			
System	EWM	o		●			
System	Memory protection unit	●		●			
System	FIRC CMU	●		o			
System	Watchdog	1x		1x			
System	Low power modes	●		●			
System	HSRUN mode	o		●			
System	Number of I/Os	up to 43	up to 58	up to 89		up to 128	up to 156
System	Single supply voltage	2.7 - 5.5 V		2.7 - 5.5 V			
System	Operating temperature (T_a) Temperature ambient	-40 to +85ºC / +105ºC / +125ºC		-40 to +85ºC / +105ºC / +125ºC			
Memory	Flash	128 KB	256 KB	256 KB	512 KB	1 MB	2 MB[2]
Memory	Error correction code (ECC)	●		●			
Memory	System RAM (including FlexRAM and MTB)	17 KB	25 KB	32 KB	64 KB	128 KB	256 KB
Memory	FlexRAM (also available as system RAM)	2 KB		4 KB			
Memory	Cache	o		4 KB			
Memory	EEPROM emulated by FlexRAM[1]	2 KB (up to 32 KB D-Flash)		4 KB (up to 64 KB D-Flash)			4 KB (up to 512 KB D-Flash as a part of 2 MB Flash)[3]
Memory	External memory interface	o		o			QuadSPI incl. HyperBus™
Timer	Low power interrupt timer	1x		1x			
Timer	FlexTimer (16-bit counter) 8 channels	2x (16)		4x (32)		6x (48)	8x (64)
Timer	Low power timer (LPTMR)	1x		1x			
Timer	Real time counter (RTC)	1x		1x			
Timer	Programmable delay block (PDB)	1x		2x			
Analog	Trigger mux (TRGMUX)	1x (43)	1x (45)	1x (64)		1x (73)	1x (81)
Analog	12-bit SAR ADC (1 MSPS each)	1x (14)	1x (16)	2x (16)		2x (24)	2x (32)
Analog	Comparator with 8-bit DAC	1x		1x			
Communication	100 Mbit IEEE-1588 ethernet MAC	o		o			1x
Communication	Serial audio interface (AC97, TDM, I2S)	o		o			2x
Communication	Low power UART/LIN (Supports LIN protocol versions 1.3, 2.0, 2.1, and SAE J2602)	2x		2x	3x		
Communication	Low power SPI	1x	2x	2x	3x		
Communication	Low power I2C	1x		1x			2x
Communication	FlexCAN (CAN-FD ISO/CD 11898-1)	1x (1x with FD)		2x (1x with FD)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
Communication	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		1x			
IDEs	Debug & trace	SWD, MTB (1 KB), JTAG[4]		SWD, JTAG (ITM, SWV, SWO)			SWD, JTAG (ITM, SWV, SWO), ETM
IDEs	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, COSMIC, Lauterbach, iSystems		NXP S32 Design Studio (GCC) + SDK, IAR, GHS, COSMIC, Lauterbach, iSystems			
Other	Packages	QFN-32 LQFP-48	LQFP-48 LQFP-64	LQFP-64 LQFP-100	LQFP-64 LQFP-100 MAPBGA-100	LQFP-64 MAPBGA-100 LQFP-100 LQFP-144	MAPBGA-100 LQFP-144 LQFP-176

LEGEND:
- o Not implemented
- ● Available on the device

1 No FTFC commands, including CSE commands (CSEc parts) are available when chip is in VLPR or HSRUN mode.
2 Available when EEEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
3 Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.
4 Only for BSR

Figure 3. S32K1xx product series comparison

3 Ordering parts

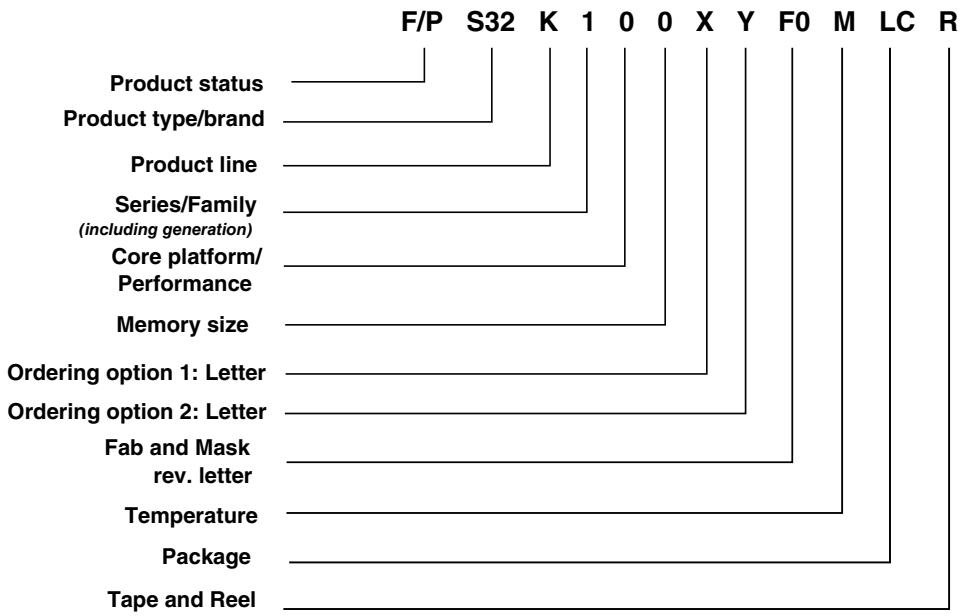
3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search. Additionally see the attachment *S32K_Part_Numbers.xlsx* .

NOTE

Not all part number combinations exist

3.2 Ordering information



Product status
P: Prototype
F: Qualified ordering P/N

Product type/brand
S32: Automotive 32-bit MCU

Product line
K: ARM Cortex MCUs
M: MagniV/Mixed Signal

Series/Family
1: 1st product series
2: 2nd product series

Core platform/Performance
1: ARM Cortex M0+
4: ARM Cortex M4F

Memory size

	2	4	6	8
M0+	32 K	64 K	128 K	256 K
M4F	256 K	512 K	1 M	2 M

Ordering option
X: Speed
B: 48 MHz without DMA (only for S32K11x)
L: 48 MHz with DMA (only for S32K11x)
M: 64 MHz
H: 80 MHz
U: 112 MHz

Y: Optional feature
N: No/None
R: Max. RAM
F: CAN-FD and FlexIO including max. RAM
S: Security including max. RAM
A: CAN-FD, FlexIO, and Security including max. RAM
E: Ethernet and audio including max. RAM
J: CAN FD, FlexIO, Security, Ethernet and audio including max. RAM

Fab and Mask rev. letter
Fx: ATMC
Tx: GF
XX: Flex #

x0: 1st fab revision
x1: 2nd fab revision

Temperature
C: -40C to 85C
V: -40C to 105C
M: -40C to 125C

Package

Pins	LQFP	LQFP -EP	QFN	BGA
32	LC	-	FM	-
48	LF	KF	FT	-
64	LH	KH	-	-
100	LL	-	-	MH
144	LQ	-	-	-
176	LU	-	-	-

Tape and Reel
T: Trays and Tubes
R: Tape and Reel

Figure 4. Ordering information

T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

- Assumes maximum θJA for 2s2p board. See Thermal characteristics

8. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

Full functionality/specifications cannot be guaranteed when voltage drops below 2.7 V.

Table 2. Voltage and current operating requirements [1]

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.
5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
6. Open drain outputs must be pulled to V_{DD}.
7. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.

4.4 Power and ground pins

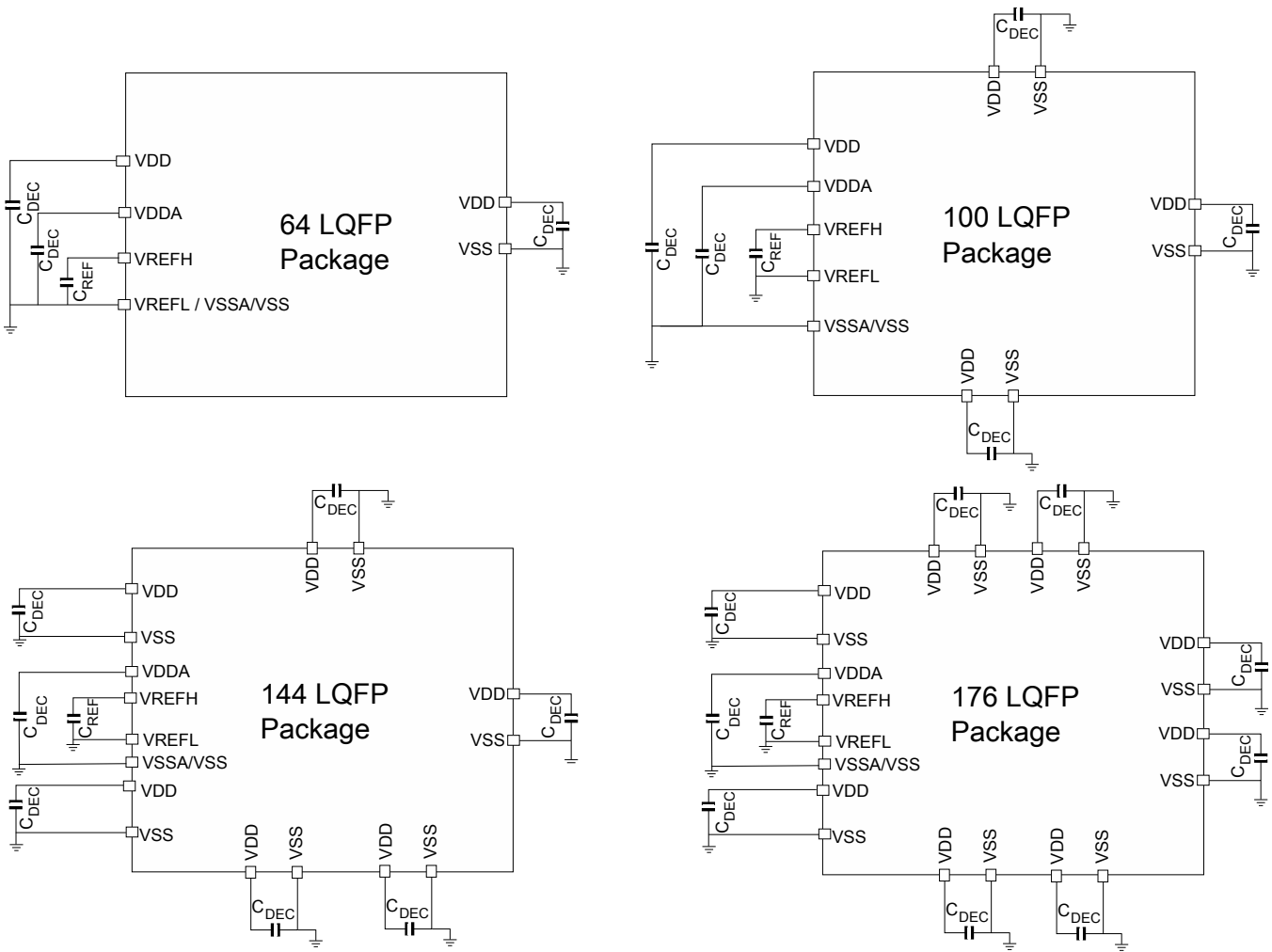


Figure 5. Pinout decoupling

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. 3	Typ.	Max.	Unit
C_{REF}, 4, 5	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} 5, 6, 7	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
   - The protection/decoupling capacitors must be on the path of the trace connected to that component.

Table 7. Power consumption (Typicals unless stated otherwise) 1

	Ambient Temperature (°C)		VLPS (µA)[2, 3]		VLPR (mA)		STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [4]		Idd/MHz (µA/MHz)[5]
			Peripherals disabled [6]	Peripherals enabled	Peripherals disabled	Peripherals enabled			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
S32K116	25	Typ	26	38	1.9	2.5	7	12	TBD	TBD	NA						TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	40							TBD
S32K118	25	Typ	26	38	1.9	2.5	7	12	TBD	TBD	NA						TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	42							TBD
S32K142	25	Typ	29	42	1.9	2.5	10	15	TBD	TBD	NA		TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD			48	57	65	75	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD			TBD	TBD	85	90	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD			60	65	NA		TBD
S32K144	25	Typ	29.8	39.1	1.48	1.50	7	7.7	19.7	26.9	25.1	33.3	30.2	39.6	43.3	55.6	378

Table continues on the next page...

Table 7. Power consumption (Typicals unless stated otherwise) 1 (continued)

	Ambient Temperature (°C)		VLPS (µA)[2, 3]		VLPR (mA)		STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [4]		Idd/MHz (µA/MHz)[5]
	85	Typ	150	159	1.72	1.85	7.2	8.1	20.4	27.1	26.1	33.5	30.5	40	43.9	56.1	381
		Max	359	384	2.60	2.65	8.3	9.2	21.9	28.5	27.8	34.4	32.9	41.5	45.5	57.5	411
	105	Typ	256	273	1.80	2.10	7.8	8.5	20.6	27.4	26.6	33.8	31.2	40.5	44.8	57.1	390
		Max	850	900	2.65	2.70	10.3	10.6	22.7	30	28.3	36.5	33.4	43.3	47.9	61.3	418
	125	Max	1960	1998	3.18	3.25	12.2	13	25.3	32.7	35	39.8	37.1	46.5	NA	NA	464
S32K146	25	Typ	40	55	5	6	15	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	95	110	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	70	80	NA	NA	TBD
S32K148[7, 8]	25	Typ	40	60	5	6	15	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	120	125	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	100	110	NA	NA	TBD

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration.
2. This is an average based on the use case described in the Comparator section, whereby the analog sampling is taking place periodically, with a mechanism to only enable the DAC as required. The numbers quoted assumes that only a single ANLCMP is active and the others are disabled
3. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
4. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
5. Values mentioned are measured at 25 ℃ at RUN@80 MHz with peripherals disabled.
6. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
7. Above S32K148 data is preliminary targets only
8. The S32K148 data points assume that ENET/QuadSPI/SAI etc. are active. If the same configuration is selected as per the S32K144, then the two devices will have very similar IDD.

Table 10. DC electrical specifications at 5.0 V Range (continued)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
Ioh_Strong	I/O current source capability measured when pad = V_{DDE} - 0.8 V	20	—	—	mA	3, 4
Iol_Strong	I/O current sink capability measured when pad = 0.8 V	20	—	—	mA	4, 5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	7
R_{PD}	Internal pulldown resistors	20		50	kΩ	8

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
4. The strong pad I/O pin is capable of switching a 50 pF load at up to 40 MHz.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. Measured at input V = V_{SS}
8. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 11. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
Standard	NA	4.6	14.5	3.9	15.7	25
		7.2	23.7	6.2	26.2	50
		24.0	75.4	20.8	88.4	200
Strong	0	4.6	14.5	3.9	15.7	25
		7.2	23.7	6.2	26.2	50
		24.0	75.4	20.8	88.4	200
	1	2.0	5.8	1.8	6.1	25
		2.8	8.0	2.6	8.3	50
		7.0	20.7	6.0	22.4	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

Table 15. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Table 16. External System Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_hi}	Oscillator crystal or resonator frequency	4	—	40	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal Start-up Time					
	8 MHz low-gain mode (HGO=0)	—	1.5	—	ms	1
	8 MHz high-gain mode (HGO=1)	—	2.5	—		
	40 MHz low-gain mode (HGO=0)	—	2	—		
	40 MHz high-gain mode (HGO=1)	—	2	—		

1. Proper PC board layout procedures must be followed to achieve specifications.

6.2.4 Low Power Oscillator (LPO) electrical specifications

Table 19. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	113	128	139	kHz
$T_{startup}$	Startup Time	—	—	20	µs

6.2.5 SPLL electrical specifications

Table 20. SPLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPLL_REF}[1]	PLL Reference Frequency Range	8	—	16	MHz
F_{SPLL_Input}[2]	PLL Input Frequency	8	—	40	MHz
F_{VCO_CLK}	VCO output frequency	180	—	320	MHz
F_{SPLL_CLK}	PLL output frequency	90	—	160	MHz
J_{CYC_SPLL}	PLL Period Jitter (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	120	—	ps
	at F_{VCO_CLK} 320 MHz	—	75	—	ps
J_{ACC_SPLL}	PLL accumulated jitter over 1µs (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	1350	—	ps
	at F_{VCO_CLK} 320 MHz	—	600	—	ps
D_{UNL}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%
T_{SPLL_LOCK}	Lock detector detection time[4]	—	—	$150 \times 10^{-6} + 1075(1/F_{SPLL\_REF})$	s

1. F_{SPLL_REF} is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLLCFG register of Reference Manual.
2. F_{SPLL_Input} is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

6.3 Memory and memory interfaces

6.3.1 Flash memory module (FTFC) electrical specifications

This section describes the electrical characteristics of the flash memory module.

Table 29. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_v	Data valid (after SPSCK edge)	Slave	-	30	-	39	-	26	-	36	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback[5]	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow) [6]	-	8	-	10	-	7	-	9	-	44	-	44	
11	t_{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback[5]	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	
			Master Loopback(slow) [6]	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	$t_{RI/FI}$	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		
			Master Loopback[5]	-		-		-		-		-		-		
			Master Loopback(slow) [6]	-		-		-		-		-		-		
13	$t_{RO/FO}$	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		
			Master Loopback [5]	-		-		-		-		-		-		
			Master Loopback(slow) [6]	-		-		-		-		-		-		

1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. f_{periph} = LPSPI peripheral clock

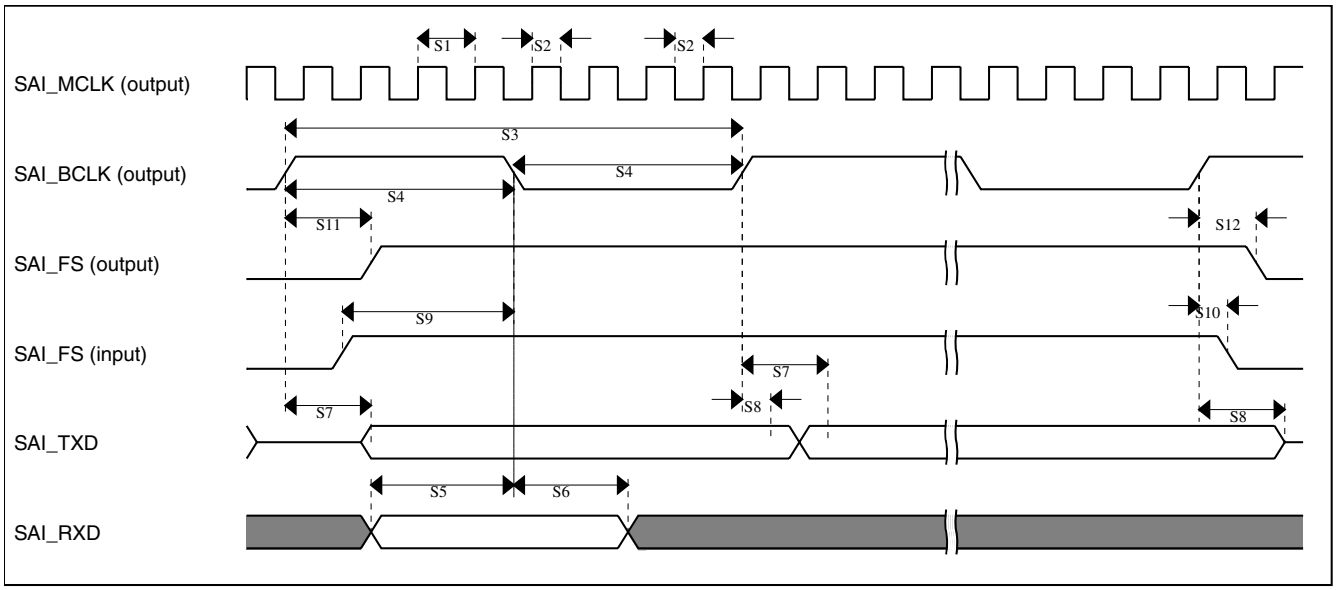


Figure 22. SAI Timing — Master modes

Table 31. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14[1]	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

Table 33. RMII signal switching specifications (continued)

Symbol	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	2	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

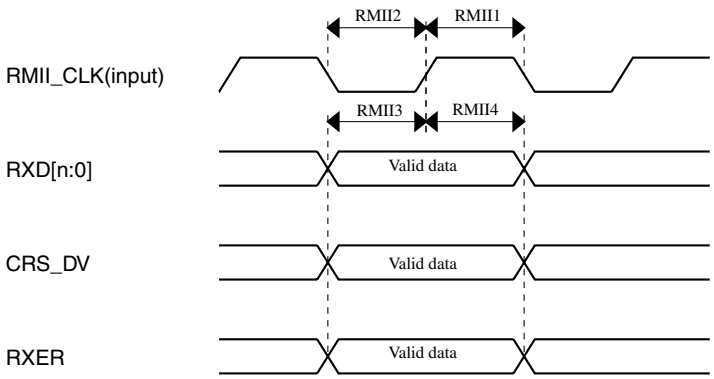


Figure 26. RMII receive diagram

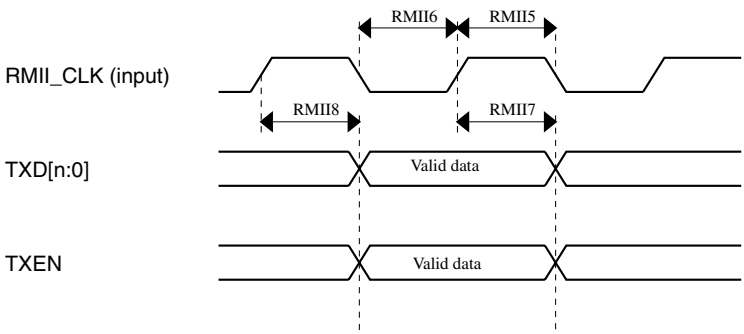


Figure 27. RMII transmit diagram

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- MDIO pin must have external Pull-up.

Table 34. MDIO timing specifications

Symbol	Description	Min.	Max.	Unit
—	MDC Clock Frequency	—	2.5	MHz

Table continues on the next page...

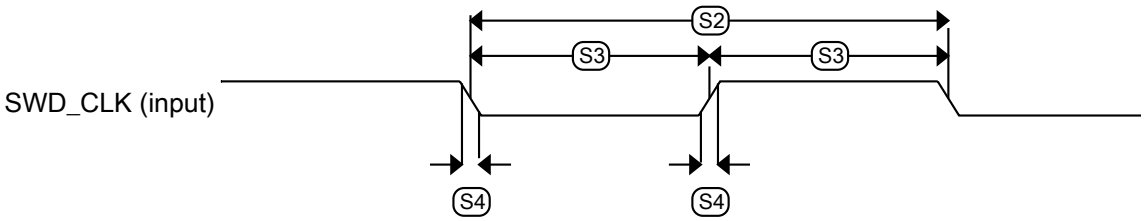


Figure 29. Serial wire clock input timing

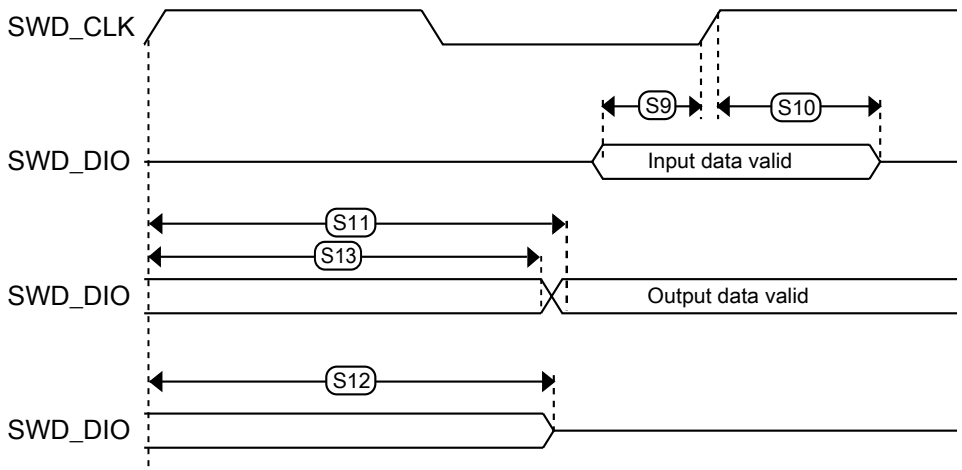


Figure 30. Serial wire data timing

6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. Trace specifications

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
—	Fsys	System frequency	80	48	40	112	80	4	MHz

Table continues on the next page...

Table 36. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

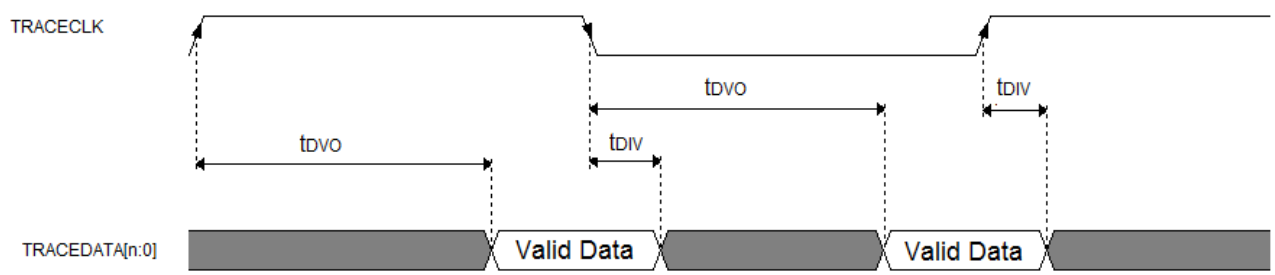


Figure 31. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

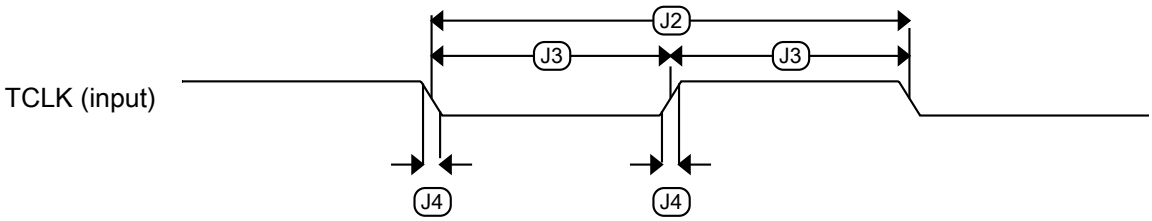


Figure 32. Test clock input timing

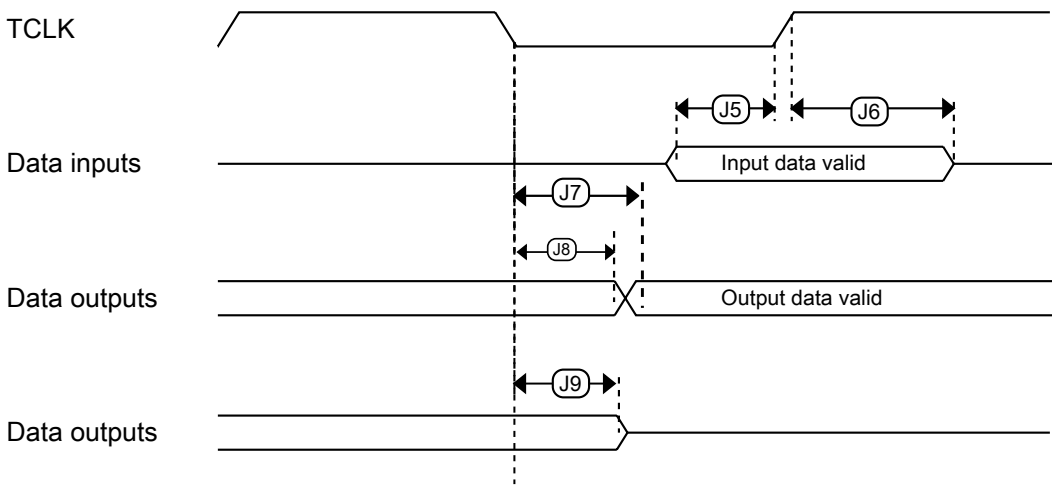


Figure 33. Boundary scan (JTAG) timing

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number
32-pin QFN	SOT617-3 [1]
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W
100 MAP BGA	98ASA00802D
144-pin LQFP	98ASS23177W
176-pin LQFP	98ASS23479W

1. 5x5 mm package

Table 40. Revision History

Rev. No.	Date	Substantial Changes

		• Added footnotes V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		• Updated table: AC electrical specifications at 3.3 V range
		• Updated table: AC electrical specifications at 5 V range
		• In table: Standard input pin capacitance
		  • Added footnote to Normal run mode (S32K14x series)
		• Removed note from 1M ohms Feedback Resistor in figure Oscillator connections scheme
		• In table: External System Oscillator electrical specifications
		  • Updated typical of I_{DDOSC} Supply current — low-gain mode (low-power mode) (HGO=0) 1 for 4 and 8 MHz
		  • Removed rows for I_{lk_ext} EXTAL/XTAL impedence High-frequency, low-gain mode (low-power mode) and high-frequency, high-gain mode and V_{EXTAL}
		  • Updated Typ. of R_S low-gain mode
		  • Updated description of R_F, R_S, and V_{PP}
		  • Removed footnote from R_F Feedback resistor
		  • Updated footnote for C_1 C_2 and R_F
		• In table: Table 16
		  • Removed mention of high-frequency
		  • Added HGO 0, 1 information
		• In table: Fast internal RC Oscillator electrical specifications
		  • Updated F_{FIRC}
		  • Updated description of ΔF
		  • Updated typ and max values of T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Added footnotes to T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Updated naming convention of I_{DDFIRC} Supply current
		  • Added footnote to I_{DDFIRC} Supply current
		  • Added footnote to column Parameter
		• In table: Slow internal RC oscillator (SIRC) electrical specifications
		  • Removed V_{DD} Supply current in 2 MHz Mode
		  • Removed footnote and updated description of ΔF
		  • Updated footnote to F_{SIRC} and I_{DDSIRC}
		• In table: SPLL electrical specifications
		  • Added row for F_{SPLL_REF} PLL Reference
		  • Updated naming convention throughout the table
		  • Updated the max value of T_{SPLL_LOCK} Lock detector detection time
		• In table: Table 21
		  • Added footnotes:
		  • All command times assumes ...
		  • For all EEPROM Emulation terms ...
		  • 'First time' EERAM writes after a POR ...
		  • Removed footnote 'Assumes 25 MHz or ...'
		  • Updated Max of $t_{eewr32bers}$
		  • Added parameters $t_{quickwr}$ and $t_{quickwrClnup}$
		• In table: Table 22
		  • Removed Typ. values for all parameters
		  • Removed footnote 'Typical values represent ... '
		  • Added footnote 'Any other EEE driver usage ... '
		• Updated QuadSPI AC specifications
		• Removed topic: Reliability, Safety and Security modules
		• In table: 12-bit ADC operating conditions
		  • Updated V_{DDA}

Table continues on the next page...

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