#### NXP USA Inc. - FS32K146HRT0CLHT Datasheet





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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, FlexIO, I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k146hrt0clht

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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# 1 Block diagram

Following figures show superset high level architecture block diagrams of S32K14x series and S32K11x series respectively. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.

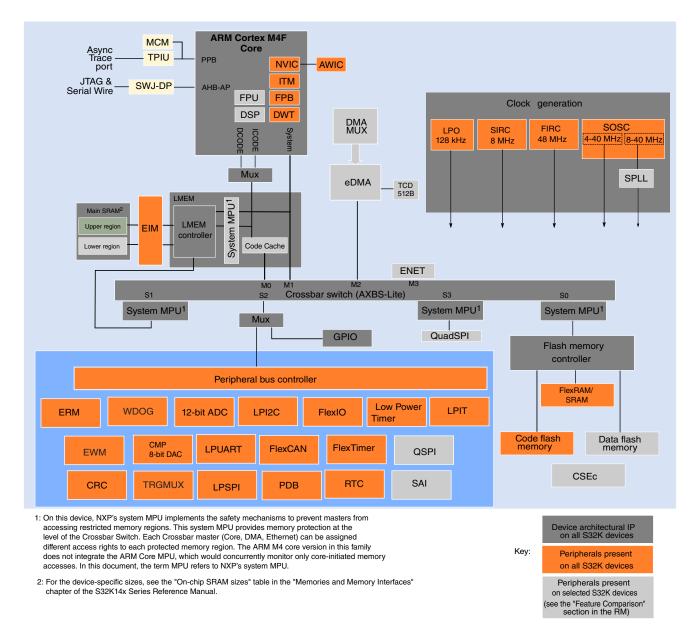


Figure 1. High-level architecture diagram for the S32K14x family

# 3 Ordering parts

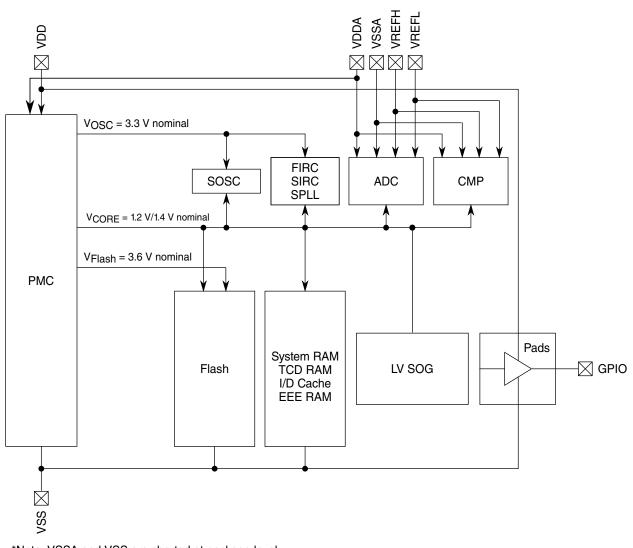
## 3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search. Additionally see the attachment  $S32K_Part_Numbers.xlsx$ .

### NOTE

Not all part number combinations exist

- No trace exceeding 1 mm from the protection to the trace or to the ground.
- The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
- The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.



\*Note: VSSA and VSS are shorted at package level

#### Figure 6. Power diagram

## 4.5 LVR, LVD and POR operating requirements

### Table 5. V<sub>DD</sub> supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>POR</sub>	Rising and falling $V_{DD}$ POR detect voltage	1.1	1.6	2.0	V	
V <sub>LVR</sub>	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V <sub>LVR_HYST</sub>	LVR hysteresis	—	45	—	mV	1
V <sub>LVR_LP</sub>	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	

Table continues on the next page...

Symbol	Description	Min.	Тур.	Max.	Unit
	$VLPS \rightarrow RUN$	8	—	17	μs
	STOP1 → RUN	0.07	0.075	0.08	μs
	$STOP2 \rightarrow RUN$	0.07	0.075	0.08	μs
	$VLPR \rightarrow RUN$	19	_	26	μs
	$VLPR \rightarrow VLPS$	5.75	6.25	6.5	μs
	$VLPS \rightarrow VLPR$	26.5	27.25	27.75	μs
	$RUN \rightarrow Compute operation$	0.35	0.38	0.4	μs
	HSRUN $\rightarrow$ Compute operation	0.3	0.31	0.35	μs
	$RUN \rightarrow STOP1$	0.35	0.38	0.4	μs
	$RUN \rightarrow STOP2$	0.2	0.23	0.25	μs
	$RUN \rightarrow VLPS$	0.35	0.38	0.4	μs
	$RUN \rightarrow VLPR$	4.4	4.7	5	μs
	VLPS → Asynchronous DMA Wakeup	105	110	125	μs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	Pin reset $\rightarrow$ Code execution	_	214		μs

 Table 6. Power mode transition operating behaviors (continued)

### NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

## 4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations.

## 4.7.1 Modes configuration

Attached *S32K1xx\_Power\_Modes \_Configuration.xlsx* details the modes used in gathering the power consumption data stated in the above table Table 7. For full functionality refer to table: Module operation in available low power modes of the *Reference Manual*.

## 4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	- 4000	4000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	- 500	500	V	
	Corner pins only	- 750	750	V	
I <sub>LAT</sub>	Latch-up current at ambient temperature of 125 °C	- 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

## 4.9 EMC radiated emissions operating behaviors

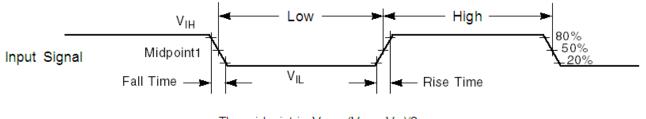
EMC measurements to IC-level IEC standards are available from NXP on request.

# 5 I/O parameters

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

I/O parameters



The midpoint is  $V_{IL}$  +  $(V_{IH} - V_{IL})/2$ .

Figure 7. Input signal measurement reference

## 5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Symbol	I Description		Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	_	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	_	ns	3
WFRST	RESET input filtered pulse		100	ns	4
WFRST	RESET input not filtered pulse	100	—	ns	

Table 8. General switching specifications

 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.

- 2. The greater of synchronous and asynchronous timing must be met.
- 3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
- 4. Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.

## 5.3 DC electrical specifications at 3.3 V Range

#### Table 9. DC electrical specifications at 3.3 V Range

Symbol	Parameter		Value	Unit	Notes	
		Min.	Тур.	Max.		
V <sub>DD</sub>	I/O Supply Voltage	2.7	3.3	4	V	1
V <sub>ih</sub>	Input Buffer High Voltage	$0.7 \times V_{DD}$	_	V <sub>DD</sub> + 0.3	V	2
V <sub>il</sub>	Input Buffer Low Voltage	V <sub>SS</sub> – 0.3	_	$0.3 \times V_{DD}$	V	3
V <sub>hys</sub>	Input Buffer Hysteresis	$0.06 \times V_{DD}$	_	—	V	
loh_Standard	I/O current source capability measured when pad = $(V_{DDE} - 0.8 V)$	3.5		—	mA	

Table continues on the next page...

Symbol	Parameter	Value			Unit	Notes
		Min.	Тур.	Max.	1	
lol_Standard	I/O current sink capability measured when pad = 0.8 V	3	_	_	mA	
loh_Strong	I/O current source capability measured when pad = $(V_{DDE} - 0.8 V)$	14	_	—	mA	4
Iol_Strong	I/O current sink capability measured when pad = 0.8 V	12		_	mA	5
IOHT	Output high current total for all ports	—	_	100	mA	
IIN	Input leakage current (per pin) for full temper	ature range a	at V <sub>DD</sub> = 3.3	V		6
	All pins other than high drive port pins		0.005	0.5	μA	
	High drive port pins <sup>7</sup>		0.010	0.5	μA	
R <sub>PU</sub>	Internal pullup resistors	20		60	kΩ	8
R <sub>PD</sub>	Internal pulldown resistors	20		60	kΩ	9

#### Table 9. DC electrical specifications at 3.3 V Range (continued)

- 1. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
- 2. For reset pads, same  $V_{ih}$  levels are applicable
- 3. For reset pads, same  $V_{il}$  levels are applicable
- 4. The value given is measured at high drive strength mode. For value at low drive strength mode see the loh\_Standard value given above.
- 5. The value given is measured at high drive strength mode. For value at low drive strength mode see the lol\_Standard value given above.
- 6. Several I/O have both high drive and normal drive capability selected by the associated Portx\_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to S32K144\_IO\_Signal\_Description\_Input\_Multiplexing.xlsx attached with the *Reference Manual*.
- 7. When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
- 8. Measured at input  $V = V_{SS}$
- 9. Measured at input  $V = V_{DD}$

### 5.4 DC electrical specifications at 5.0 V Range

#### Table 10. DC electrical specifications at 5.0 V Range

Symbol	Parameter		Value			Notes
		Min.	Тур.	Max.		
V <sub>DD</sub>	I/O Supply Voltage	4		5.5	V	
V <sub>ih</sub>	Input Buffer High Voltage	0.65 x V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V	1
V <sub>il</sub>	Input Buffer Low Voltage	V <sub>SS</sub> – 0.3		0.35 x V <sub>DD</sub>	V	2
V <sub>hys</sub>	Input Buffer Hysteresis	0.06 x V <sub>DD</sub>			V	
Ioh_Standard	I/O current source capability measured when $pad = (V_{DDE} - 0.8)$ V)	5	—	_	mA	
lol_Standard	I/O current sink capability measured when pad = 0.8 V	5	—		mA	

Table continues on the next page...

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Symbol	Description	Min.	Max.	Unit
f <sub>SYS</sub>	System and core clock	_	48	MHz
f <sub>BUS</sub>	Bus clock		24	MHz
f <sub>FLASH</sub>	Flash clock	_	24	MHz
	Normal run mode (S32K14x series)	3		
f <sub>SYS</sub>	System and core clock		80	MHz
f <sub>BUS</sub>	Bus clock	_	40	MHz
f <sub>FLASH</sub>	Flash clock	—	26.67	MHz
	VLPR mode <sup>4</sup>			•
f <sub>SYS</sub>	System and core clock		4	MHz
f <sub>BUS</sub>	Bus clock	—	4	MHz
f <sub>FLASH</sub>	Flash clock		1	MHz
f <sub>ERCLK</sub>	External reference clock	_	16	MHz

 Table 14.
 Device clock specifications 1 (continued)

1. Refer to the section Feature comparison for the availability of modes and other specifications.

2. Only available on some devices. See section Feature comparison.

3. With SPLL as system clock source.

4. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

# 6 Peripheral operating requirements and behaviors

## 6.1 System modules

There are no electrical specifications necessary for the device's system modules.

## 6.2 Clock interface modules

### 6.2.1 External System Oscillator electrical specifications

## 6.2.3 System Clock Generation (SCG) specifications

#### 6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications Table 17. Fast internal RC Oscillator electrical specifications

Symbol	Parameter <sup>1</sup>	Value			Unit
		Min.	Тур.	Max.	
F <sub>FIRC</sub>	FIRC target frequency	—	48		MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	%F <sub>FIRC</sub>
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	%F <sub>FIRC</sub>
T <sub>Startup</sub>	Startup time		3.4	5	μs²
T <sub>JIT</sub> , 3	Cycle-to-Cycle jitter	—	250	500	ps
T <sub>JIT</sub> <sup>3</sup>	Long term jitter over 1000 cycles	—	0.04	0.1	%F <sub>FIRC</sub>

1. With FIRC regulator enable

2. Startup time is defined as the time between clock enablement and clock availability for system use.

3. FIRC as system clock

### NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

#### 6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications Table 18. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter		Unit		
		Min.	Тур.	Max.	
F <sub>SIRC</sub>	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	_	_	±3	%F <sub>SIRC</sub>
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	_	_	±3.3	%F <sub>SIRC</sub>
T <sub>Startup</sub>	Startup time	—	9	12.5	µs <sup>1</sup>

1. Startup time is defined as the time between clock enablement and clock availability for system use.

Symbol	Description <sup>1</sup>	Min.	Тур.	Max.	Unit	Notes
t <sub>eewr16b64k</sub>	<ul><li> 48 KB EEPROM backup</li><li> 64 KB EEPROM backup</li></ul>	_	475	2000	μs	
t <sub>eewr32bers</sub>	32-bit write to erased FlexRAM location execution time		360	2000	μs	
t <sub>eewr32b32k</sub> t <sub>eewr32b48k</sub> t <sub>eewr32b64k</sub>	<ul> <li>32-bit write to FlexRAM execution time:</li> <li>32 KB EEPROM backup</li> <li>48 KB EEPROM backup</li> <li>64 KB EEPROM backup</li> </ul>		630 720 810	2000 2125 2250	μs μs μs	3, 4
t <sub>quickwr</sub>	32-bit Quick Write execution time : Time from CCI complete, ready for next 32-bit write)	F clearing (st	art the write)	until CCIF s	etting (32-bit	write
	<ul> <li>1st 32-bit write</li> <li>2nd through Next to Last (Nth-1) 32-bit write</li> <li>Last (Nth) 32-bit write (time for write only, not cleanup)</li> </ul>		200 150 200	550 550 550	µs µs µs	5, 6
t <sub>quickwr</sub> Clnup	Quick Write Cleanup execution time			(Number of Quick Writes) * 2.0	ms	7

Table 21. Flash command timing specifications (continued)

- 1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
- 2. Maximum times for erase parameters based on expectations at cycling end-of-life.
- 3. For all EEPROM Emulation terms, the specified timing shown assumes previous record clean up has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 No EEPROM issues detected.
- 4. 'First time' EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
- 5. For 'Typ.', only after the Nth write completes will any data will be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power or reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
- 6. Quick Write may take up to 550 µs as additional cleanup may occur when crossing sector boundaries.
- 7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

### NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

### 6.3.1.2 Reliability specifications

### Table 22. NVM reliability specifications

Symbol	Symbol Description		Min. Typ.		Unit	Notes
	When using as Program	and Data	Flash			

Table continues on the next page ...

FLASH PORT	Sym	Unit						FLA	ASH A							FLA	ASH B	
	1				Rl	JN <sup>1</sup>					HSF	RUN <sup>1</sup>			RUN/HSRUN <sup>2</sup>			
QuadSPI Mode	1			SDR				SDR					SDR		DDR <sup>3</sup>			
				ernal pling		Internal DQS				Internal Internal DQS Sampling				Internal Sampling		External DQS		
			Ν	N1 L		PAD Internal Loopback Loopback		1	N1 PAD Internal Loopback Loopback				N1		Extrenal DQS			
			Min	Мах	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCK Duty Cycle	t <sub>SDC</sub>	ns	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 0.750	tSCK/2 - 0.750	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 2.5	tSCK/2 + 2.5	tSCK/2 - 2.5	tSCK/2 + 2.5

-

4.5

-

-

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4

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10

5

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10

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25

0

-

5

10

5

25

-

10

-

-

-

Table 23 QuadSPI electrical specifications (continued)

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1. See Reference Manual for details on mode settings

2. See Reference Manual for details on mode settings

t<sub>IH</sub>

tov

t<sub>IV</sub>

t<sub>CSSCK</sub>

t<sub>SCKCS</sub>

ns

ns

ns

ns

ns

pf

0

-

5

5

5

-

4.5

-

-

-

25

1

-

5

5

5

25

-

4.5

-

-

-

1

-

5

5

5

25

3. Valid for HyperRAM only

Data Input Hold Time

Data Output Valid Time

Data Output In-Valid

Time

CS to SCK Time 6

SCK to CS Time 7

Output Load

4. RWDS(External DQS CLK) frequency

5. For operating frequency  $\leq$  64 Mhz,Output invalid time is 5 ns.

6. Program register value QuadSPI\_FLSHCR[TCSS] = 4`h2

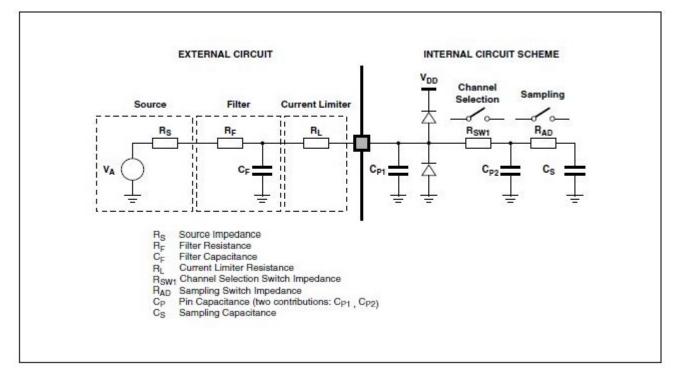
7. Program register value QuadSPI\_FLSHCR[TCSH] = 4`h1

32

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
C <sub>P2</sub>	Analog Bus Capacitance		—	—	4	pF	
C <sub>S</sub>	Sampling capacitance		_	4	5	pF	
f <sub>ADCK</sub>	ADC conversion clock frequency	Normal usage	2	40	50	MHz	4, 5
f <sub>CONV</sub>	ADC conversion frequency	No ADC hardware averaging. <sup>6</sup> Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	7, 8
		ADC hardware averaging set to 32. <sup>6</sup> Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	7, 8

Table 24. 12-bit ADC operating conditions (continued)

- 1. Typical values assume  $V_{DDA} = 5 \text{ V}$ , Temp = 25 °C,  $f_{ADCK} = 40 \text{ MHz}$ ,  $R_{AS}=20 \Omega$ , and  $C_{AS}=10 \text{ nF}$  unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- For packages without dedicated V<sub>REFH</sub> and V<sub>REFL</sub> pins, V<sub>REFH</sub> is internally tied to V<sub>DDA</sub>, and V<sub>REFL</sub> is internally tied to V<sub>SS</sub>. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
- 4. Clock and compare cycle need to be set according to the guidelines mentioned in the Reference Manual .
- 5. ADC conversion will become less reliable above maximum frequency.
- 6. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
- 7. Numbers based on the minimum sampling time of 275 ns.
- 8. For guidelines and examples of conversion rate calculation, see the *Reference Manual* or download the ADC calculator tool.



#### Figure 13. ADC input impedance equivalency diagram

**ADC electrical specifications** 

Table 26. 12-bit ADC characteristics (3 V to 5.5 V)( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SS}$ ) (continued)

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
TUE <sup>4</sup>	Total unadjusted error		—	±4	±8	LSB <sup>5</sup>	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	_	LSB <sup>5</sup>	6, 7, 8, 9
INL	Integral non-linearity			±1.0	_	LSB <sup>5</sup>	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V<sub>REFH</sub>=V<sub>DDA</sub>=V<sub>DD</sub>, with the calibration frequency set to half the ADC clock frequency.

2. Typical values assume  $V_{DDA} = 5.0 \text{ V}$ , Temp = 25 °C,  $f_{ADCK} = 40 \text{ MHz}$ ,  $R_{AS}=20 \Omega$ , and  $C_{AS}=10 \text{ nF}$  unless otherwise stated.

3. The ADC supply current depends on the ADC conversion rate.

4. Represents total static error, which includes offset and full scale error.

5. 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$ 

6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.

 For ADC signals adjacent to V<sub>DD</sub>/V<sub>SS</sub> or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.

8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.

9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

#### NOTE

When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

## 6.4.2 CMP with 8-bit DAC electrical specifications

 Table 28.
 Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
I <sub>DDHS</sub>	Supply current, High-speed mode <sup>1</sup>			-	μA
	-40 - 125 °C	_	230	300	
I <sub>DDLS</sub>	Supply current, Low-speed mode <sup>1</sup>				μA
	-40 - 105 °C		5	10	
	-40 - 125 °C		5	13	

Table continues on the next page...

**Communication modules** 

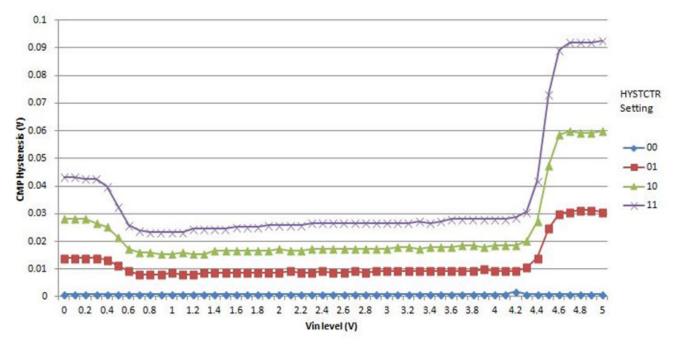


Figure 17. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 1)

## 6.5 Communication modules

### 6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

### 6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) \* SBR).

For details, see section: 'Baud rate generation' of the Reference Manual.

## 6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting ( DSE = 1 ).

### Table 29. LPSPI electrical specifications1 (continued)

Num	Symbol	Description	Conditions		Run	Mode <sup>2</sup>		T	HSRU	N Mode <sup>2</sup>			VLP	R Mode		Un																	
				5.0	V IO	3.3	V IO	5.0	O V IO	3.3	V IO	5.0	V IO	3.3 \	/ 10	1																	
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	1																	
5	t <sub>WSPSCK</sub>	Clock(SPSC	Slave													ns																	
		K) high or low time	Master																														
		(SPSCK duty cycle)	Master Loopback <sup>5</sup>																														
6			Master Loopback(slow) 6	tspsck/2 - 3	tspsck/2 + 3	tspsck/2 - 3	tspsck/2 + 3	tspsck/2 - 3	tspsck/2 + 3	tspsck/2 - 3	tspsck/2 + 3	tsPSCK/2 - 5	tspsck/2 + 5	tsPSCK/2 - 5	t <sub>sPSCK</sub> /2 + 5																		
6	t <sub>SU</sub>	Data setup	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns																	
		time(inputs)	Master	29	-	38	-	26	-	37	-	72	-	78	-	1																	
			Master	7	-	8	-	5	-	7	-	20	-	20	-	1																	
			Loopback <sup>5</sup>																														
		-	N L 6	l L e				l	L 6	Lo 6	Lc 6	L0 6	Lc 6	Lc 6	Lc 6	L 6	L0 6	Lo 6	Lc 6	Master Loopback(slow) 6	8	-	10	-	7	-	9	-	20	-	20	-	
7	t <sub>HI</sub>	Data hold	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns																	
		time(inputs)	Master	0	-	0	-	0	-	0	-	0	-	0	-	1																	
												Master	3	-	3	-	2	-	3	-	11	-	11	-	1								
			Loopback <sup>5</sup>																														
			Master Loopback(slow)	3	-	3	-	3	-	3	-	12	-	12	-																		
8	t <sub>a</sub>	Slave access time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns																	
9	t <sub>dis</sub>	Slave MISO (SOUT) disable time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns																	

Table continues on the next page...

#### **Communication modules**

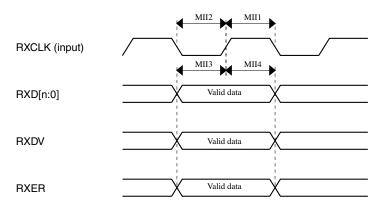
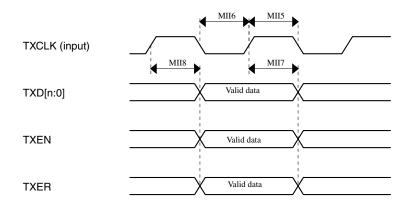


Figure 24. MII receive diagram



#### Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN ), the interface should be OFF.

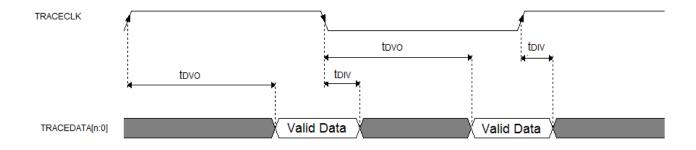
Symbol	Description	Min.	Max.	Unit
_	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

#### S32K1xx Data Sheet, Rev. 4, 06/2017 Preliminary

	Symbol	Description	F	RUN Mode	9	HSRU	N Mode	VLPR Mode	Unit
	f <sub>TRACE</sub>	Max Trace frequency	80	48	40	74.667	80	4	MHz
ads	t <sub>DVO</sub>	Data Output Valid	4	4	4	4	4	20	ns
Trace on fast pads	t <sub>DIV</sub>	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
	f <sub>TRACE</sub>	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
ads	t <sub>DVO</sub>	Data Output Valid	8	8	8	8	8	20	ns
Trace on slow pads	t <sub>DIV</sub>	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

Table 36. Trace specifications (continued)





## 6.6.3 JTAG electrical specifications

Rev. No.	Date	Substantial Changes
		<ul> <li>Added footnotes V<sub>ih</sub> Input Buffer High Voltage and V<sub>ih</sub> Input Buffer Low</li> </ul>
		Voltage
		Updated table: AC electrical specifications at 3.3 V range
		Updated table: AC electrical specifications at 5 V range
		<ul> <li>In table: Standard input pin capacitance</li> <li>Added factacts to Normal run mode (S20K14x parioe)</li> </ul>
		<ul> <li>Added footnote to Normal run mode (S32K14x series)</li> <li>Removed note from 1M ohms Feedback Resistor in figure Oscillator</li> </ul>
		connections scheme
		In table: External System Oscillator electrical specifications
		<ul> <li>Updated typical of I<sub>DDOSC</sub> Supply current — low-gain mode (low-power</li> </ul>
		mode) (HGO=0) 1 for 4 and 8 MHz
		<ul> <li>Removed rows for I<sub>Ik_ext</sub> EXTAL/XTAL impedence High-frequency, low-</li> </ul>
		gain mode (low-power mode) and high-frequency, high-gain mode and
		V <sub>EXTAL</sub>
		Updated Typ. of R <sub>S</sub> low-gain mode
		<ul> <li>Updated description of R<sub>F</sub>, R<sub>S</sub>, and V<sub>PP</sub></li> <li>Removed footnote from R<sub>F</sub> Feedback resistor</li> </ul>
		• Updated footnote for $C_1 C_2$ and $R_F$
		• In table: Table 16
		<ul> <li>Removed mention of high-frequency</li> </ul>
		Added HGO 0, 1 information
		<ul> <li>In table: Fast internal RC Oscillator electrical specifications</li> </ul>
		Updated F <sub>FIRC</sub>
		• Updated description of $\Delta F$
		<ul> <li>Updated typ and max values of T<sub>JIT</sub> cycle-to-cycle jitter and T<sub>JIT</sub> Long</li> <li>torm jitter over 1000 evelop</li> </ul>
		term jitter over 1000 cycles <ul> <li>Added footnotes to T<sub>JIT</sub> cycle-to-cycle jitter and T<sub>JIT</sub> Long term jitter</li> </ul>
		over 1000 cycles
		<ul> <li>Updated naming convention of I<sub>DDFIRC</sub> Supply current</li> </ul>
		Added footnote to I <sub>DDFIRC</sub> Supply current
		<ul> <li>Added footnote to column Parameter</li> </ul>
		In table: Slow internal RC oscillator (SIRC) electrical specifications
		Removed V <sub>DD</sub> Supply current in 2 MHz Mode
		<ul> <li>Removed footnote and updated description of ΔF</li> <li>Updated footnote to F<sub>SIRC</sub> and I<sub>DDSIRC</sub></li> </ul>
		In table: SPLL electrical specifications
		Added row for F <sub>SPLL REF</sub> PLL Reference
		<ul> <li>Updated naming convention throughout the table</li> </ul>
		<ul> <li>Updated the max value of T<sub>SPLL_LOCK</sub> Lock detector detection time</li> </ul>
		In table: Table 21
		Added footnotes:
		<ul> <li>All command times assumes</li> <li>For all EEPROM Emulation terms</li> </ul>
		<ul> <li>'First time' EERAM writes after a POR</li> </ul>
		<ul> <li>Removed footnote 'Assumes 25 MHz or'</li> </ul>
		Updated Max of t <sub>eewr32bers</sub>
		Added parameters t <sub>quickwr</sub> and t <sub>quickwrClnup</sub>
		In table: Table 22
		Removed Typ. values for all parameters
		Removed footnote 'Typical values represent '     Added footnote 'Any other EEE driver usage
		<ul> <li>Added footnote 'Any other EEE driver usage '</li> <li>Updated QuadSPI AC specifications</li> </ul>
		<ul> <li>Removed topic: Reliability, Safety and Security modules</li> </ul>
		<ul> <li>In table: 12-bit ADC operating conditions</li> </ul>
		Updated V <sub>DDA</sub>

Table continues on the next page ...

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