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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-fl.com/product-detail/nxp-semiconductors/fs32k146hrt0cllt

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search. Additionally see the attachment *S32K_Part_Numbers.xlsx*.

NOTE

Not all part number combinations exist

3.2 Ordering information

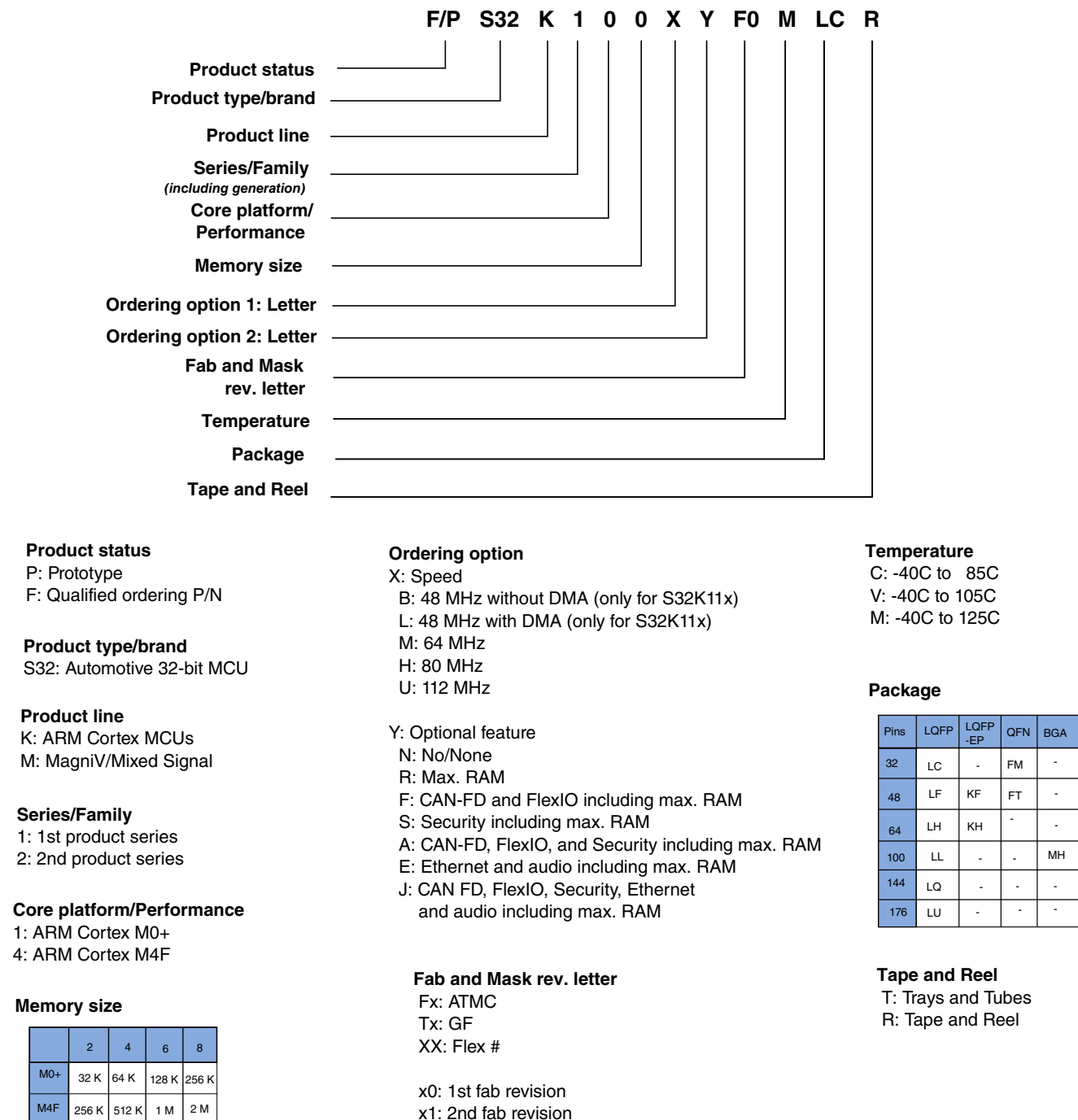


Figure 4. Ordering information

4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP, 100 LQFP, and 100 MAP-BGA packages.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
T_A C-Grade Part	Ambient temperature under bias	-40	—	85 ¹	°C
T_J C-Grade Part	Junction temperature under bias	-40	—	105 ¹	°C
T_A V-Grade Part	Ambient temperature under bias	-40	—	105 ¹	°C
T_J V-Grade Part	Junction temperature under bias	-40	—	125 ¹	°C
T_A M-Grade Part	Ambient temperature under bias	-40	—	125 ²	°C
T_J M-Grade Part	Junction temperature under bias	-40	—	135 ²	°C

1. Values mentioned are measured at ≤ 112 MHz in HSRUN mode.
2. Values mentioned are measured at ≤ 80 MHz in RUN mode.

Table 9. DC electrical specifications at 3.3 V Range (continued)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
Iol_Standard	I/O current sink capability measured when pad = 0.8 V	3	—	—	mA	
Ioh_Strong	I/O current source capability measured when pad = ($V_{DDE} - 0.8$ V)	14	—	—	mA	4
Iol_Strong	I/O current sink capability measured when pad = 0.8 V	12	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at $V_{DD} = 3.3$ V					6
	All pins other than high drive port pins		0.005	0.5	μ A	
	High drive port pins ⁷		0.010	0.5	μ A	
R _{PU}	Internal pullup resistors	20		60	k Ω	8
R _{PD}	Internal pulldown resistors	20		60	k Ω	9

1. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable
3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *S32K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
8. Measured at input $V = V_{SS}$
9. Measured at input $V = V_{DD}$

5.4 DC electrical specifications at 5.0 V Range

Table 10. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	$0.65 \times V_{DD}$	—	$V_{DD} + 0.3$	V	1
V_{il}	Input Buffer Low Voltage	$V_{SS} - 0.3$	—	$0.35 \times V_{DD}$	V	2
V_{hys}	Input Buffer Hysteresis	$0.06 \times V_{DD}$	—	—	V	
Ioh_Standard	I/O current source capability measured when pad = ($V_{DDE} - 0.8$ V)	5	—	—	mA	
Iol_Standard	I/O current sink capability measured when pad = 0.8 V	5	—	—	mA	

Table continues on the next page...

Table 14. Device clock specifications 1 (continued)

Symbol	Description	Min.	Max.	Unit
f _{SYS}	System and core clock	—	48	MHz
f _{BUS}	Bus clock	—	24	MHz
f _{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) ³				
f _{SYS}	System and core clock	—	80	MHz
f _{BUS}	Bus clock	—	40	MHz
f _{FLASH}	Flash clock	—	26.67	MHz
VLPR mode ⁴				
f _{SYS}	System and core clock	—	4	MHz
f _{BUS}	Bus clock	—	4	MHz
f _{FLASH}	Flash clock	—	1	MHz
f _{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section [Feature comparison](#) for the availability of modes and other specifications.
2. Only available on some devices. See section [Feature comparison](#).
3. With SPLP as system clock source.
4. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

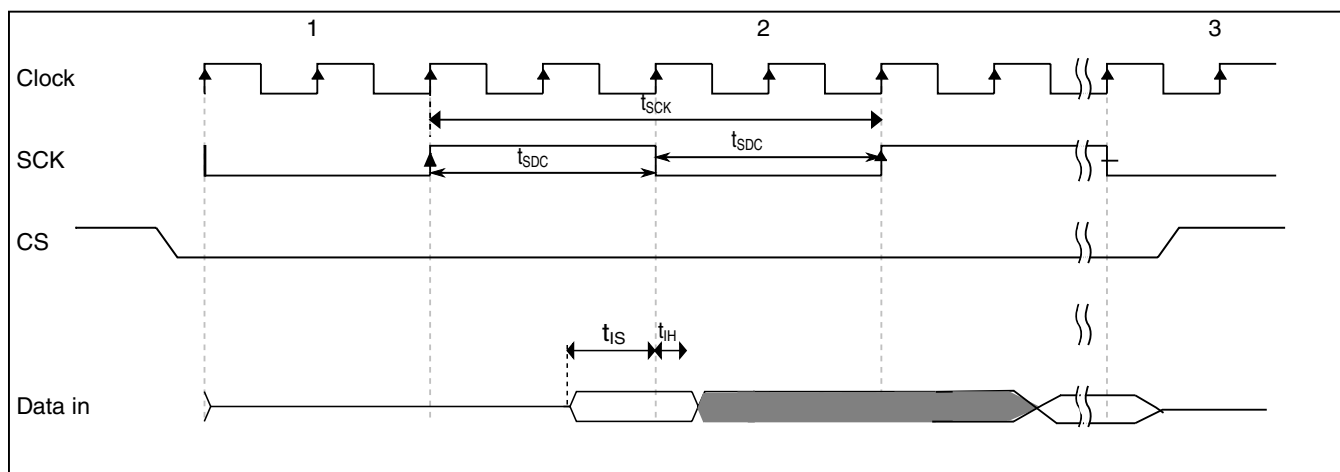


Figure 9. QuadSPI input timing (SDR mode) diagram

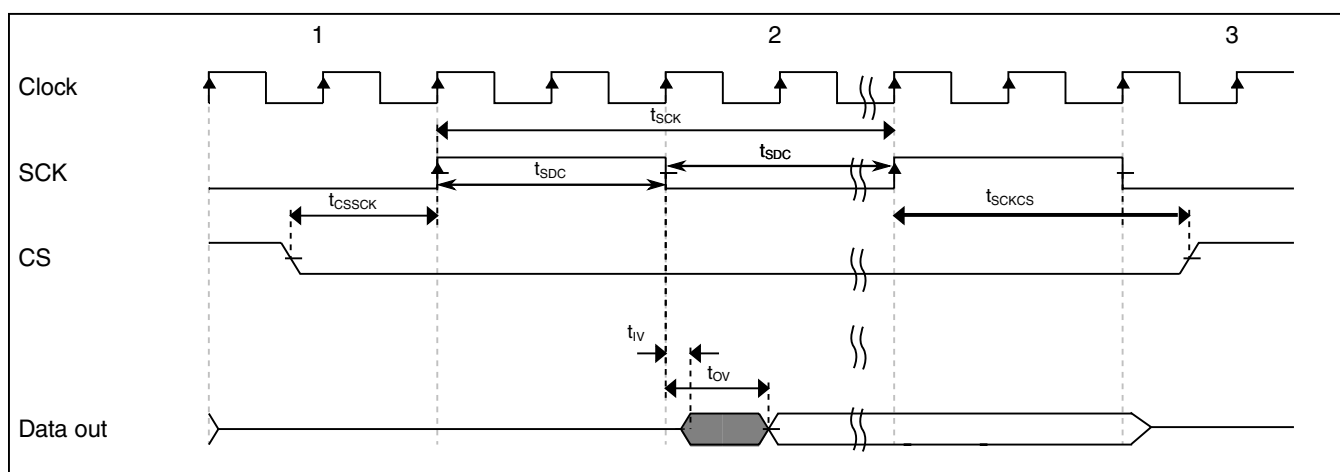


Figure 10. QuadSPI output timing (SDR mode) diagram

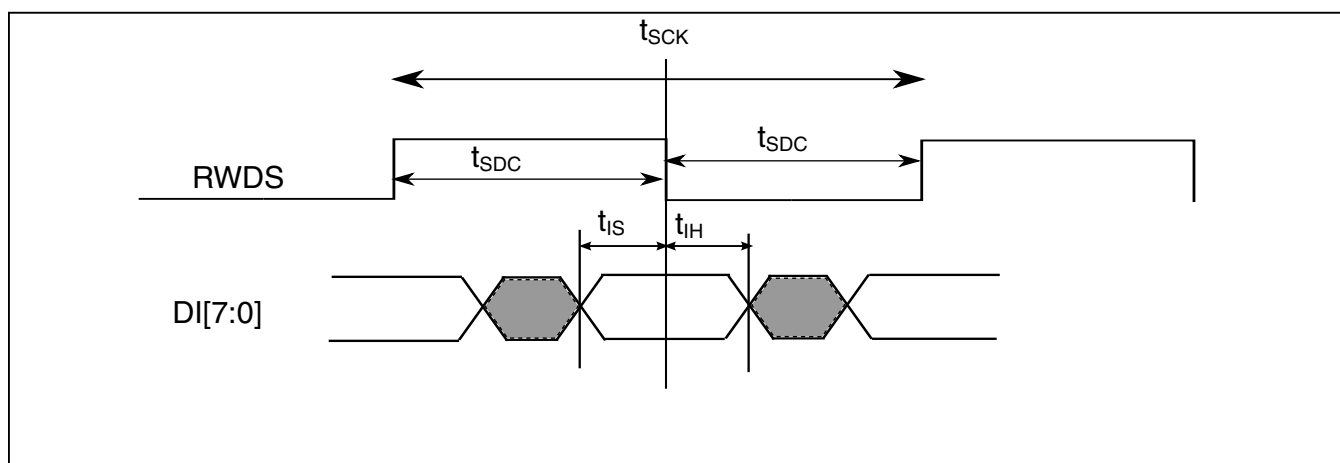


Figure 11. QuadSPI input timing (HyperRAM mode) diagram

Table 26. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
TUE ⁴	Total unadjusted error		—	±4	±8	LSB ⁵	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB ⁵	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB ⁵	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}=V_{DD}$, with the calibration frequency set to half the ADC clock frequency.
2. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 40$ MHz, $R_{AS}=20$ Ω, and $C_{AS}=10$ nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

6.4.2 CMP with 8-bit DAC electrical specifications**Table 28. Comparator with 8-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode ¹				μA
	-40 - 125 °C	—	230	300	
I_{DDL5}	Supply current, Low-speed mode ¹				μA
	-40 - 105 °C	—	5	10	
	-40 - 125 °C		5	13	

Table continues on the next page...

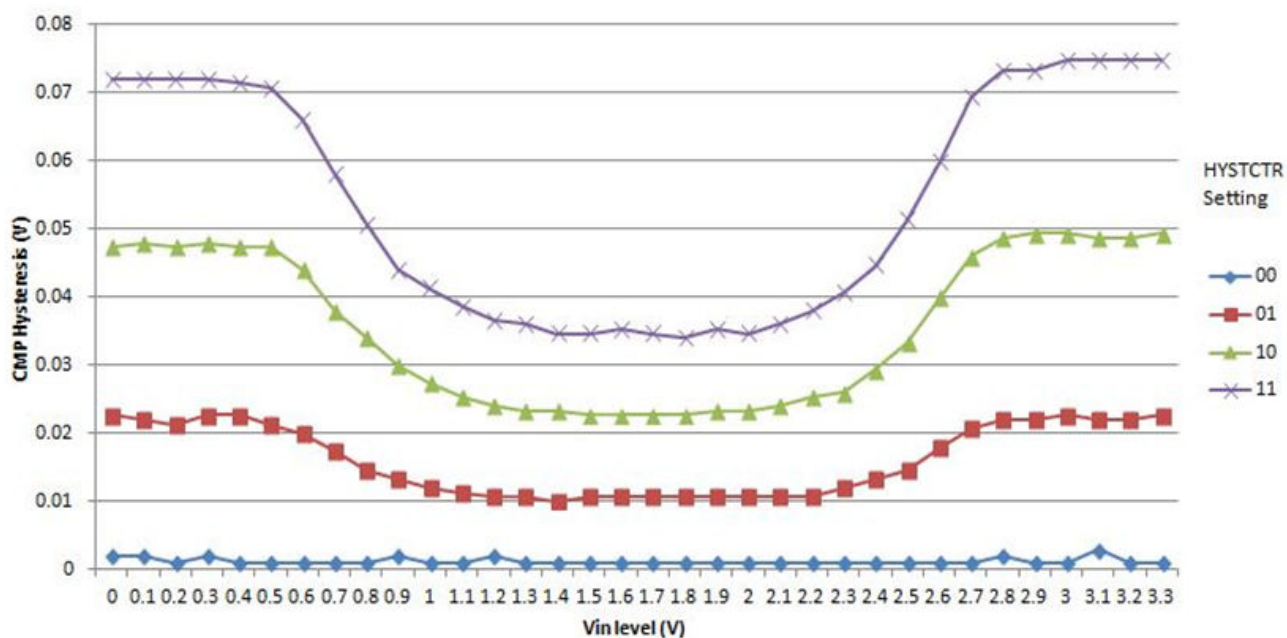


Figure 15. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

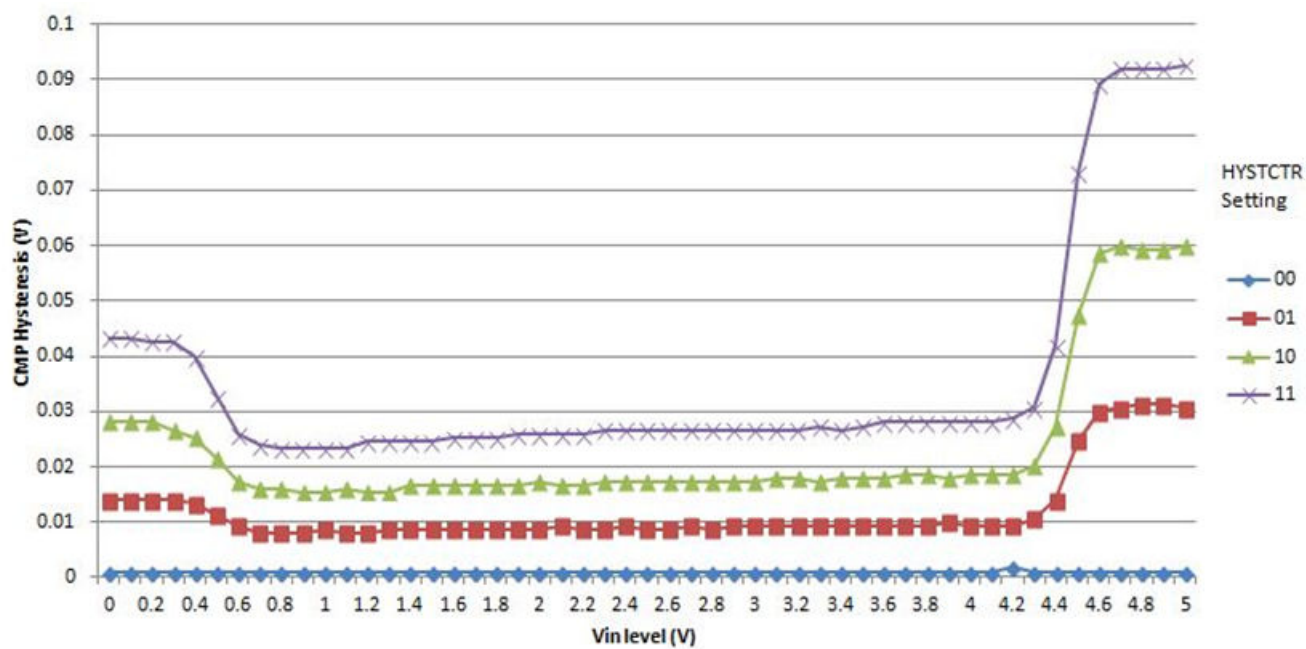


Figure 16. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 0)

Table 29. LPSPI electrical specifications¹

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	f _{periph} ^{3, 4}	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	8	-	8	MHz
			Master	-	40	-	40	-	56	-	56	-	8	-	8	
			Master Loopback ⁵	-	40	-	48	-	48	-	48	-	8	-	8	
			Master Loopback(Slow) ⁶	-	48	-	48	-	48	-	48	-	8	-	8	
1	f _{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14	-	4	-	4	MHz
			Master	-	10	-	10	-	14	-	14	-	4	-	4	
			Master Loopback ⁵	-	20	-	12	-	24	-	12	-	4	-	4	
			Master Loopback(slow) ⁶	-	12	-	12	-	12	-	12	-	4	-	4	
2	t _{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	250	-	250	-	ns
			Master	100	-	100	-	72	-	72	-	250	-	250	-	
			Master Loopback ⁵	50	-	83	-	42	-	83	-	250	-	250	-	
			Master Loopback(slow) ⁶	83	-	83	-	83	-	83	-	250	-	250	-	
3	t _{Lead} ⁷	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	ns	

Table continues on the next page...

Table 29. LPSPI electrical specifications¹ (continued)

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t _v	Data valid (after SPSCK edge)	Slave	-	30	-	39	-	26	-	36	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback ⁵	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow) ⁶	-	8	-	10	-	7	-	9	-	44	-	44	
11	t _{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback ⁵	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	
			Master Loopback(slow) ⁶	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	t _{RI/FI}	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		
			Master Loopback ⁵	-		-		-		-		-		-		
			Master Loopback(slow) ⁶	-		-		-		-		-		-		
13	t _{RO/FO}	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		
			Master Loopback ⁵	-		-		-		-		-		-		
			Master Loopback(slow) ⁶	-		-		-		-		-		-		

- Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
- While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
- f_{periph} = LPSPI peripheral clock

4. $t_{\text{periph}} = 1/f_{\text{periph}}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPi0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPi0.
7. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
8. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.

6.5.4 FlexCAN electrical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

6.5.5 SAI electrical specifications

The following table describes the SAI electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 30. Master mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	—	ns
S4	SAI_BCLK pulse width high/low	45%	55%	BCLK period
S5	SAI_RXD input setup before SAI_BCLK	28	—	ns
S6	SAI_RXD input hold after SAI_BCLK	0	—	ns
S7	SAI_BCLK to SAI_TXD output valid	—	8	ns
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	ns
S9	SAI_FS input setup before SAI_BCLK	28	—	ns
S10	SAI_FS input hold after SAI_BCLK	0	—	ns
S11	SAI_BCLK to SAI_FS output valid	—	8	ns
S12	SAI_BCLK to SAI_FS output invalid	-2	—	ns

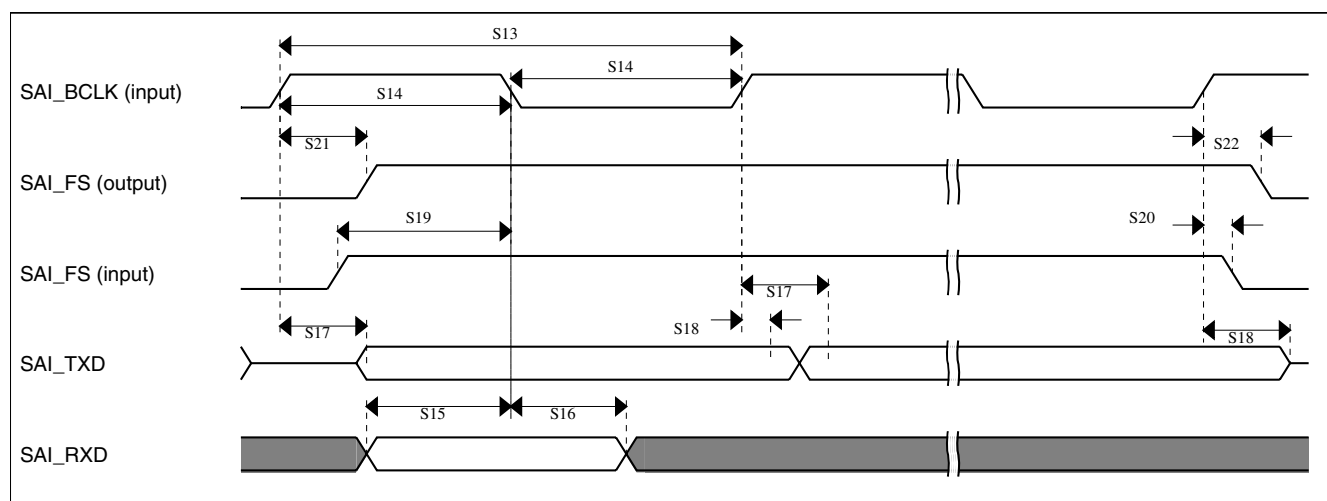


Figure 23. SAI Timing — Slave modes

6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 32. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

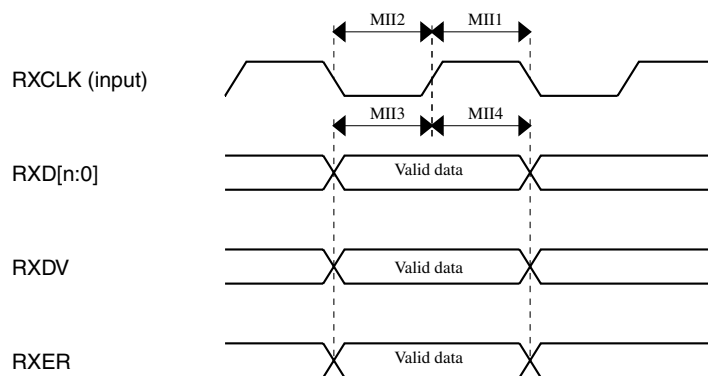


Figure 24. MII receive diagram

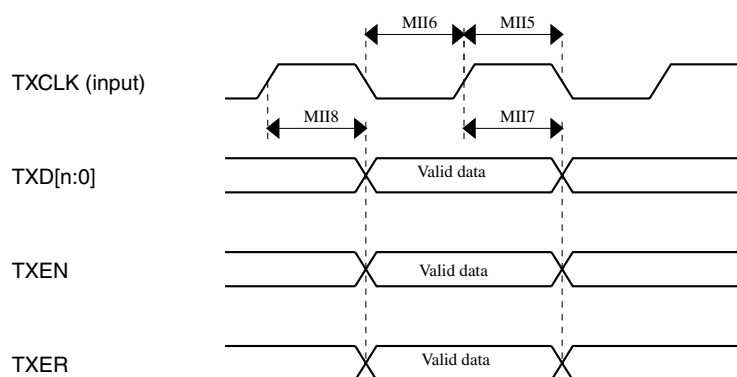


Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 33. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 35. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

Table 38. Thermal characteristics for the 64/100/144/176-pin LQFP package

Rating	Conditions	Symbol	Packages	Values					Unit
				S32K11x	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Single layer board (1s)	$R_{\theta JA}$	64	TBD	61	61	59	NA	°C/W
			100	TBD	53	52	21	NA	°C/W
			144	TBD	NA	NA	51	44	°C/W
			176	TBD	NA	NA	NA	42	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) ¹	Two layer board (1s1p)	$R_{\theta JA}$	64	TBD	45	45	44	NA	°C/W
			100	TBD	42	42	40	NA	°C/W
			144	TBD	NA	NA	44	37	°C/W
			176	TBD	NA	NA	NA	36	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Four layer board (2s2p)	$R_{\theta JA}$	64	TBD	43	43	41	NA	°C/W
			100	TBD	40	40	39	NA	°C/W
			144	TBD	NA	NA	42	36	°C/W
			176	TBD	NA	NA	NA	35	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 3}	Single layer board (1s)	$R_{\theta JMA}$	64	TBD	49	49	48	NA	°C/W
			100	TBD	43	42	41	NA	°C/W
			144	TBD	NA	NA	42	36	°C/W
			176	TBD	NA	NA	NA	34	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ¹	Two layer board (1s1p)	$R_{\theta JMA}$	64	TBD	38	38	37	NA	°C/W
			100	TBD	35	35	34	NA	°C/W
			144	TBD	NA	NA	37	31	°C/W
			176	TBD	NA	NA	NA	30	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 3}	Four layer board (2s2p)	$R_{\theta JMA}$	64	TBD	36	36	35	NA	°C/W
			100	TBD	34	34	33	NA	°C/W
			144	TBD	NA	NA	36	30	°C/W
			176	TBD	NA	NA	NA	29	°C/W
Thermal resistance, Junction to Board ⁴	—	$R_{\theta JB}$	64	TBD	25	25	23	NA	°C/W
			100	TBD	25	25	24	NA	°C/W
			144	TBD	NA	NA	30	24	°C/W
			176	TBD	NA	NA	NA	24	°C/W

Table continues on the next page...

Table 39. Thermal characteristics for the 100 MAPBGA package

Rating	Conditions	Symbol	Values			Unit
			S32K146	S32K144	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Single layer board (1s)	R _{θJA}	57.2	61.0	52.5	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2, 3}	Four layer board (2s2p)	R _{θJA}	32.1	35.6	27.5	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 2, 3}	Single layer board (1s)	R _{θJMA}	44.1	46.6	39.0	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 3}	Two layer board (2s2p)	R _{θJMA}	27.2	30.9	22.8	°C/W
Thermal resistance, Junction to Board ⁴	—	R _{θJB}	15.3	18.9	11.2	°C/W
Thermal resistance, Junction to Case ⁵	—	R _{θJC}	10.2	14.2	7.5	°C/W
Thermal resistance, Junction to Package Top outside center ⁶	—	Ψ _{JT}	0.2	0.4	0.2	°C/W
Thermal resistance, Junction to Package Bottom outside center ⁷	—	Ψ _{JB}	12.2	15.9	18.3	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J , can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 40. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release
2	03 March 2017	- Updated description of QSPI and Clock interfaces in Key Features section - Updated figure: High-level architecture diagram for the S32K1xx family - Updated figure: S32K1xx product series comparison - Added note in section Determining valid orderable parts - Updated figure: Ordering information - In table: Absolute maximum ratings : - Added footnote to I_{INJPAD_DC} - Updated min and max value of I_{INJPAD_DC} - Updated description, max and min values for I_{INJSUM} - Updated $V_{IN_TRANSIENT}$ - In table: Voltage and current operating requirements : - Renamed V_{SUP_OFF} - Updated max value of V_{DD_OFF} - Removed V_{INA} and V_{IN} - Added V_{REFH} and V_{REFL} - Updated footnote "Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V ..." - Removed I_{NJSUM_AF} - Updated footnotes in table Table 4 - Updated section Power mode transition operating behaviors - In table: Power consumption - Added footnote "With PMC_REGSC[CLKBIASDIS] ... " - Updated conditions for VLPR - Removed I_{dd}/MHz for S32K144 - Updated numbers for S32K142 and S32K148 - Removed use case footnotes - In section Modes configuration : - Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes_Master_configuration_sheet' - In table: DC electrical specifications at 3.3 V Range : - Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage - Added footnote to High drive port pins - In table: DC electrical specifications at 5.0 V Range :

Table continues on the next page...

Table 40. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated values for V_{REFH} and V_{REFL} to add reference to the section "voltage and current operating requirements" for Min and Max values - Updated footnote to Typ. - Removed footnote from RAS Analog source resistance - Updated figure: ADC input impedance equivalency diagram - In table: 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Removed rows for V_{TEMP_S} and V_{TEMP25} - Updated footnote to Typ. - In table: 12-bit ADC characteristics (3 V to 5.5 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Removed rows for V_{TEMP_S} and V_{TEMP25} - Removed number for TUE - Updated footnote to Typ. - In table: Comparator with 8-bit DAC electrical specifications - Updated Typ. of I_{DDL5} Supply current, Low-speed mode - Updated Typ. of t_{DLSB} Propagation delay, Low-speed mode - Updated Typ. of t_{DHSS} Propagation delay, High-speed mode - Updated t_{DLSS} Propagation delay - Added row for t_{DDAC} Initialization and switching settling time - Updated footnote - Updated section LPSPi electrical specifications - Added section: SAI electrical specifications - Updated section: Ethernet AC specifications - Added section: Clockout frequency - Added section: Trace electrical specifications - Updated table: Table 38 : Updated numbers for S32K142 and S32K148 - Updated table: Table 39 : Updated numbers for S32K148 - Updated Document number for 32-pin QFN in topic Obtaining package dimensions
3	14 March 2017	- In Table 2 - Updated min. value of V_{DD_OFF} - Added parameter I_{INJSUM_AF} - Updated Power mode transition operating behaviors - Updated Power consumption - Updated footnote to T_{SPLL_LOCK} in SPLL electrical specifications - In 12-bit ADC electrical characteristics - Updated table: 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Added typ. value to I_{DDA_ADC}, TUE, DNL, and INL - Added min. value to SMPLTS - Removed footnote 'All the parameters in this table ... ' - Updated table: 12-bit ADC characteristics (3 V to 5.5 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Added typ. value to I_{DDA_ADC} - Removed footnote 'All the parameters in this table ... ' - In Table 21 updated Max. value of t_{Vfykey} to 33 μs
4	02 June 2017	- In section: Block diagram, added block diagram for S32K11x series. - Updated figure: S32K1xx product series comparison. - In section: Determining valid orderable parts , added reference to attachment S32K_Part_Numbers.xlsx. - In section: Ordering information - Updated figure: Ordering information. - In Table 1,