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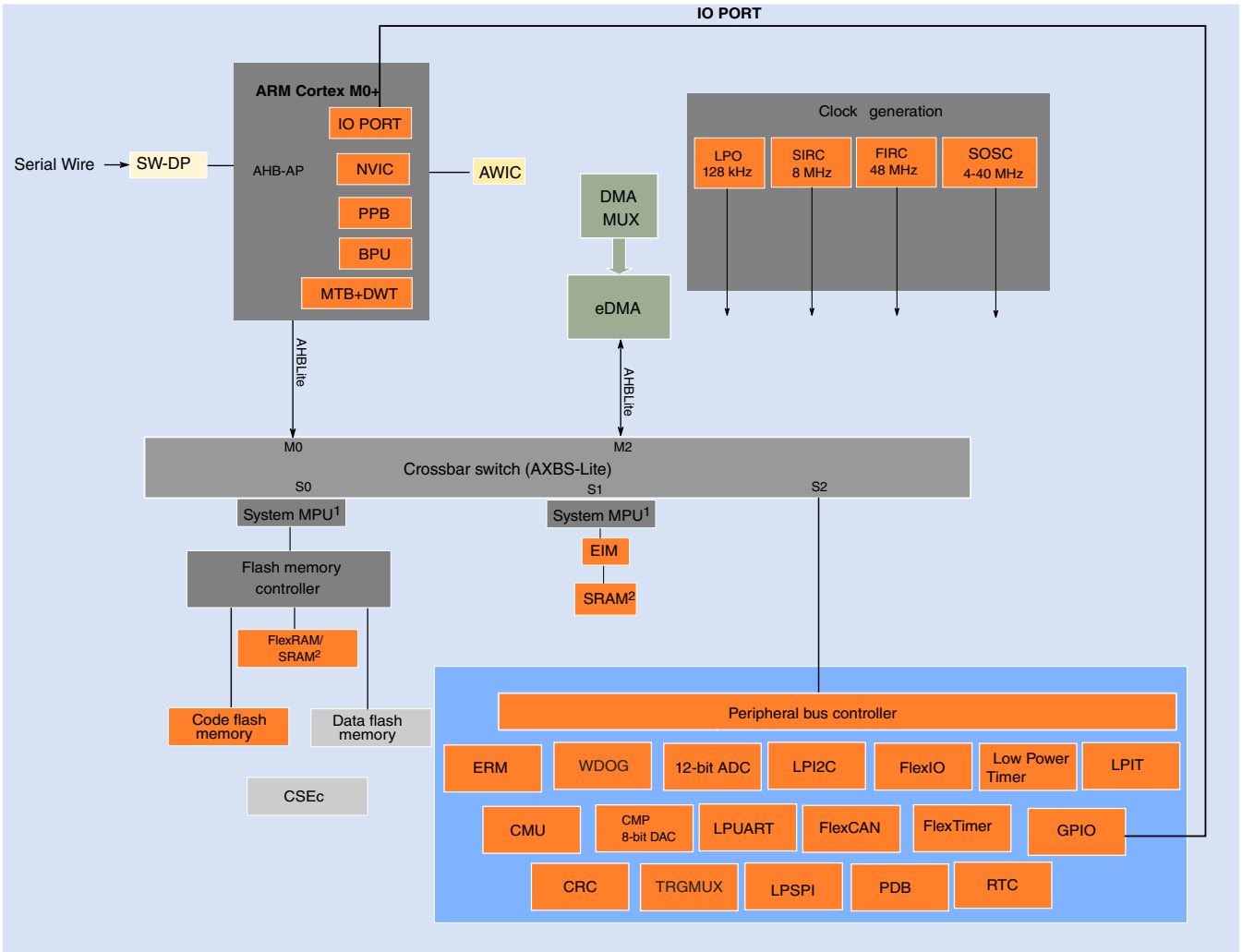
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 112MHz |
| Connectivity | CANbus, I²C, LINbus, SPI, UART/USART |
| Peripherals | DMA, PWM, WDT |
| Number of I/O | - |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/ps32k144uat0vlla |




1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Crossbar master (Core, DMA) can be assigned different access rights to each protected memory region. The ARM M0+ core version in this family does not integrate the ARM Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

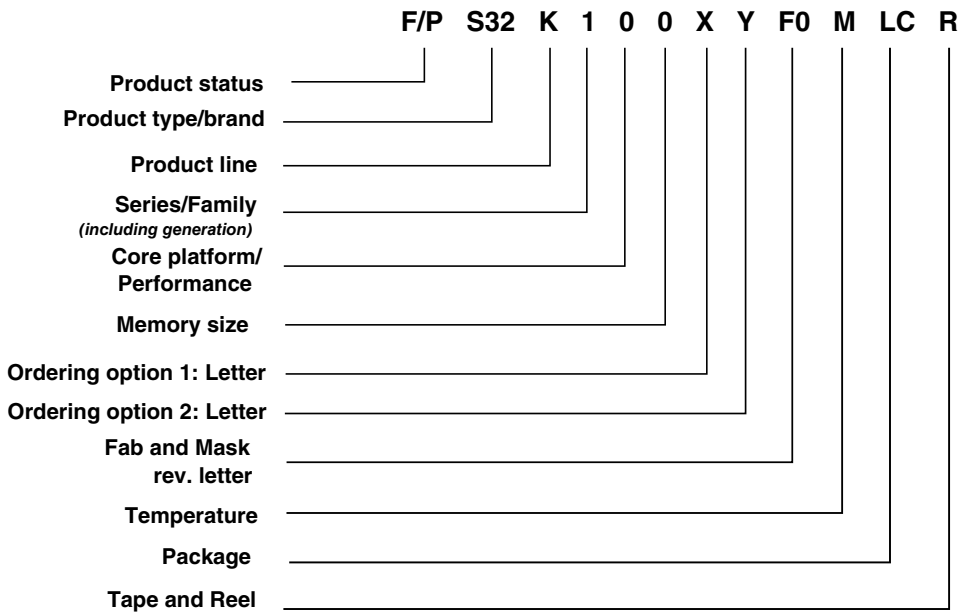
Key:
- Device architectural IP on all S32K devices
- Peripherals present on all S32K devices
- Peripherals present on selected S32K devices (see the "Feature Comparison" section in the RM)

**Figure 2. High-level architecture diagram for the S32K11x family**

# 2 Feature comparison

The following figure summarizes the memory and package options for the S32K product series and demonstrates where this device fits within the overall series. All devices which share a common package are pin-to-pin compatible.

## 3.2 Ordering information




**Product status**
P: Prototype
F: Qualified ordering P/N

**Product type/brand**
S32: Automotive 32-bit MCU

**Product line**
K: ARM Cortex MCUs
M: MagniV/Mixed Signal

**Series/Family**
1: 1st product series
2: 2nd product series

**Core platform/Performance**
1: ARM Cortex M0+
4: ARM Cortex M4F

**Memory size**

| | 2 | 4 | 6 | 8 |
|---|---|---|---|---|
| M0+ | 32 K | 64 K | 128 K | 256 K |
| M4F | 256 K | 512 K | 1 M | 2 M |

**Ordering option**
X: Speed
B: 48 MHz without DMA (only for S32K11x)
L: 48 MHz with DMA (only for S32K11x)
M: 64 MHz
H: 80 MHz
U: 112 MHz

Y: Optional feature
N: No/None
R: Max. RAM
F: CAN-FD and FlexIO including max. RAM
S: Security including max. RAM
A: CAN-FD, FlexIO, and Security including max. RAM
E: Ethernet and audio including max. RAM
J: CAN FD, FlexIO, Security, Ethernet and audio including max. RAM

**Fab and Mask rev. letter**
Fx: ATMC
Tx: GF
XX: Flex #

x0: 1st fab revision
x1: 2nd fab revision

**Temperature**
C: -40C to 85C
V: -40C to 105C
M: -40C to 125C

**Package**

| Pins | LQFP | LQFP -EP | QFN | BGA |
|---|---|---|---|---|
| 32 | LC | - | FM | - |
| 48 | LF | KF | FT | - |
| 64 | LH | KH | - | - |
| 100 | LL | - | - | MH |
| 144 | LQ | - | - | - |
| 176 | LU | - | - | - |

**Tape and Reel**
T: Trays and Tubes
R: Tape and Reel

**Figure 4. Ordering information**

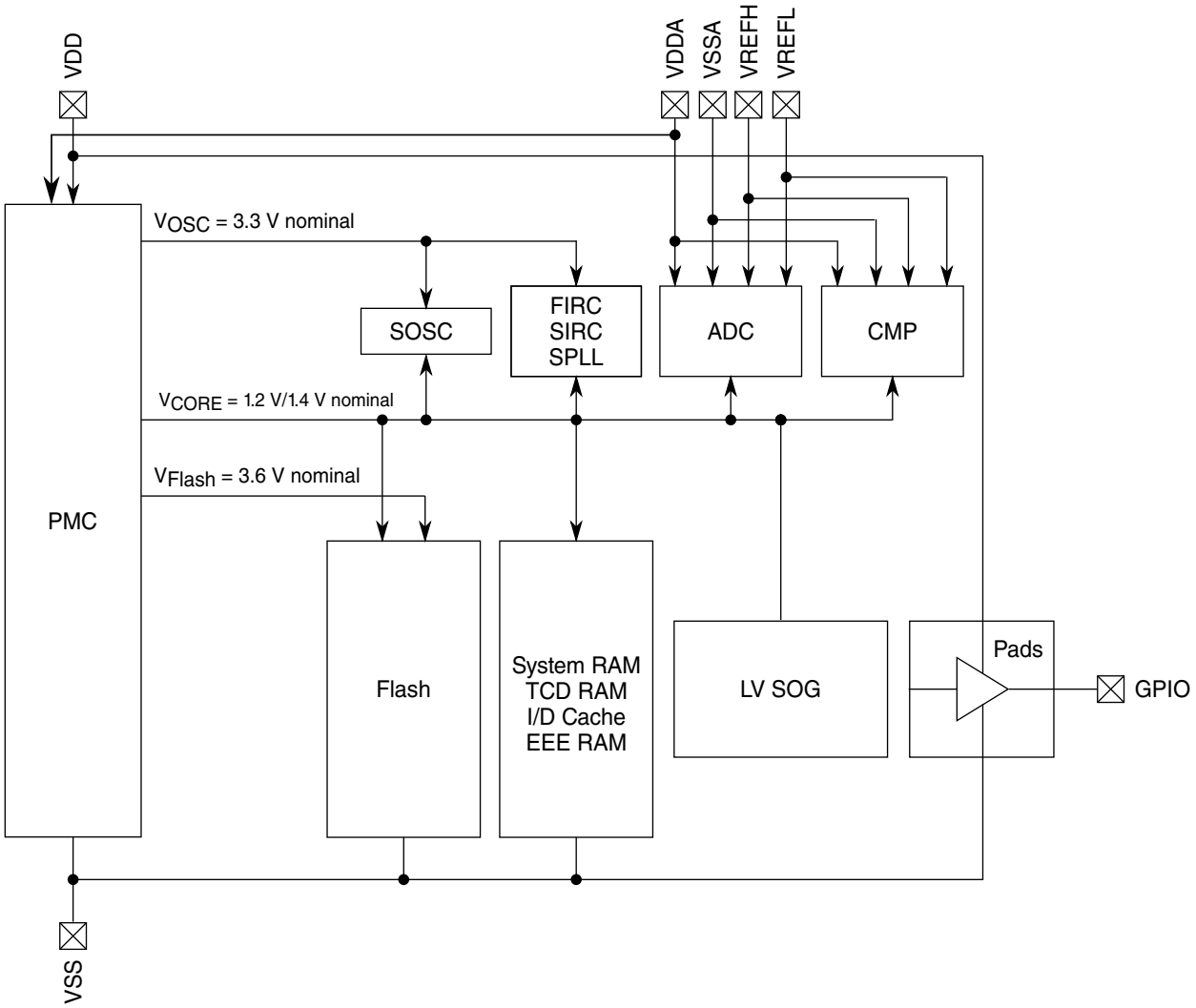
## 4.3 Thermal operating characteristics

**Table 3. Thermal operating characteristics for 64 LQFP, 100 LQFP, and 100 MAP-BGA packages.**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $T_{A\ C\text{-}Grade\ Part}$ | Ambient temperature under bias | –40 | — | 85[1] | ℃ |
| $T_{J\ C\text{-}Grade\ Part}$ | Junction temperature under bias | –40 | — | 105[1] | ℃ |
| $T_{A\ V\text{-}Grade\ Part}$ | Ambient temperature under bias | –40 | — | 105[1] | ℃ |
| $T_{J\ V\text{-}Grade\ Part}$ | Junction temperature under bias | –40 | — | 125[1] | ℃ |
| $T_{A\ M\text{-}Grade\ Part}$ | Ambient temperature under bias | –40 | — | 125[2] | ℃ |
| $T_{J\ M\text{-}Grade\ Part}$ | Junction temperature under bias | –40 | — | 135[2] | ℃ |

1. Values mentioned are measured at ≤ 112 MHz in HSRUN mode.
2. Values mentioned are measured at ≤ 80 MHz in RUN mode.

- No trace exceeding 1 mm from the protection to the trace or to the ground.
- The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
- The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.




*Note: VSSA and VSS are shorted at package level

**Figure 6. Power diagram**

## 4.5 LVR, LVD and POR operating requirements

**Table 5. $V_{DD}$ supply LVR, LVD and POR operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Rising and falling $V_{DD}$ POR detect voltage | 1.1 | 1.6 | 2.0 | V | |
| $V_{LVR}$ | LVR falling threshold (RUN, HSRUN, and STOP modes) | 2.50 | 2.58 | 2.7 | V | |
| $V_{LVR\_HYST}$ | LVR hysteresis | — | 45 | — | mV | 1 |
| $V_{LVR\_LP}$ | LVR falling threshold (VLPS/VLPR modes) | 1.97 | 2.22 | 2.44 | V | |

*Table continues on the next page...*

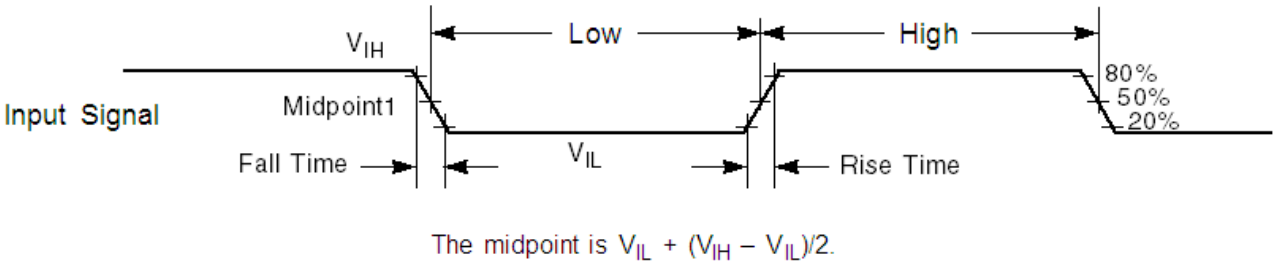



**Figure 7. Input signal measurement reference**

## 5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

**Table 8. General switching specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path | 50 | — | ns | 3 |
| WFRST | $\overline{\text{RESET}}$ input filtered pulse | — | 100 | ns | 4 |
| WFRST | $\overline{\text{RESET}}$ input not filtered pulse | 100 | — | ns | |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter.

## 5.3 DC electrical specifications at 3.3 V Range

**Table 9. DC electrical specifications at 3.3 V Range**

| Symbol | Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | I/O Supply Voltage | 2.7 | 3.3 | 4 | V | 1 |
| $V_{ih}$ | Input Buffer High Voltage | 0.7 × $V_{DD}$ | — | $V_{DD}$ + 0.3 | V | 2 |
| $V_{il}$ | Input Buffer Low Voltage | $V_{SS}$ – 0.3 | — | 0.3 × $V_{DD}$ | V | 3 |
| $V_{hys}$ | Input Buffer Hysteresis | 0.06 × $V_{DD}$ | — | — | V | |
| Ioh_Standard | I/O current source capability measured when pad = ($V_{DDE}$ – 0.8 V) | 3.5 | — | — | mA | |

*Table continues on the next page...*

### Table 9. DC electrical specifications at 3.3 V Range (continued)

| Symbol | Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Iol_Standard | I/O current sink capability measured when pad = 0.8 V | 3 | — | — | mA | |
| Ioh_Strong | I/O current source capability measured when pad = ($V_{DDE}$ – 0.8 V) | 14 | — | — | mA | 4 |
| Iol_Strong | I/O current sink capability measured when pad = 0.8 V | 12 | — | — | mA | 5 |
| IOHT | Output high current total for all ports | — | — | 100 | mA | |
| IIN | Input leakage current (per pin) for full temperature range at $V_{DD}$ = 3.3 V | | | | | 6 |
| | All pins other than high drive port pins | | 0.005 | 0.5 | µA | |
| | High drive port pins [7] | | 0.010 | 0.5 | µA | |
| $R_{PU}$ | Internal pullup resistors | 20 | | 60 | kΩ | 8 |
| $R_{PD}$ | Internal pulldown resistors | 20 | | 60 | kΩ | 9 |

1. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
2. For reset pads, same $V_{ih}$ levels are applicable
3. For reset pads, same $V_{il}$ levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *S32K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
8. Measured at input V = $V_{SS}$
9. Measured at input V = $V_{DD}$

## 5.4 DC electrical specifications at 5.0 V Range

### Table 10. DC electrical specifications at 5.0 V Range

| Symbol | Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | I/O Supply Voltage | 4 | — | 5.5 | V | |
| $V_{ih}$ | Input Buffer High Voltage | 0.65 x $V_{DD}$ | — | $V_{DD}$ + 0.3 | V | 1 |
| $V_{il}$ | Input Buffer Low Voltage | $V_{SS}$ – 0.3 | — | 0.35 x $V_{DD}$ | V | 2 |
| $V_{hys}$ | Input Buffer Hysteresis | 0.06 x $V_{DD}$ | — | — | V | |
| Ioh_Standard | I/O current source capability measured when pad = ($V_{DDE}$ - 0.8 V) | 5 | — | — | mA | |
| Iol_Standard | I/O current sink capability measured when pad = 0.8 V | 5 | — | — | mA | |

*Table continues on the next page...*

**Table 10. DC electrical specifications at 5.0 V Range (continued)**

| Symbol | Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Ioh_Strong | I/O current source capability measured when pad = $V_{DDE}$ - 0.8 V | 20 | — | — | mA | 3, 4 |
| Iol_Strong | I/O current sink capability measured when pad = 0.8 V | 20 | — | — | mA | 4, 5 |
| IOHT | Output high current total for all ports | — | — | 100 | mA | |
| IIN | Input leakage current (per pin) for full temperature range at $V_{DD}$ = 5.5 V | | | | | 6 |
| | All pins other than high drive port pins | | 0.005 | 0.5 | µA | |
| | High drive port pins | | 0.010 | 0.5 | µA | |
| $R_{PU}$ | Internal pullup resistors | 20 | | 50 | kΩ | 7 |
| $R_{PD}$ | Internal pulldown resistors | 20 | | 50 | kΩ | 8 |

1. For reset pads, same $V_{ih}$ levels are applicable
2. For reset pads, same $V_{il}$ levels are applicable
3. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
4. The strong pad I/O pin is capable of switching a 50 pF load at up to 40 MHz.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. Measured at input V = $V_{SS}$
8. Measured at input V = $V_{DD}$

## 5.5 AC electrical specifications at 3.3 V range

**Table 11. AC electrical specifications at 3.3 V Range**

| Symbol | DSE | Rise time (nS) [1] | | Fall time (nS) [1] | | Capacitance (pF) [2] |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| Standard | NA | 4.6 | 14.5 | 3.9 | 15.7 | 25 |
| | | 7.2 | 23.7 | 6.2 | 26.2 | 50 |
| | | 24.0 | 75.4 | 20.8 | 88.4 | 200 |
| Strong | 0 | 4.6 | 14.5 | 3.9 | 15.7 | 25 |
| | | 7.2 | 23.7 | 6.2 | 26.2 | 50 |
| | | 24.0 | 75.4 | 20.8 | 88.4 | 200 |
| | 1 | 2.0 | 5.8 | 1.8 | 6.1 | 25 |
| | | 2.8 | 8.0 | 2.6 | 8.3 | 50 |
| | | 7.0 | 20.7 | 6.0 | 22.4 | 200 |

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

**Table 21. Flash command timing specifications (continued)**

| Symbol | Description[1] | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{eewr16b64k}$ | • 48 KB EEPROM backup<br>• 64 KB EEPROM backup | — | 475 | 2000 | µs | |
| $t_{eewr32bers}$ | 32-bit write to erased FlexRAM location execution time | — | 360 | 2000 | µs | |
| $t_{eewr32b32k}$<br>$t_{eewr32b48k}$<br>$t_{eewr32b64k}$ | 32-bit write to FlexRAM execution time:<br>• 32 KB EEPROM backup<br>• 48 KB EEPROM backup<br>• 64 KB EEPROM backup | —<br>—<br>— | 630<br>720<br>810 | 2000<br>2125<br>2250 | µs<br>µs<br>µs | 3, 4 |
| $t_{quickwr}$ | 32-bit Quick Write execution time : Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write) | | | | | |
| | • 1st 32-bit write<br>• 2nd through Next to Last (Nth-1) 32-bit write<br>• Last (Nth) 32-bit write (time for write only, not cleanup) | —<br>—<br>— | 200<br>150<br>200 | 550<br>550<br>550 | µs<br>µs<br>µs | 5, 6 |
| $t_{quickwrClnup}$ | Quick Write Cleanup execution time | — | — | (Number of Quick Writes) * 2.0 | ms | 7 |

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record clean up has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 'First time' EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. For 'Typ.', only after the Nth write completes will any data will be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power or reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write may take up to 550 µs as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

**NOTE**

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

### 6.3.1.2 Reliability specifications

**Table 22. NVM reliability specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| When using as Program and Data Flash | | | | | | |

*Table continues on the next page...*

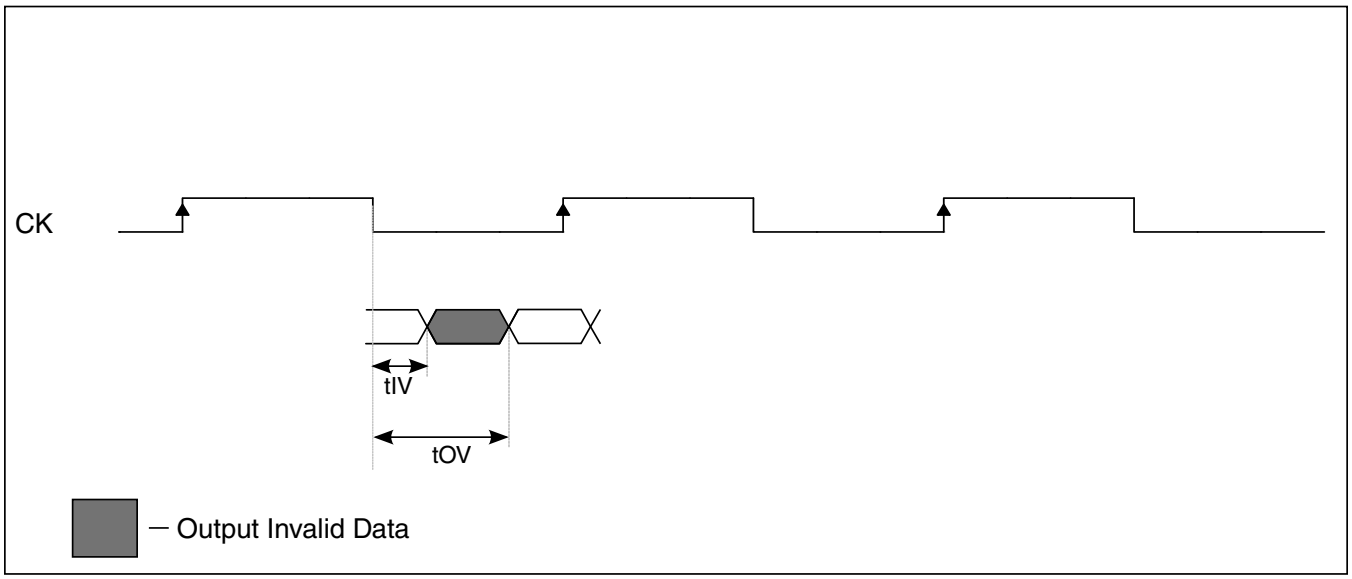



**Figure 12. QuadSPI output timing (HyperRAM mode) diagram**

# 6.4 Analog modules

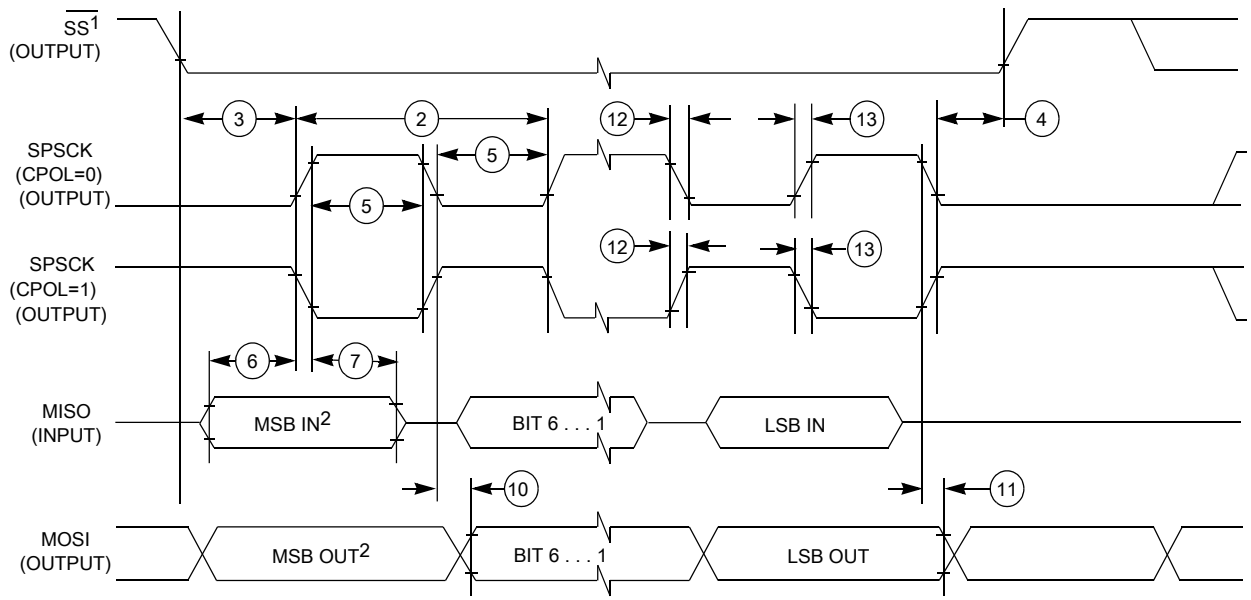
## 6.4.1 ADC electrical specifications

### 6.4.1.1 12-bit ADC operating conditions

**Table 24. 12-bit ADC operating conditions**

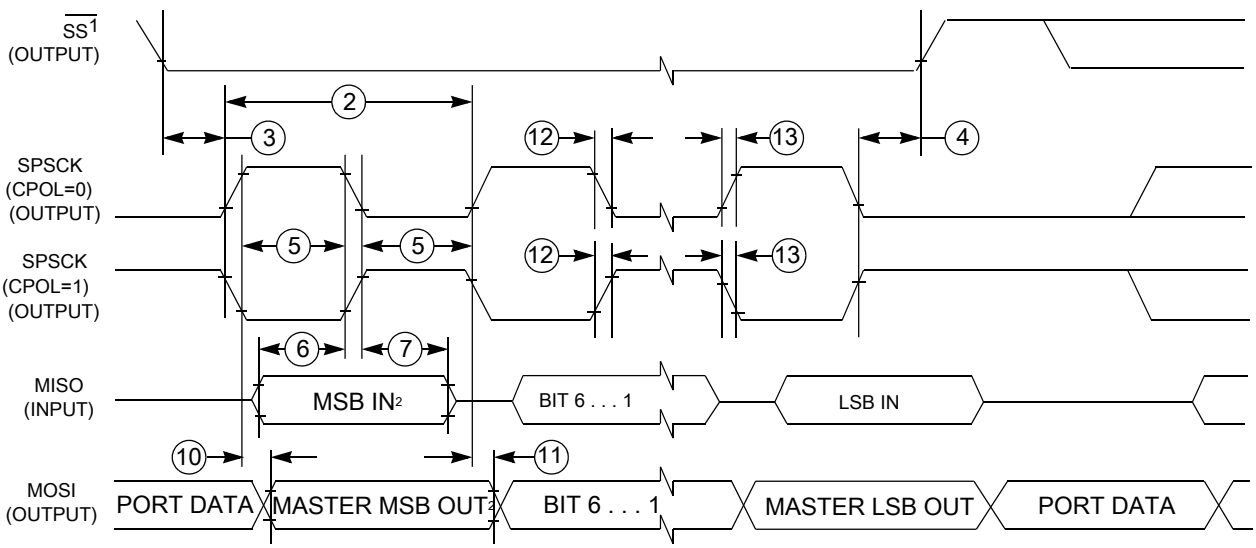
| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$ – $V_{DDA}$) | -0.1 | 0 | +0.1 | V | 2 |
| $V_{REFH}$ | ADC reference voltage high | | See Voltage and current operating requirements for values | $V_{DDA}$ | See Voltage and current operating requirements for values | V | 3 |
| $V_{REFL}$ | ADC reference voltage low | | See Voltage and current operating requirements for values | 0 | See Voltage and current operating requirements for values | mV | 3 |
| $V_{ADIN}$ | Input voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| $R_S$ | Source impedendance | $f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | |
| $R_{SW1}$ | Channel Selection Switch Impedance | | — | -0.75 | 1.2 | kΩ | |
| $R_{AD}$ | Sampling Switch Impedance | | — | 2 | 5 | kΩ | |
| $C_{P1}$ | Pin Capacitance | | — | 10 | — | pF | |

*Table continues on the next page...*




1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 18. LPSPI master mode timing (CPHA = 0)**




1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 19. LPSPI master mode timing (CPHA = 1)**

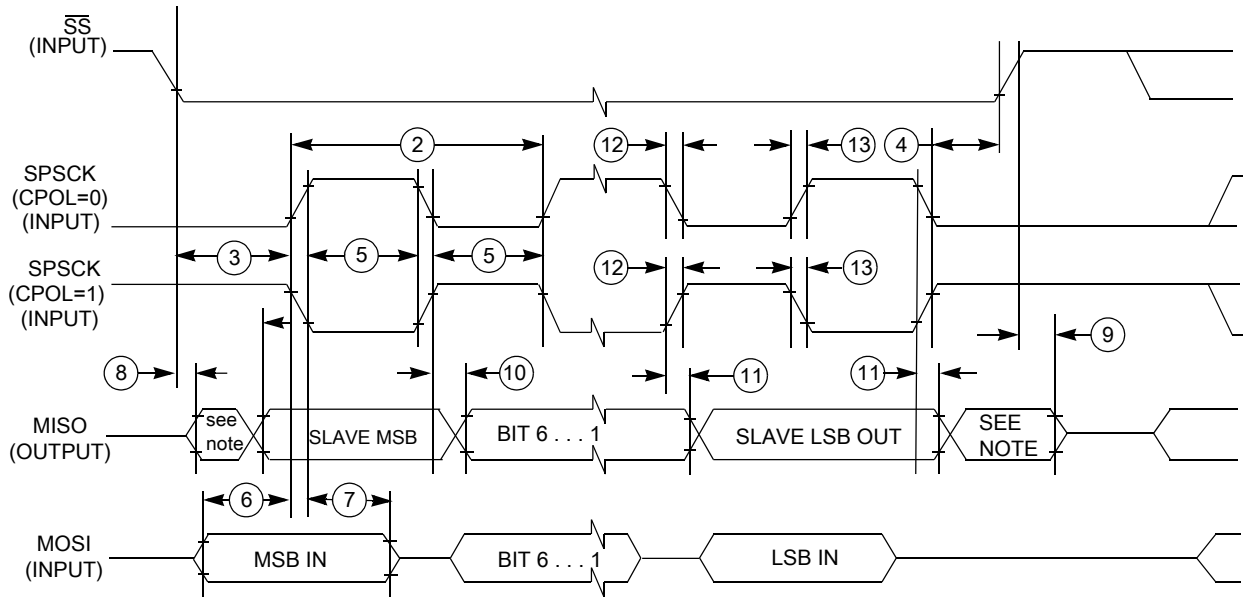



**Figure 20. LPSPI slave mode timing (CPHA = 0)**

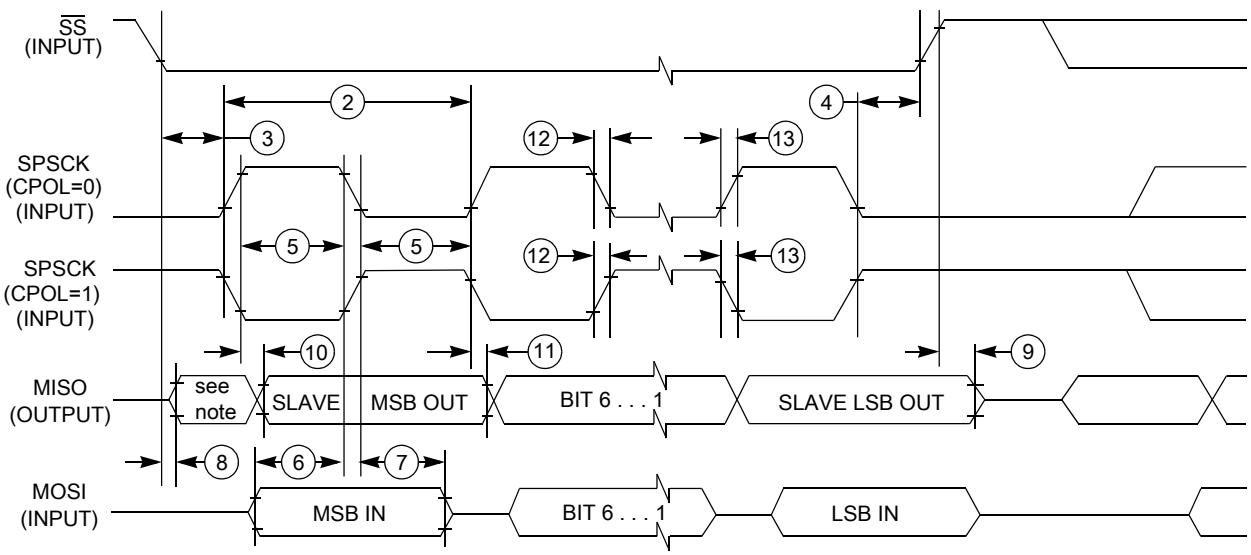



**Figure 21. LPSPI slave mode timing (CPHA = 1)**

## 6.5.3 LPI2C electrical specifications

See General AC specifications for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual.*

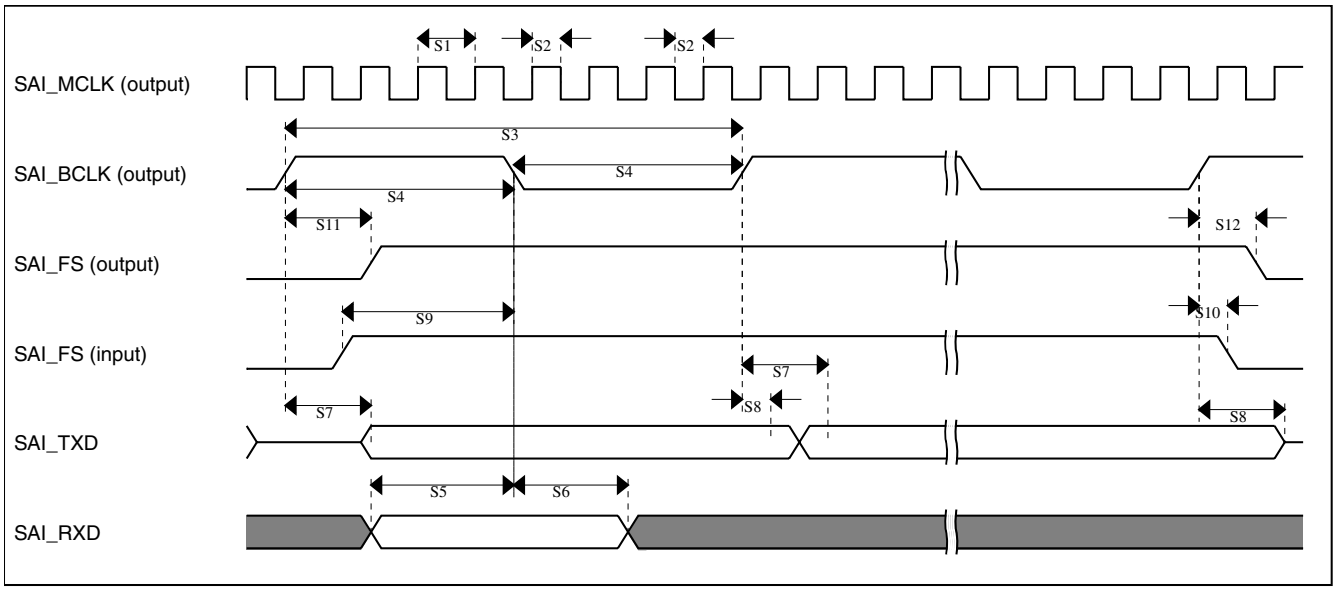



**Figure 22. SAI Timing — Master modes**

## Table 31. Slave mode timing specifications

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | Operating voltage | 2.97 | 3.6 | V |
| S13 | SAI_BCLK cycle time (input) | 80 | — | ns |
| S14[1] | SAI_BCLK pulse width high/low (input) | 45% | 55% | BCLK period |
| S15 | SAI_RXD input setup before SAI_BCLK | 8 | — | ns |
| S16 | SAI_RXD input hold after SAI_BCLK | 2 | — | ns |
| S17 | SAI_BCLK to SAI_TXD output valid | — | 28 | ns |
| S18 | SAI_BCLK to SAI_TXD output invalid | 0 | — | ns |
| S19 | SAI_FS input setup before SAI_BCLK | 8 | — | ns |
| S20 | SAI_FS input hold after SAI_BCLK | 2 | — | ns |
| S21 | SAI_BCLK to SAI_FS output valid | — | 28 | ns |
| S22 | SAI_BCLK to SAI_FS output invalid | 0 | — | ns |

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

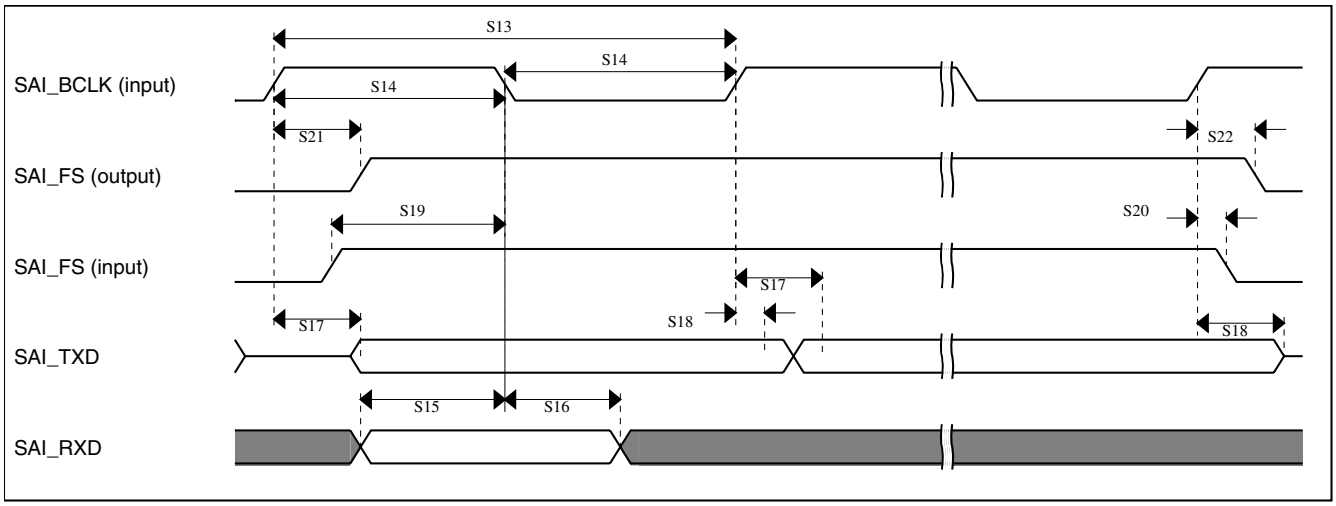



**Figure 23. SAI Timing — Slave modes**

## 6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN ), the interface should be OFF.

**Table 32. MII signal switching specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | RXCLK frequency | — | 25 | MHz |
| MII1 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| MII2 | RXCLK pulse width low | 35% | 65% | RXCLK period |
| MII3 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| MII4 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| — | TXCLK frequency | — | 25 | MHz |
| MII5 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| MII6 | TXCLK pulse width low | 35% | 65% | TXCLK period |
| MII7 | TXCLK to TXD[3:0], TXEN, TXER invalid | 2 | — | ns |
| MII8 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |

**Table 33. RMII signal switching specifications (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| RMII7 | RMII_CLK to TXD[1:0], TXEN invalid | 2 | — | ns |
| RMII8 | RMII_CLK to TXD[1:0], TXEN valid | — | 15 | ns |

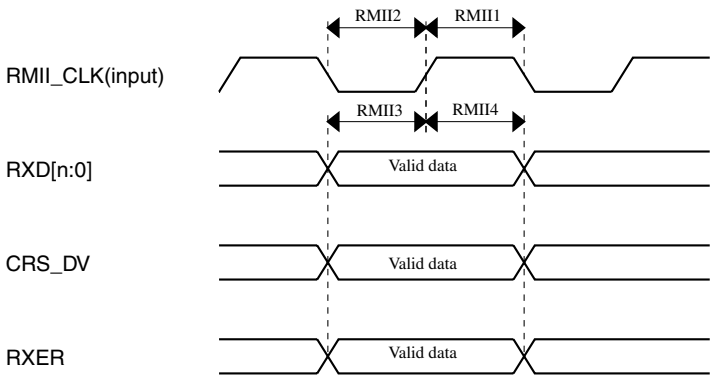



**Figure 26. RMII receive diagram**

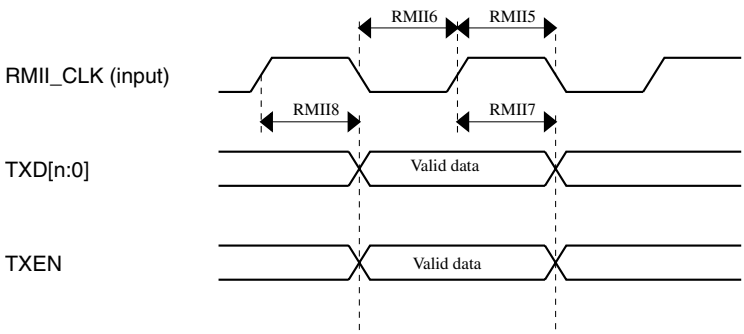



**Figure 27. RMII transmit diagram**

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN ), the interface should be OFF.
- MDIO pin must have external Pull-up.

**Table 34. MDIO timing specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | MDC Clock Frequency | — | 2.5 | MHz |

*Table continues on the next page...*

**Table 34. MDIO timing specifications (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| MDC1 | MDC pulse width high | 40% | 60% | MDC period |
| MDC2 | MDC pulse width low | 40% | 60% | MDC period |
| MDC3 | MDIO (input) to MDC rising edge setup | 25 | — | ns |
| MDC4 | MDIO (input) to MDC rising edge hold | 0 | — | ns |
| MDC5 | MDC falling edge to MDIO output valid (maximum propagation delay) | — | 25 | ns |
| MDC6 | MDC falling edge to MDIO output invalid (minimum propagation delay) | -10 | — | ns |

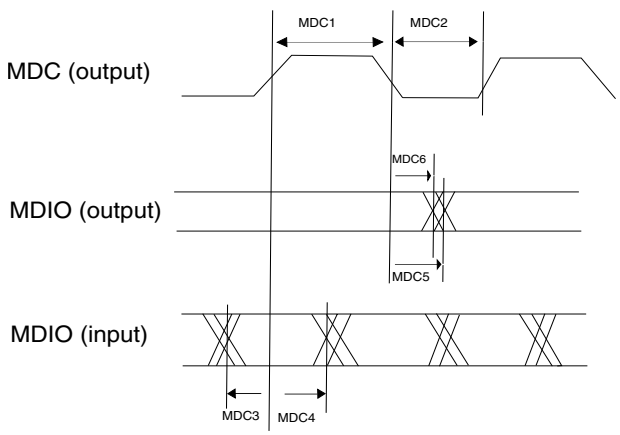



**Figure 28. MII/RMII serial management channel timing diagram**

### 6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

## 6.6 Debug modules

### 6.6.1 SWD electrical specofications

## Table 35. SWD electrical specifications

| Symbol | Description | Run Mode | | | | HSRUN Mode | | | | VLPR Mode | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| S1 | SWD_CLK frequency of operation | - | 25 | - | 25 | - | 25 | - | 25 | - | 10 | - | 10 | MHz |
| S2 | SWD_CLK cycle period | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | ns |
| S3 | SWD_CLK clock pulse width | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | ns |
| S4 | SWD_CLK rise and fall times | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | ns |
| S9 | SWD_DIO input data setup time to SWD_CLK rise | 4 | - | 4 | - | 4 | - | 4 | - | 16 | - | 16 | - | ns |
| S10 | SWD_DIO input data hold time after SWD_CLK rise | 3 | - | 3 | - | 3 | - | 3 | - | 10 | - | 10 | - | ns |
| S11 | SWD_CLK high to SWD_DIO data valid | - | 28 | - | 38 | - | 28 | - | 38 | - | 70 | - | 77 | ns |
| S12 | SWD_CLK high to SWD_DIO high-Z | - | 28 | - | 38 | - | 28 | - | 38 | - | 70 | - | 77 | ns |
| S13 | SWD_CLK high to SWD_DIO data invalid | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns |

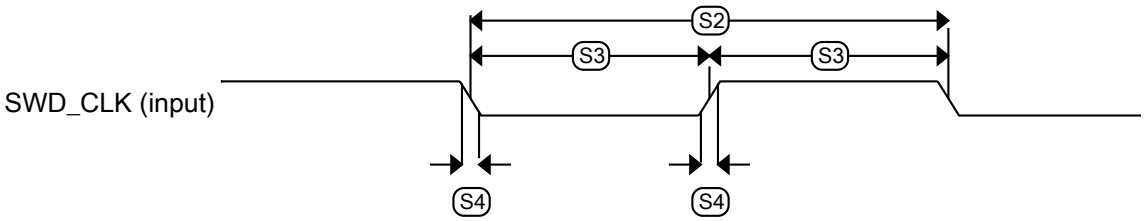



**Figure 29. Serial wire clock input timing**

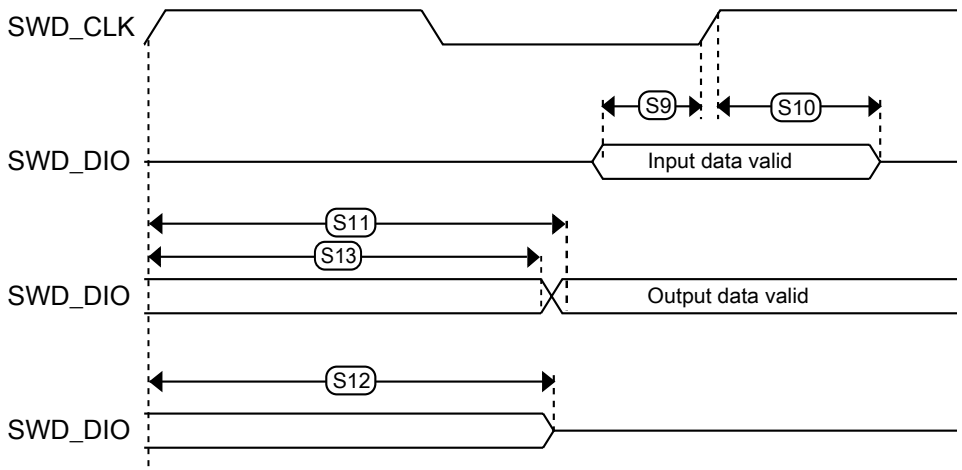



**Figure 30. Serial wire data timing**

## 6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN ), the interface should be OFF.

**Table 36. Trace specifications**

| | Symbol | Description | RUN Mode | | | HSRUN Mode | | VLPR Mode | Unit |
|---|---|---|---|---|---|---|---|---|---|
| — | Fsys | System frequency | 80 | 48 | 40 | 112 | 80 | 4 | MHz |

*Table continues on the next page...*

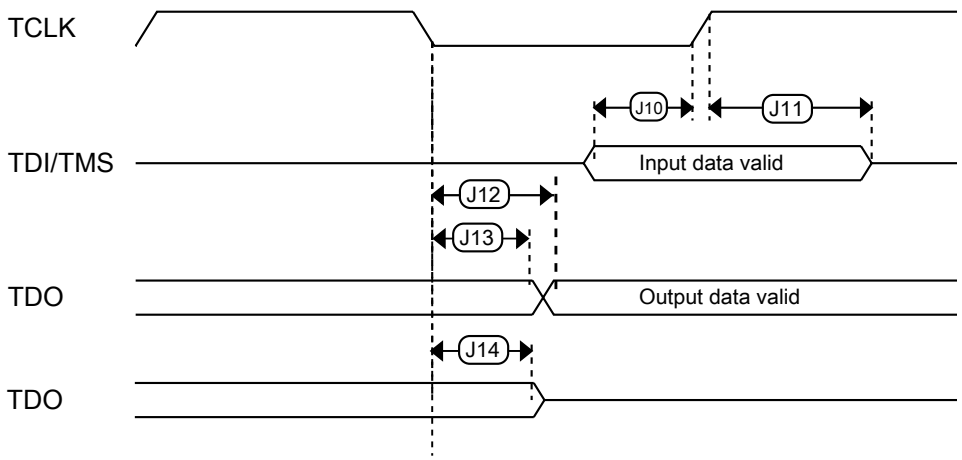



**Figure 34. Test Access Port timing**

# 7 Thermal attributes

## 7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

**NOTE**

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

## 7.2 Thermal characteristics

## Table 38. Thermal characteristics for the 64/100/144/176-pin LQFP package

| Rating | Conditions | Symbol | Packages | Values | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | S32K11x | S32K142 | S32K144 | S32K146 | S32K148 | |
| Thermal resistance, Junction to Ambient (Natural Convection)[1, 2] | Single layer board (1s) | $R_{\theta JA}$ | 64 | TBD | 61 | 61 | 59 | NA | °C/W |
| | | | 100 | TBD | 53 | 52 | 21 | NA | °C/W |
| | | | 144 | TBD | NA | NA | 51 | 44 | °C/W |
| | | | 176 | TBD | NA | NA | NA | 42 | °C/W |
| Thermal resistance, Junction to Ambient (Natural Convection)[1] | Two layer board (1s1p) | $R_{\theta JA}$ | 64 | TBD | 45 | 45 | 44 | NA | °C/W |
| | | | 100 | TBD | 42 | 42 | 40 | NA | °C/W |
| | | | 144 | TBD | NA | NA | 44 | 37 | °C/W |
| | | | 176 | TBD | NA | NA | NA | 36 | °C/W |
| Thermal resistance, Junction to Ambient (Natural Convection)[1, 2] | Four layer board (2s2p) | $R_{\theta JA}$ | 64 | TBD | 43 | 43 | 41 | NA | °C/W |
| | | | 100 | TBD | 40 | 40 | 39 | NA | °C/W |
| | | | 144 | TBD | NA | NA | 42 | 36 | °C/W |
| | | | 176 | TBD | NA | NA | NA | 35 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3] | Single layer board (1s) | $R_{\theta JMA}$ | 64 | TBD | 49 | 49 | 48 | NA | °C/W |
| | | | 100 | TBD | 43 | 42 | 41 | NA | °C/W |
| | | | 144 | TBD | NA | NA | 42 | 36 | °C/W |
| | | | 176 | TBD | NA | NA | NA | 34 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1] | Two layer board (1s1p) | $R_{\theta JMA}$ | 64 | TBD | 38 | 38 | 37 | NA | °C/W |
| | | | 100 | TBD | 35 | 35 | 34 | NA | °C/W |
| | | | 144 | TBD | NA | NA | 37 | 31 | °C/W |
| | | | 176 | TBD | NA | NA | NA | 30 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3] | Four layer board (2s2p) | $R_{\theta JMA}$ | 64 | TBD | 36 | 36 | 35 | NA | °C/W |
| | | | 100 | TBD | 34 | 34 | 33 | NA | °C/W |
| | | | 144 | TBD | NA | NA | 36 | 30 | °C/W |
| | | | 176 | TBD | NA | NA | NA | 29 | °C/W |
| Thermal resistance, Junction to Board[4] | — | $R_{\theta JB}$ | 64 | TBD | 25 | 25 | 23 | NA | °C/W |
| | | | 100 | TBD | 25 | 25 | 24 | NA | °C/W |
| | | | 144 | TBD | NA | NA | 30 | 24 | °C/W |
| | | | 176 | TBD | NA | NA | NA | 24 | °C/W |

*Table continues on the next page...*

## Table 39. Thermal characteristics for the 100 MAPBGA package

| Rating | Conditions | Symbol | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | S32K146 | S32K144 | S32K148 | |
| Thermal resistance, Junction to Ambient (Natural Convection) [1, 2] | Single layer board (1s) | $R_{\theta JA}$ | 57.2 | 61.0 | 52.5 | °C/W |
| Thermal resistance, Junction to Ambient (Natural Convection) [1, 2, 3] | Four layer board (2s2p) | $R_{\theta JA}$ | 32.1 | 35.6 | 27.5 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min) [1, 2, 3] | Single layer board (1s) | $R_{\theta JMA}$ | 44.1 | 46.6 | 39.0 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3] | Two layer board (2s2p) | $R_{\theta JMA}$ | 27.2 | 30.9 | 22.8 | °C/W |
| Thermal resistance, Junction to Board[4] | — | $R_{\theta JB}$ | 15.3 | 18.9 | 11.2 | °C/W |
| Thermal resistance, Junction to Case [5] | — | $R_{\theta JC}$ | 10.2 | 14.2 | 7.5 | °C/W |
| Thermal resistance, Junction to Package Top outside center[6] | — | $\Psi_{JT}$ | 0.2 | 0.4 | 0.2 | °C/W |
| Thermal resistance, Junction to Package Bottom outside center[7] | — | $\Psi_{JB}$ | 12.2 | 15.9 | 18.3 | °C/W |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.