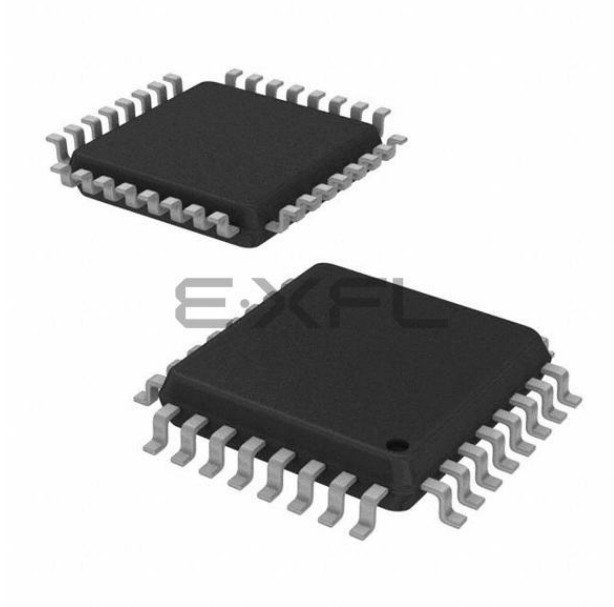

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	29
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1008 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f334kpmc-g-sne2

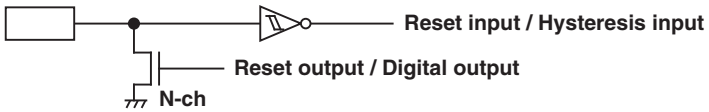
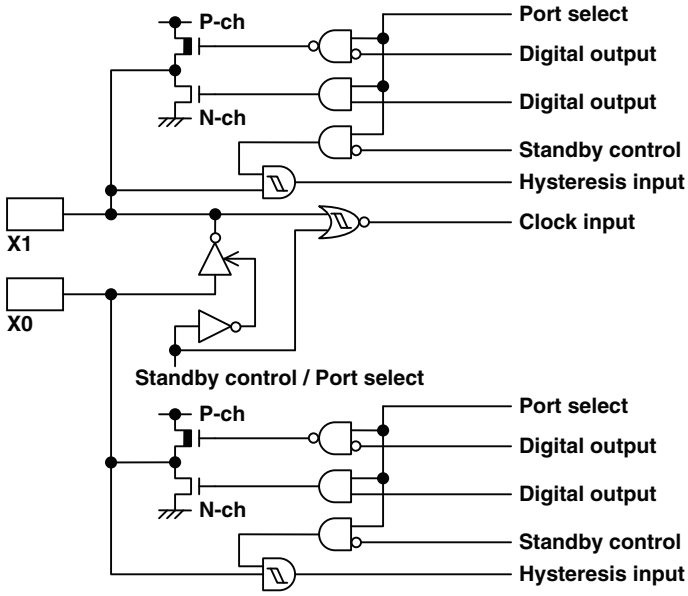
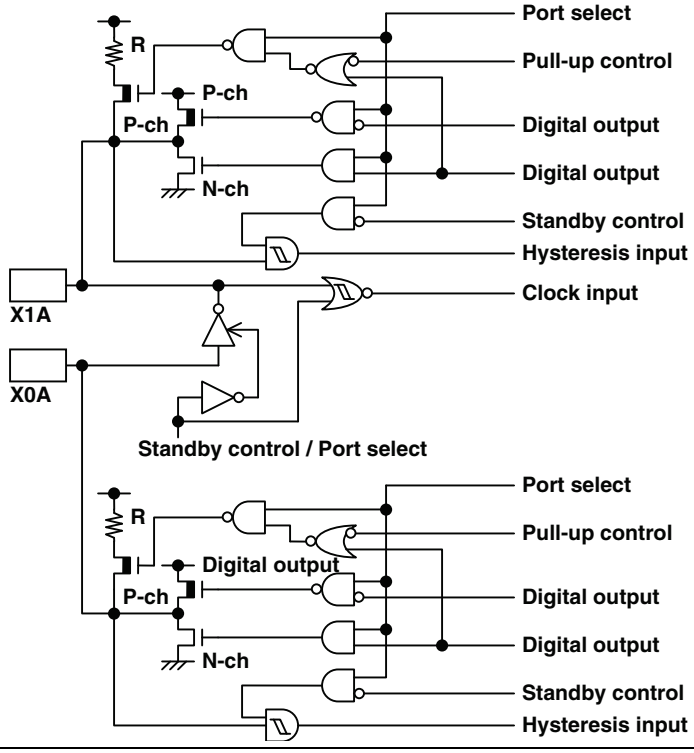
(Continued)

Part number / Parameter	MB95F332H	MB95F333H	MB95F334H	MB95F332K	MB95F333K	MB95F334K
UART/SIO	1 channel					
	Data transfer with UART/SIO is enabled. It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. It uses the NRZ type transfer format. LSB-first data transfer and MSB-first data transfer are available to use. Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
I^2C	1 channel					
	Master/slave transmission and receiving It has a bus error function, an arbitration function, a transmission direction detection function and a wake-up function. It also has functions of generating and detecting repeated START conditions.					
8/16-bit PPG	3 channels					
	Each channel of PPG can be used as two 8-bit PPG channels or a single 16-bit PPG channel. The counter operating clock can be selected from eight clock sources.					
16-bit PPG	PWM mode and one-shot mode are available to use. The counter operating clock can be selected from eight clock sources. It supports external trigger start. It can work independently or together with the multi-pulse generator.					
16-bit reload timer	Two clock modes and two counter operating modes are available to use. It can output square waveform. Count clock: it can be selected from internal clocks (seven types) and external clocks. Two counter operating modes: reload mode and one-shot mode It can work independently or together with the multi-pulse generator.					
Multi-pulse generator (for DC motor control)	16-bit PPG timer: 1 channel 16-bit reload timer operations: toggle output, one-shot output Event counter: 1 channel Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	It supports automatic programming, Embedded Algorithm, and write/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of write/erase cycles: 100000 Data retention time: 20 years Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-32P-M30 DIP-32P-M06 LCC-32P-M19					

Pin no.		Pin name	I/O circuit type*4	Function
LQFP32*1 & QFN32*2	SH-DIP32*3			
10	14	P62	D	General-purpose I/O port High-current pin
		TO10		8/16-bit composite timer ch. 1 output pin
		PPG00		8/16-bit PPG ch. 0 output pin
		OPT0		MPG waveform sequencer output pin
11	15	P61	I	General-purpose I/O port
		INT09		External interrupt input pin
		SCL		I^2C clock I/O pin
		TI1		16-bit reload timer ch. 1 input pin
12	16	P60	I	General-purpose I/O port
		INT08		External interrupt input pin
		SDA		I^2C data I/O pin
		DTTI		MPG waveform sequencer input pin
13	17	P00	E	General-purpose I/O port
		INT00		External interrupt input pin
		AN00		A/D converter analog input pin
14	18	P01	E	General-purpose I/O port
		INT01		External interrupt input pin
		AN01		A/D converter analog input pin
15	19	P02	E	General-purpose I/O port
		INT02		External interrupt input pin
		AN02		A/D converter analog input pin
		SCK		LIN-UART clock I/O pin
16	20	P03	E	General-purpose I/O port
		INT03		External interrupt input pin
		AN03		A/D converter analog input pin
		SOT		LIN-UART data output pin
17	21	P04	F	General-purpose I/O port
		INT04		External interrupt input pin
		AN04		A/D converter analog input pin
		SIN		LIN-UART data input pin
		HCLK1		External clock input pin
		EC0		8/16-bit composite timer ch. 0 clock input pin

(Continued)

6. I/O Circuit Type

Type	Circuit	Remarks
A		■ N-ch open drain output ■ Hysteresis input ■ Reset output
B		■ Oscillation circuit ■ High-speed side Feedback resistance: approx. 1 MΩ ■ CMOS output ■ Hysteresis input
C		■ Oscillation circuit ■ Low-speed side Feedback resistance: approx.10 MΩ ■ CMOS output ■ Hysteresis input ■ Pull-up control available

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$	PPS01	8/16-bit PPG01 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9D_H$	PPS00	8/16-bit PPG00 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9E_H$	PDS01	8/16-bit PPG01 duty setting buffer register ch. 0	R/W	11111111_B
$0F9F_H$	PDS00	8/16-bit PPG00 duty setting buffer register ch. 0	R/W	11111111_B
$0FA0_H$	PPS11	8/16-bit PPG11 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA1_H$	PPS10	8/16-bit PPG10 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA2_H$	PDS11	8/16-bit PPG11 duty setting buffer register ch. 1	R/W	11111111_B
$0FA3_H$	PDS10	8/16-bit PPG10 duty setting buffer register ch. 1	R/W	11111111_B
$0FA4_H$	PPGS	8/16-bit PPG startup register	R/W	00000000_B
$0FA5_H$	REVC	8/16-bit PPG output reverse register	R/W	00000000_B
$0FA6_H$	PPS21	8/16-bit PPG21 cycle setting buffer register ch. 2	R/W	11111111_B
$0FA7_H$	PPS20	8/16-bit PPG20 cycle setting buffer register ch. 2	R/W	11111111_B
$0FA8_H$	TMRH1	16-bit timer register (upper) ch. 1	R/W	00000000_B
	TMRLRH1	16-bit reload register (upper) ch. 1		
$0FA9_H$	TMRL1	16-bit timer register (lower) ch. 1	R/W	00000000_B
	TMRLRL1	16-bit reload register (lower) ch. 1		
$0FAA_H$	PDS21	8/16-bit PPG21 duty setting buffer register ch. 2	R/W	11111111_B
$0FAB_H$	PDS20	8/16-bit PPG20 duty setting buffer register ch. 2	R/W	11111111_B
$0FAC_H$ to $0FAF_H$	—	(Disabled)	—	—
$0FB0_H$	PDCRH1	16-bit PPG down counter register (upper) ch. 1	R	00000000_B
$0FB1_H$	PDCRL1	16-bit PPG down counter register (lower) ch. 1	R	00000000_B
$0FB2_H$	PCSRH1	16-bit PPG cycle setting buffer register (upper) ch. 1	R/W	11111111_B
$0FB3_H$	PCSRL1	16-bit PPG cycle setting buffer register (lower) ch. 1	R/W	11111111_B
$0FB4_H$	PDUTH1	16-bit PPG duty setting buffer register (upper) ch. 1	R/W	11111111_B
$0FB5_H$	PDUTL1	16-bit PPG duty setting buffer register (lower) ch. 1	R/W	11111111_B

(Continued)

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P62 to P67
	I_{OL2}		15		P62 to P67
"L" level average current	I_{OLAV1}	—	4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}	—	12		P62 to P67 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	−15	mA	Other than P62 to P67
	I_{OH2}	—	−15		P62 to P67
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}	—	−8		P62 to P67 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	Tstg	−55	+150	°C	

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Flash memory product (except writing and erasing)
				—	20.5	26.5	mA	Flash memory product (at writing and erasing)
				—	15	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25°C	—	65	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	—	10	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	5	30	µA	
	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode	—	10	13.2	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (divided by 2) T_A = +25°C	—	110	410	µA	

(Continued)

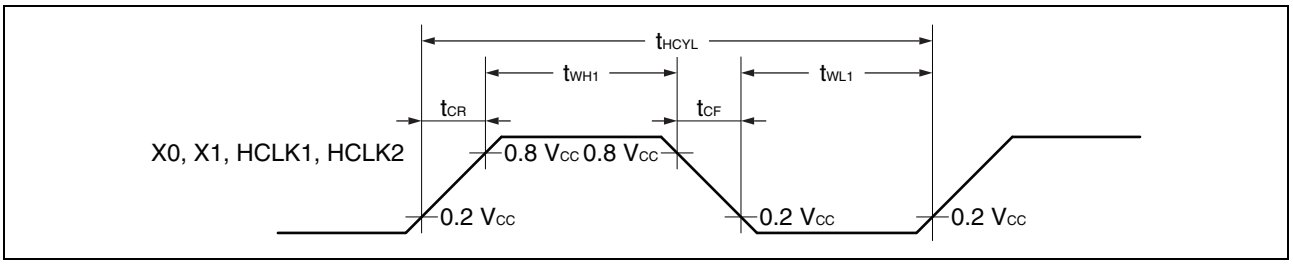
(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CCTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz Time-base timer mode T_A = +25°C	—	1.1	3	mA	
	I_{CCH}		V_{CC} = 5.5 V Substop mode T_A = +25°C	—	3.5	22.5	µA	
	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	37	54	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	

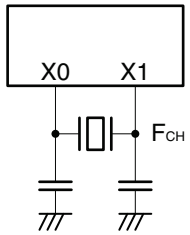
*1: The input levels of P04, P16, P60 and P61 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See "4. AC Characteristics: (1) Clock Timing" for F_{CH} and F_{CL}.
- See "4. AC Characteristics: (2) Source Clock/Machine Clock" for F_{MP} and F_{MPL}.

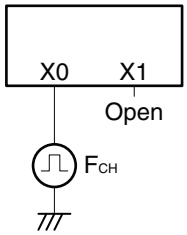


- Figure of main clock input port external connection

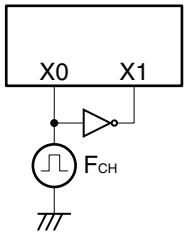
When a crystal oscillator or a ceramic oscillator is used



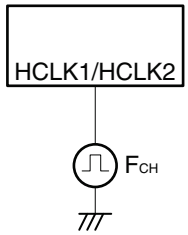
When the external clock is used (X1 is open)

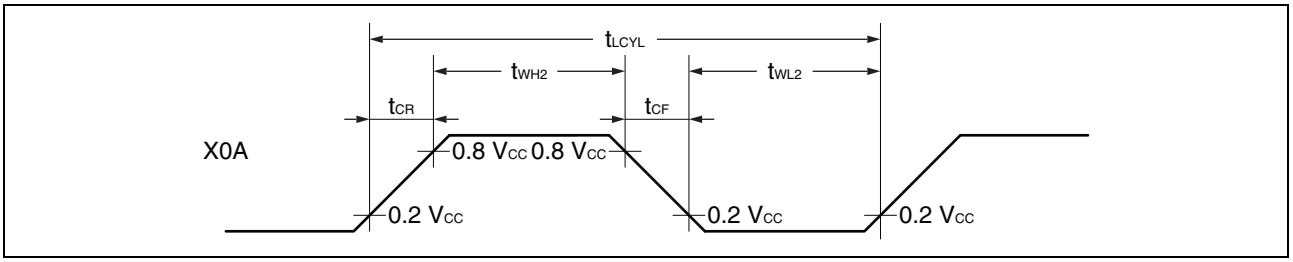


When the external clock is used



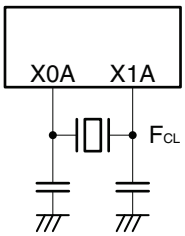
When the external clock is used



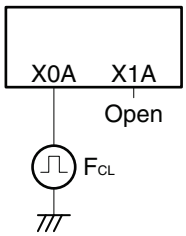


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



13.4.3 External Reset

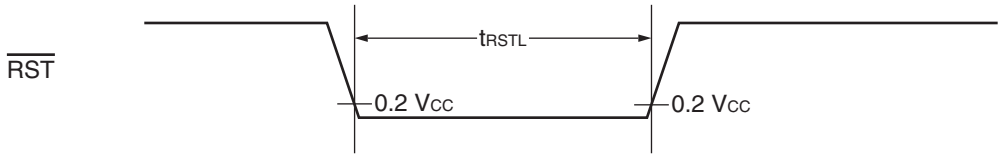
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

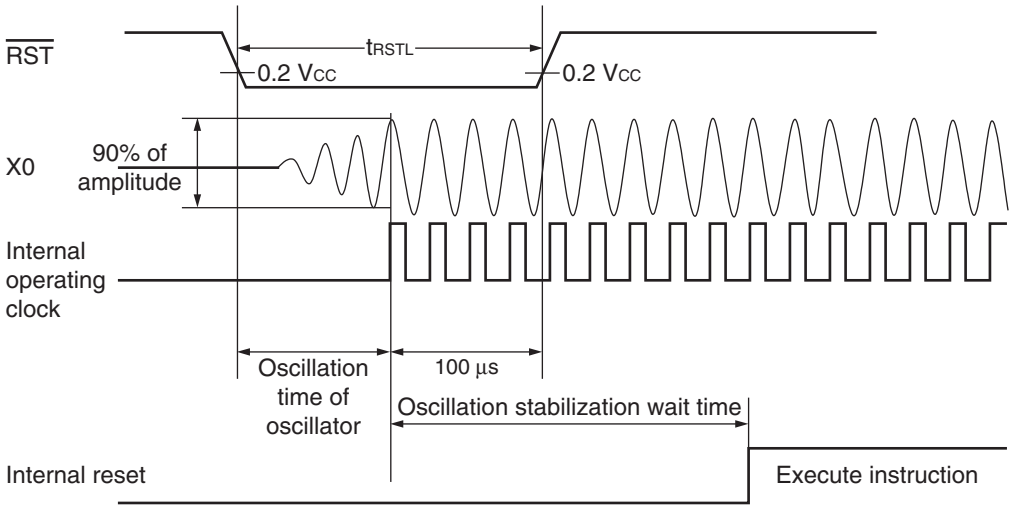
*1: See "(2) Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

- In normal operation



- In stop mode, subclock mode, subsleep mode, watch mode and power-on



13.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on

13.4.6 LIN-UART Timing

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

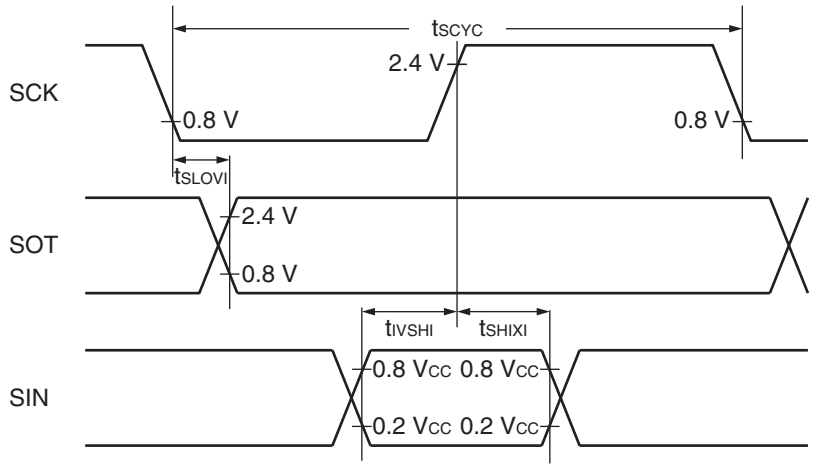
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

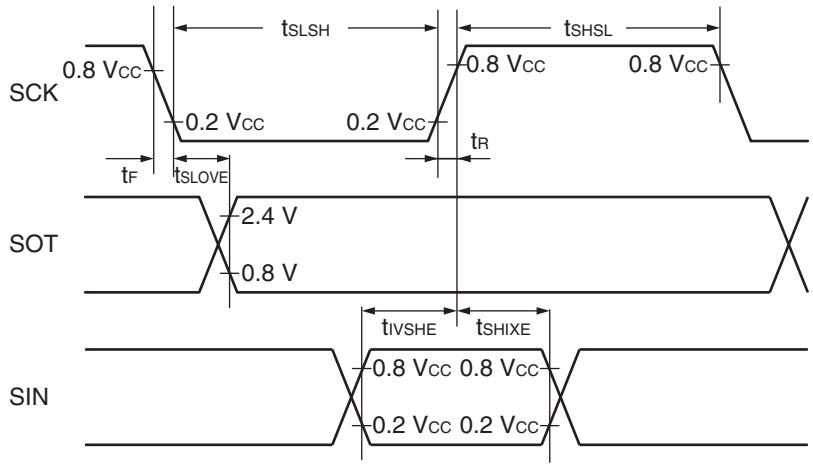
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

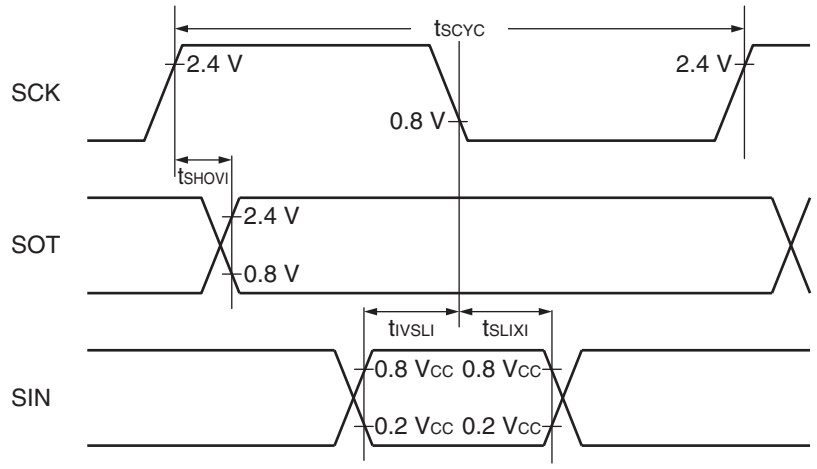
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

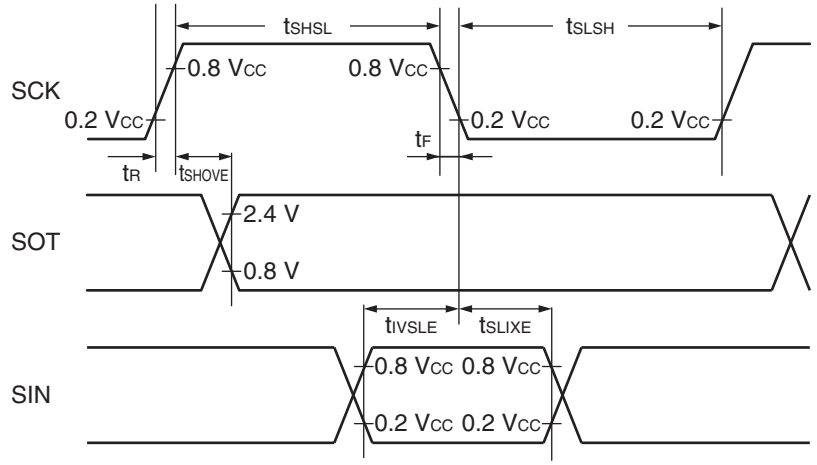
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



13.4.8 I²C Timing

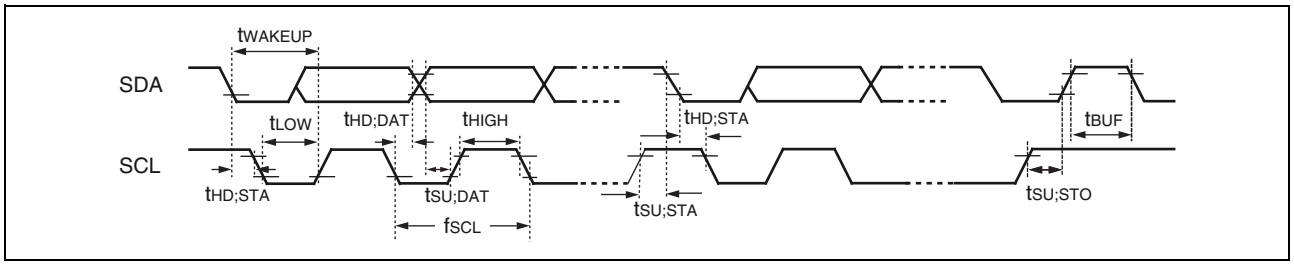
(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Stan-dard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock "L" width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock "H" width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeated) START condition hold time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.

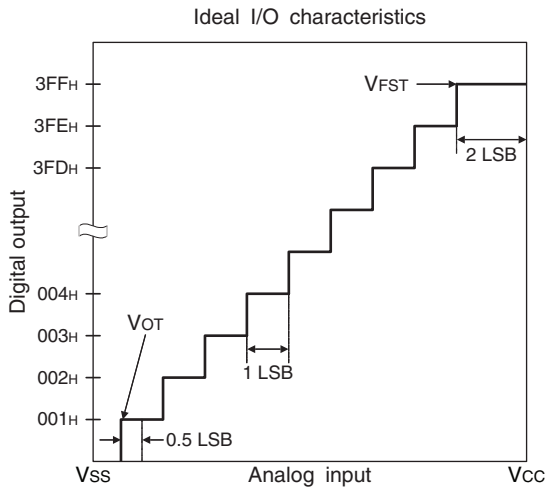


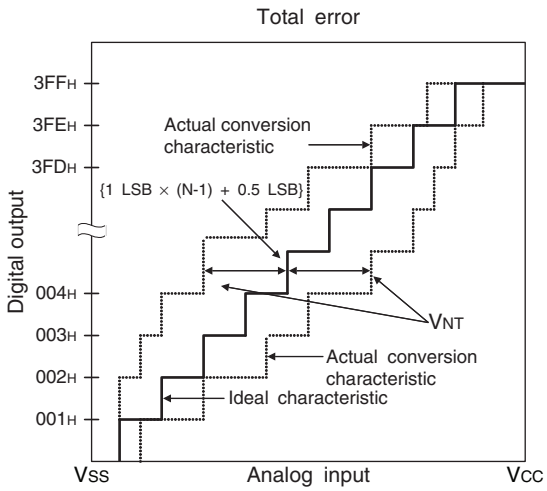
(Continued)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL, SDA		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		$(2\ nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3\ t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(-2 + nm/2)t_{MCLK} - 20$	$(-1 + nm/2)t_{MCLK} + 20$	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to the interrupt at the 8th SCL↓.

(Continued)





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

N : A/D converter digital output value

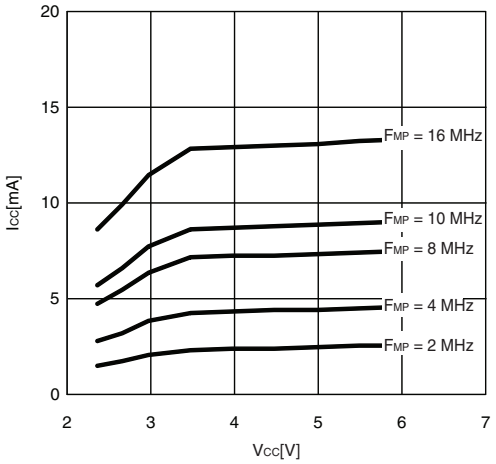
V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

(Continued)

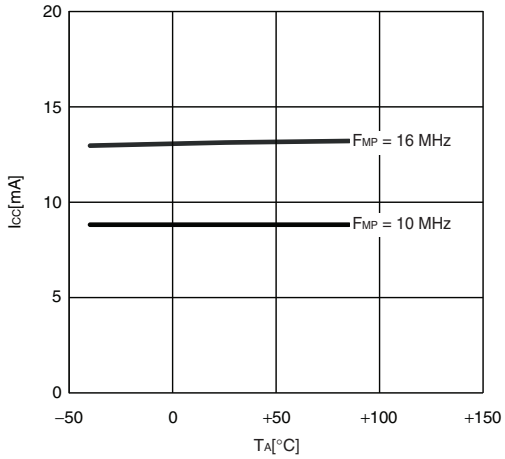
14. Sample Characteristics

■ Power supply current temperature characteristics

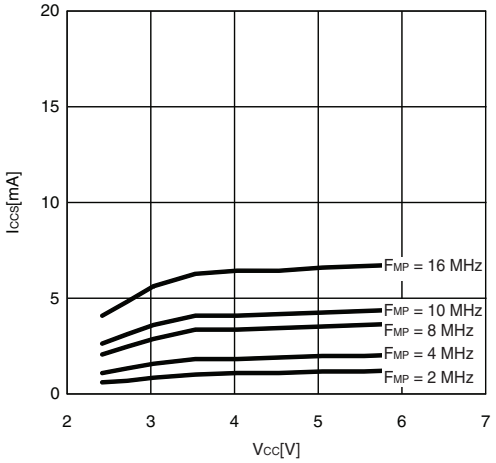
$I_{CC} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



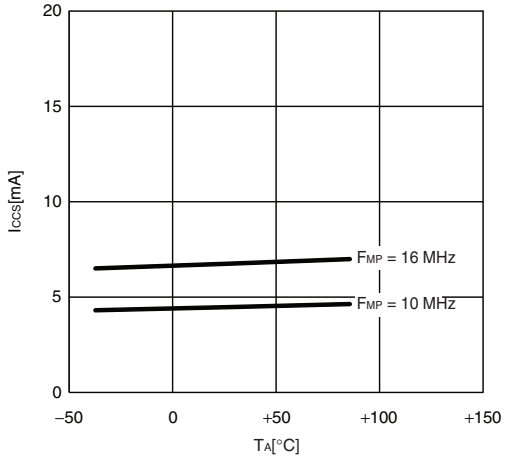
$I_{CC} - T_A$
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



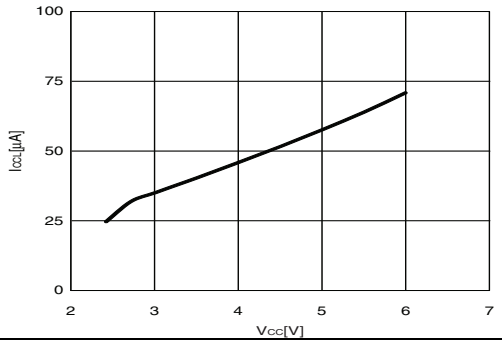
$I_{CCS} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



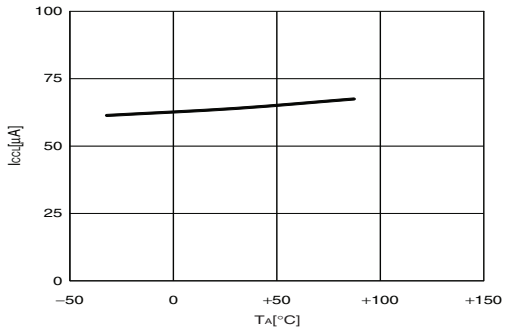
$I_{CCS} - T_A$
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



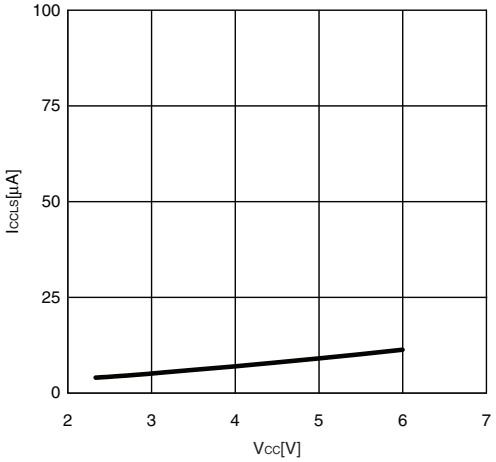
$I_{CCL} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



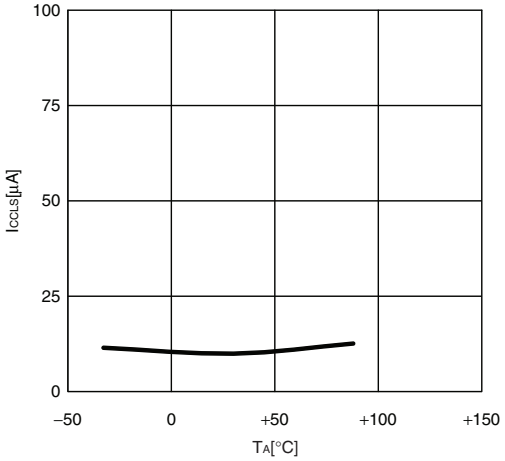
$I_{CCL} - T_A$
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



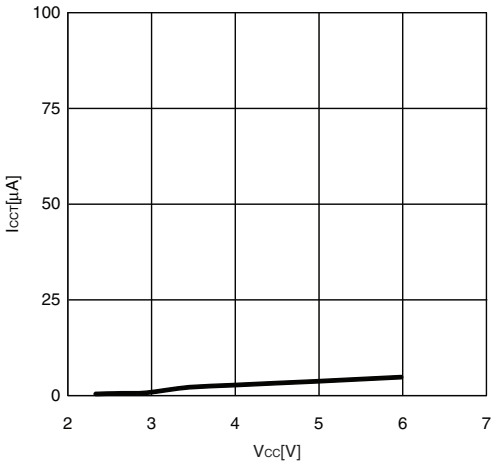
$I_{CCLS} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



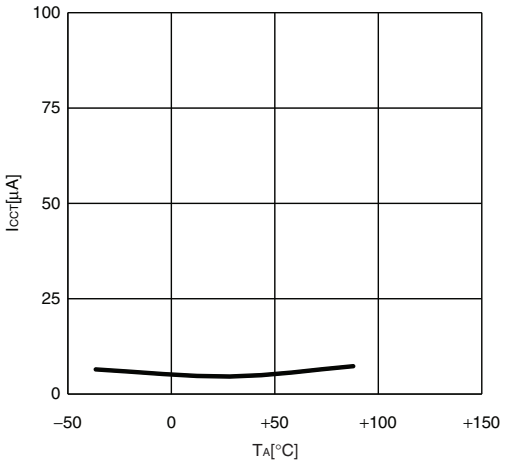
$I_{CCLS} - T_A$
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



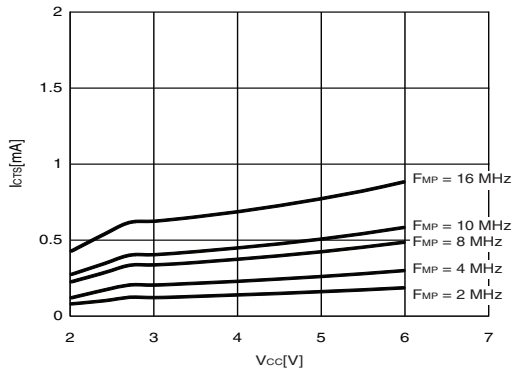
$I_{CCT} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



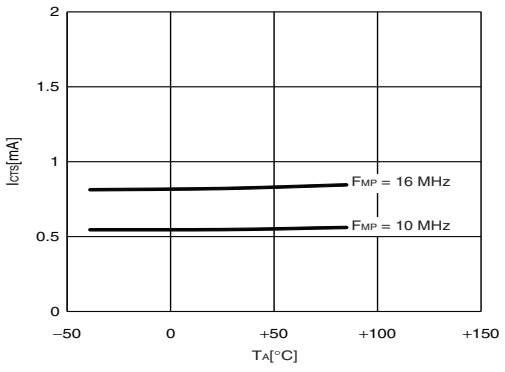
$I_{CCT} - T_A$
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



$I_{CTS} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



$I_{CTS} - T_A$
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



16. Ordering Information

Part Number	Package
MB95F332HPMC-G-SNE2 MB95F332KPMC-G-SNE2 MB95F333HPMC-G-SNE2 MB95F333KPMC-G-SNE2 MB95F334HPMC-G-SNE2 MB95F334KPMC-G-SNE2	32-pin plastic LQFP (FPT-32P-M30)
MB95F332HP-G-SH-SNE2 MB95F332KP-G-SH-SNE2 MB95F333HP-G-SH-SNE2 MB95F333KP-G-SH-SNE2 MB95F334HP-G-SH-SNE2 MB95F334KP-G-SH-SNE2	32-pin plastic SH-DIP (DIP-32P-M06)
MB95F332HWQN-G-SNE1 MB95F332KWQN-G-SNE1 MB95F333HWQN-G-SNE1 MB95F333KWQN-G-SNE1 MB95F334HWQN-G-SNE1 MB95F334KWQN-G-SNE1	32-pin plastic QFN (LCC-32P-M19)

Document History

Document Title: MB95F332H/F332K/F333H/F333K/F334H/F334K F^{2}MC-8FX MB95330H Series 8-bit Microcontrollers Document Number: 002-07522				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	04/12/2010	Migrated to Cypress and assigned document number 002-07522. No change to document contents or format.
*A	5181238	AKIH	04/04/2016	Updated to Cypress template