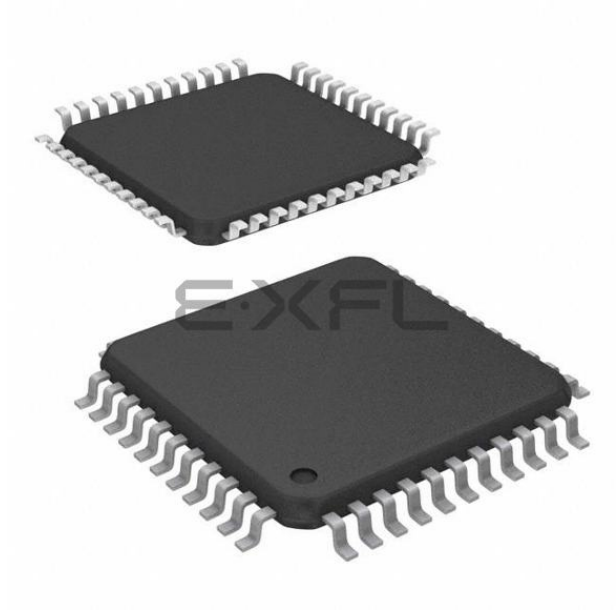

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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp51id2-20aau

1.5 Pin Description

Table 1-1. Atmel AT89LP51RD2/ED2/ID2 Pin Description

Pin Number					
VQFP VQFN	PLCC	(1) PDIP	Symbol	Type	Description
1	7	6	P1.5	I/O I/O I/O I/O	**P1.5**: User-configurable I/O Port 1 bit 5. **MISO**: SPI master-in/slave-out. When configured as master, this pin is an input. When configured as slave, this pin is an output. **MOSI**: SPI master-out/slave-in (Remap mode). When configured as master, this pin is an output. When configured as slave, this pin is an input. During In-System Programming, this pin is an input. **CEX2**: Capture/Compare external I/O for PCA module 2.
2	8	7	P1.6	I/O I/O I/O I/O	**P1.6**: User-configurable I/O Port 1 bit 6. **SCK**: SPI Clock. When configured as master, this pin is an output. When configured as slave, this pin is an input. **MISO**: SPI master-in/slave-out (Remap mode). When configured as master, this pin is an input. When configured as slave, this pin is an output. During In-System Programming, this pin is an output. **CEX3**: Capture/Compare external I/O for PCA module 3.
3	9	8	P1.7	I/O I/O I/O I/O	**P1.7**: User-configurable I/O Port 1 bit 7. **MOSI**: SPI master-out/slave-in. When configured as master, this pin is an output. When configured as slave, this pin is an input. **SCK**: SPI Clock (Remap mode). When configured as master, this pin is an output. When configured as slave, this pin is an input. During In-System Programming, this pin is an input. **CEX4**: Capture/Compare external I/O for PCA module 4.
4	10	9	RST	I/O I	**RST**: External Reset input (Reset polarity depends on POL pin). The RST pin can output a pulse when the internal Watchdog reset or POR is active. **DCL**: Serial Debug Clock input for On-Chip Debug Interface when OCD is enabled.
5	11	10	P3.0	I/O I	**P3.0**: User-configurable I/O Port 3 bit 0. **RXD**: Serial Port Receiver Input.
6	12		P4.1	I/O I/O	**P4.1**: User-configurable I/O Port 4bit 1. **SDA**: TWI bidirectional Serial Data line.
7	13	11	P3.1	I/O O	**P3.1**: User-configurable I/O Port 3 bit 1. **TXD**: Serial Port Transmitter Output.
8	14	12	P3.2	I/O I	**P3.2**: User-configurable I/O Port 3 bit 2. **$\overline{\text{INT0}}$**: External Interrupt 0 Input or Timer 0 Gate Input.
9	15	13	P3.3	I/O I	**P3.3**: User-configurable I/O Port 3 bit 3. **$\overline{\text{INT1}}$**: External Interrupt 1 Input or Timer 1 Gate Input
10	16	14	P3.4	I/O I/O	**P3.4**: User-configurable I/O Port 3 bit 4. **T1**: Timer/Counter 0 External input or output.
11	17	15	P3.5	I/O I/O	**P3.5**: User-configurable I/O Port 3 bit 5. **T1**: Timer/Counter 1 External input or output.
12	18	16	P3.6	I/O O	**P3.6**: User-configurable I/O Port 3 bit 6. **$\overline{\text{WR}}$**: External memory interface Write Strobe (active-low).
13	19	17	P3.7	I/O O	**P3.7**: User-configurable I/O Port 3 bit 7. **$\overline{\text{RD}}$**: External memory interface Read Strobe (active-low).
14	20	18	P4.7	I/O O	**P4.7**: User-configurable I/O Port 4 bit 7. **XTAL2A**: Output from inverting oscillator amplifier A. It may be used as a port pin if the internal RC oscillator or external clock is selected as the clock source A.
15	21	19	P4.6	I/O I	**P4.6**: User-configurable I/O Port 4 bit 6. **XTAL1A**: Input to the inverting oscillator amplifier A and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source A.

Table 1-1. Atmel AT89LP51RD2/ED2/ID2 Pin Description

Pin Number					
VQFP VQFN	PLCC	(1) PDIP	Symbol	Type	Description
16	22	20	GND	I	Ground
17	23		P4.3	I/O I/O	**P4.3**: User-configurable I/O Port 4bit 3. **DDA**: Bidirectional Debug Data line for the On-Chip Debug Interface when OCD is enabled.
18	24	21	P2.0	I/O O	**P2.0**: User-configurable I/O Port 2 bit 0. **A8**: External memory interface Address bit 8.
19	25	22	P2.1	I/O O	**P2.1**: User-configurable I/O Port 2 bit 1. **A9**: External memory interface Address bit 9.
20	26	23	P2.1	I/O O O	**P2.2**: User-configurable I/O Port 2 bit 2. **DA-**: DAC negative differential output. **A10**: External memory interface Address bit 10.
21	27	24	P2.3	I/O O O	**P2.3**: User-configurable I/O Port 2 bit 3. **DA+-**: DAC positive differential output. **A11**: External memory interface Address bit 11.
22	28	25	P2.4	I/O I O	**P2.4**: User-configurable I/O Port 2 bit 5. **AIN0**: Analog Comparator Input 0. **A12**: External memory interface Address bit 12.
23	29	26	P2.5	I/O I O	**P2.5**: User-configurable I/O Port 2 bit 5. **AIN1**: Analog Comparator Input 1. **A13**: External memory interface Address bit 13.
24	30	27	P2.6	I/O I O	**P2.6**: User-configurable I/O Port 2 bit 6. **AIN2**: Analog Comparator Input 2. **A14**: External memory interface Address bit 14.
25	31	28	P2.7	I/O I O	**P2.7**: User-configurable I/O Port 2 bit 7. **AIN3**: Analog Comparator Input 3. **A15**: External memory interface Address bit 15.
26	32	29	P4.5	I/O O	**P4.5**: User-configurable I/O Port 4 bit 5. **$\overline{\text{PSEN}}$**: External memory interface Program Store Enable (active-low).
27	33	30	P4.4	I/O I/O	**P4.4**: User-configurable I/O Port 4 bit 4. **ALE**: External memory interface Address Latch Enable.
28	34		P4.0	I/O	**P4.0**: User-configurable I/O Port 4 bit 0. **SCL**: TWI Serial Clock line. This line is an output in mater mode and an input in slave mode.
29	35	31	POL	I	**POL**: Reset polarity
30	36	32	P0.7	I/O I/O	**P0.7**: User-configurable I/O Port 0 bit 7. **AD7**: External memory interface Address/Data bit 7.
31	37	33	P0.6	I/O I/O I	**P0.6**: User-configurable I/O Port 0 bit 6. **AD6**: External memory interface Address/Data bit 6. **ADC6**: ADC analog input 6.
32	38	34	P0.5	I/O I/O I	**P0.5**: User-configurable I/O Port 0 bit 5. **AD5**: External memory interface Address/Data bit 5. **ADC5**: ADC analog input 5.
33	39	35	P0.4	I/O I/O I	**P0.4**: User-configurable I/O Port 0 bit 4. **AD4**: External memory interface Address/Data bit 4. **ADC4**: ADC analog input 4.
34	40	36	P0.3	I/O I/O I	**P0.3**: User-configurable I/O Port 0 bit 3. **AD3**: External memory interface Address/Data bit 3. **ADC3**: ADC analog input 3.

Table 1-1. Atmel AT89LP51RD2/ED2/ID2 Pin Description

Pin Number			Symbol	Type	Description
VQFP VQFN	PLCC	(1) PDIP			
35	41	37	P0.2	I/O I/O I	**P0.2**: User-configurable I/O Port 0 bit 2. **AD2**: External memory interface Address/Data bit 2. **ADC2**: ADC analog input 2.
36	42	38	P0.1	I/O I/O I	**P0.1**: User-configurable I/O Port 0 bit 1. **AD1**: External memory interface Address/Data bit 1. **ADC1**: ADC analog input 1.
37	43	39	P0.0	I/O I/O I	**P0.0**: User-configurable I/O Port 0 bit 0. **AD0**: External memory interface Address/Data bit 0. **ADC0**: ADC analog input 0.
38	44	40	VDD	I	Supply Voltage
39	1		P4.2	I/O	**P4.2**: User-configurable I/O Port 4bit 2. **XTAL2B**: Output from low-frequency inverting oscillator amplifier B (AT89LP51ID2 only). It may be used as a port pin if the internal RC oscillator or external clock is selected as the clock source.
40	2	1	P1.0	I/O I/O	**P1.0**: User-configurable I/O Port 1 bit 0. **T2**: Timer 2 External Input or Clock Output. **XTAL1B**: Input to the low-frequency inverting oscillator amplifier B and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source.
41	3	2	P1.1	I/O I I	**P1.1**: User-configurable I/O Port 1 bit 1. **T2EX**: Timer 2 External Capture/Reload Input. **$\overline{SS}$**: SPI Slave-Select.
42	4	3	P1.2	I/O	**P1.2**: User-configurable I/O Port 1 bit 2.
43	5	4	P1.3	I/O I/O	**P1.3**: User-configurable I/O Port 1 bit 3. **CEX0**: Capture/Compare external I/O for PCA module 0.
44	6	5	P1.4	I/O I I/O	**P1.4**: User-configurable I/O Port 1 bit 4. **$\overline{SS}$**: SPI Slave-Select (Remap Mode). This pin is an input for In-System Programming **CEX1**: Capture/Compare external I/O for PCA module 1.

Note: 1. The AT89LP51ID2 is not available in the PDIP package.

2. Overview

The Atmel® AT89LP51RD2/ED2/ID2 is a low-power, high-performance CMOS 8-bit 8051 microcontroller with 64KB of In-System Programmable Flash program memory. The AT89LP51ED2 and AT89LP51ID2 provide an additional 4KB of EEPROM for nonvolatile data storage. The devices are manufactured using Atmel's high-density nonvolatile memory technology and are compatible with the industry-standard 80C51 instruction set.

The AT89LP51RD2/ED2/ID2 is built around an enhanced CPU core that can fetch a single byte from memory every clock cycle. In the classic 8051 architecture, each fetch requires 6 clock cycles, forcing instructions to execute in 12, 24 or 48 clock cycles. In the AT89LP51RD2/ED2/ID2 CPU, standard instructions need only one to four clock cycles providing six to twelve times more throughput than the standard 8051. Seventy percent of instructions need only as many clock cycles as they have bytes to execute, and most of the remaining instructions require only one additional clock. The enhanced CPU core is capable of 20 MIPS throughput whereas the classic 8051 CPU can deliver only 4 MIPS at the same current consumption. Conversely, at the same throughput as the classic 8051, the new CPU core runs at a much lower speed and thereby greatly reducing power consumption and EMI. The

AT89LP51RD2/ED2/ID2 also includes a compatibility mode that will enable classic 12 clock per machine cycle operation for true timing compatibility with the Atmel AT89C51RD2/ED2.

The AT89LP51RD2/ED2/ID2 retains all of the standard features of the AT89C51RD2/ED2, including: 64KB of In-System Programmable Flash program memory, 4KB of EEPROM (AT89LP51ED2/ID2 Only), 256 bytes of RAM, 2KB of expanded RAM, up to 40 I/O lines, three 16-bit timer/counters, a Programmable Counter Array, a programmable hardware watchdog timer, a keyboard interface, a full-duplex enhanced serial port, a serial peripheral interface (SPI), on-chip crystal oscillator, and a four-level, ten-vector interrupt system. A block diagram is shown in Figure 2-1.

In addition, the Atmel® AT89LP51RD2/ED2/ID2 provides a Two-Wire Interface (TWI) for up to 400KB/s serial transfer; a 10-bit, 8-channel Analog-to-Digital Converter (ADC) with temperature sensor and digital-to-analog (DAC) mode; two analog comparators; an 8MHz internal oscillator; and more on-chip data memory than the Atmel AT89C51RD2/ED2 (4KB vs. 2KB EEPROM and 2048 vs. 1792 bytes ERAM).

Some standard features on the AT89LP51RD2/ED2/ID2 are enhanced with new modes or operations. Mode 0 of Timer 0 or Timer 1 acts as a variable 9–16 bit timer/counter and Mode 1 acts as a 16-bit auto-reload timer/counter. In addition, each timer/counter may independently drive an 8-bit precision pulse width modulation output. Mode 0 (synchronous mode) of the serial port allows flexibility in the phase/polarity relationship between clock and data.

The I/O ports of the AT89LP51RD2/ED2/ID2 can be independently configured in one of four operating modes. In quasi-bidirectional mode, the ports operate as in the classic 8051. In input-only mode, the ports are tristated. Push-pull output mode provides full CMOS drivers and open-drain mode provides just a pull-down. Unlike other 8051s, this allows Port 0 to operate with on-chip pull-ups if desired.

The AT89LP51RD2/ED2/ID2 includes an On-Chip Debug (OCD) interface that allows read-modify-write capabilities of the system state and program flow control, and programming of the internal memories. The on-chip Flash and EEPROM may also be programmed through the UART-based bootloader or the SPI-based In-System programming interface (ISP).

The TWI and OCD features are not available on the PDIP package. The AT89LP51ID2 is also not available in PDIP.

The features of the AT89LP51RD2/ED2/ID2 make it a powerful choice for applications that need pulse width modulation, high speed I/O, and counting capabilities such as alarms, motor control, corded phones, and smart card readers.

Table 2-1. User Configuration Fuses

Fuse Name	Description
Clock Source A	Selects between the High Speed Crystal Oscillator, Low Power Crystal Oscillator, External Clock on XTAL1A or Internal RC Oscillator for the source of the system clock when oscillator A is selected.
Clock Source B	Selects between the 32 kHzCrystal Oscillator, External Clock on XTAL1B or Internal RC Oscillator for the source of the system clock when oscillator B is selected (AT89LP51ID2 Only).
Oscillator Select	Selects whether oscillator A or B is enabled to boot the device. (AT89LP51ID2 Only)
X2 Mode	Selects the default state of whether the clock source is divided by two (X1) or not (X2) to generate the system clock.
Start-up Time	Selects time-out delay for the POR/BOD/PWD wake-up period.
Compatibility Mode	Configures the CPU in 12-clock compatibility or single-cycle fast execution mode.
XRAM Configuration	Configures if access to on-chip memories that are mapped to the external data memory address space is enabled/disabled by default.
Bootloader Jump Bit	Enables or disables the on-ship bootloader.
On-Chip Debug Enable	Enables or disables On-Chip Debug. OCD must be enabled prior to using an in-circuit debugger with the device.
In-System Programming Enable	Enables or disables In-System Programming.
User Signature Programming Enable	Enables or disables programming of User Signature array.
Default Port State	Configures the default port state as input-only mode (tristated) or quasi-bidirectional mode (weakly pulled high).
Low Power Mode	Enables or disables power reduction features for lower system frequencies.

2.2.2 Software Options

Table 2-2 lists some important software configuration bits that affect operation at the system level. These can be changed by the application software but are set to their default values upon any reset. Most peripherals also have multiple configuration bits that are not listed here.

Table 2-2. Important Software Configuration Bits

Bit(s)	SFR Location	Description
PxM0.y PxM1.y	P0M0, P0M1, P1M0, P1M1, P2M0, P2M1, P3M0, P3M1, P4M0, P4M1	Configures the I/O mode of Port x Pin y to be one of input-only, quasi-bidirectional, push-pull output or open-drain. The default state is controlled by the Default Port State fuse above
CKRL	CKRL	Selects the division ratio between the oscillator and the system clock
TPS_{3-0}	CLKREG.7-4	Selects the division ratio between the system clock and the timers
ALES	AUXR.0	Enables/disables toggling of ALE
EXRAM	AUXR.1	Enables/disables access to on-chip memories that are mapped to the external data memory address space
WS_{1-0}	AUXR.6-5	Selects the number of wait states when accessing external data memory
XSTK	AUXR1.4	Configures the hardware stack to be in RAM or extra RAM
EEE	EECON.1	Enables/disables access to the on-chip EEPROM
ENBOOT	AUXR1.5	Enables/disables access to the on-chip Flash API

2.3 Comparison to the Atmel AT89C51RD2/ED2/ID2

The Atmel® AT89LP51RD2/ED2/ID2 is part of a family of devices with enhanced features that are fully binary compatible with the 8051 instruction set. The AT89LP51RD2/ED2/ID2 has two modes of operations, Compatibility mode and Fast mode. In Compatibility mode the instruction timing, peripheral behavior, SFR addresses, bit assignments and pin functions are identical to the existing Atmel AT89C51RD2/ED2/ID2 product. Additional enhancements are transparent to the user and can be used if desired. Fast mode allows greater performance, but with some differences in behavior. The major enhancements from the AT89C51RD2/ED2/ID2 are outlined in the following paragraphs and may be useful to users migrating to the AT89LP51RD2/ED2/ID2 from older devices. A summary of the differences between Compatibility and Fast modes is given in Table 2-3 on page 11. See also the Application note “Migrating from AT89C51RD2/ED2/ID2 to AT89LP51RD2/ED2/ID2.”

2.3.1 Instruction Execution

In Compatibility mode the Atmel® AT89LP51RD2/ED2/ID2 CPU uses the six-state machine cycle of the standard 8051 where instruction bytes are fetched every three system clock cycles. Execution times in this mode are identical to the Atmel AT89C51RD2/ED2/ID2. For greater performance the user can enable Fast mode by disabling the Compatibility fuse. In Fast mode the CPU fetches one code byte from memory every clock cycle instead of every three clock cycles. This greatly increases the throughput of the CPU. Each standard instruction executes in only one to four clock cycles. See datasheet for more details. Any software delay loops or instruction-based timing operations may need to be retuned to achieve the desired results in Fast mode.

2.3.2 System Clock

The system clock source is not limited to a crystal or external clock. The system clock source is selectable between the crystal oscillator, an externally driven clock and an internal 8.0MHz RC oscillator for AT89LP51RD2/ED2 and clock source A of AT89LP51ID2. Clock source B of AT89LP51ID2 is not limited to a 32 kHz crystal. The clock source B is selectable between the 32 kHz crystal oscillator, an externally driven clock and an internal 8.0MHz RC oscillator. Unlike AT89C51ID2, the X2 and CKRL features will also affect the OSCB source.

By default in Compatibility mode the system clock frequency is divided by 2 from the externally supplied XTAL1 frequency for compatibility with standard 8051s (12 clocks per machine cycle). The System Clock Divider can scale the system clock versus the oscillator source. The divide-by-2 can be disabled to operate in X2 mode (6 clocks per machine cycle) or the clock may be further divided to reduce the operating frequency. In Fast mode the clock divider defaults to divide by 1.

2.3.3 Reset

The RST pin of the AT89LP51RD2/ED2/ID2 has selectable polarity using the POL pin (formerly $\overline{EA}$). When POL is high the RST pin is active high with a pull-down resistor and when POL is low the RST pin is active low with a pull-up resistor. For existing AT89C51RD2/ED2/ID2 sockets where $\overline{EA}$ is tied to VDD, replacing AT89C51RD2/ED2 with AT89LP51RD2/ED2/ID2 will maintain the active high reset. Note that forcing external execution by tying $\overline{EA}$ low is not supported.

The AT89LP51RD2/ED2/ID2 includes an on-chip Power-On Reset and Brown-out Detector circuit that ensures that the device is reset from system power up. In most cases a RC startup circuit is not required on the RST pin, reducing system cost, and the RST pin may be left unconnected if a board-level reset is not present.

2.3.4 Timer/Counters

A common prescaler is available to divide the time base for Timer 0, Timer 1, Timer 2 and the WDT. The TPS_{3-0} bits in the CLKREG SFR control the prescaler. In Compatibility mode TPS_{3-0} defaults to 0101B, which causes the timers to count once every machine cycle. The counting rate can be adjusted linearly from the system clock rate to 1/16 of the system clock rate by changing TPS_{3-0}. In Fast mode TPS_{3-0} defaults to 0000B, or the system clock rate. TPS does not affect Timer 2 in Clock Out or Baud Generator modes.

In Compatibility mode the sampling of the external Timer/Counter pins: T0, T1, T2 and T2EX; and the external interrupt pins, $\overline{INT0}$ and $\overline{INT1}$, is also controlled by the prescaler. In Fast mode these pins are always sampled at the system clock rate.

Both Timer 0 and Timer 1 can toggle their respective counter pins, T0 and T1, when they overflow by setting the output enable bits in TCONB.

2.3.5 Interrupt Handling

Fast mode allows for faster interrupt response due to the shorter instruction execution times.

2.3.6 Keyboard Interface

The AT89LP51RD2/ED2/ID2 does not clear the keyboard flag register (KBF) after a read. Each bit must be cleared in software. This allows the interrupt to be generate once per flag when multiple flags are set, if desired. To mimic the old behavior the service routine must clear the whole register.

The keyboard can also support general edge-triggered interrupts with the addition of the KBMOD register.

2.3.7 Serial Port

The timer prescaler increases the range of achievable baud rates when using Timer 1 to generate the baud rate in UART Modes 1 or 3, including an increase in the maximum baud rate available in Compatibility mode. Additional features include automatic address recognition and framing error detection.

The shift register mode (Mode 0) has been enhanced with more control of the polarity, phase and frequency of the clock and full-duplex operation. This allows emulation of master serial peripheral (SPI) and two-wire (TWI) interfaces.

2.3.8 I/O Ports

The P0, P1, P2 and P3 I/O ports of the AT89LP51RD2/ED2/ID2 may be configured in four different modes. The default setting depends on the Tristate-Port User Fuse. When the fuse is set all the I/O ports revert to input-only (tristated) mode at power-up or reset. When the fuse is not active, ports P1, P2 and P3 start in quasi-bidirectional mode and P0 starts in open-drain mode. P4 always operates in quasi-bidirectional mode. P0 can be configured to have internal pull-ups by placing it in quasi-bidirectional or output modes. This can reduce system cost by removing the need for external pull-ups on Port 0.

The P4.4–P4.7 pins are additional I/Os that replace the normally dedicated ALE, PSEN, XTAL1 and XTAL2 pins of the AT89C51RD2/ED2/ID2. These pins can be used as additional I/Os depending on the configuration of the clock and external memory.

2.3.9 Security

The AT89LP51RD2/ED2/ID2 does not support the external access pin ($\overline{EA}$). Therefore it is not possible to execute from external program memory in address range 0000H–1FFFH. When the third Lockbit is enabled (Lock Mode 4) external program execution is disabled for all addresses above 1FFFH. This differs from AT89C51RD2/ED2/ID2 where Lock Mode 4 prevents $\overline{EA}$ from being sampled low, but may still allow external execution at addresses outside the 8K internal space.

2.3.10 Programming

The AT89LP51RD2/ED2/ID2 supports a richer command set for In-System Programming (ISP). Existing AT89C51RD2/ED2 programmers should be able to program the AT89LP51RD2/ED2/ID2 in byte mode. In page mode the AT89LP51RD2/ED2/ID2 only supports programming of a half-page of 64 bytes and therefore requires an extra address byte as compared to AT89C51RD2/ED2. Furthermore the device signature is located at addresses 0000H, 0001H and 0003H instead of 0000H, 0100H and 0200H.

Table 2-3. Compatibility Mode versus Fast Mode Summary

Feature	Compatibility	Fast
Instruction Fetch in System Clocks	3	1
Instruction Execution Time in System Clocks	6, 12, 18 or 24	1, 2, 3, 4 or 5
Default System Clock Divisor	2	1
Default Timer Prescaler Divisor	6	1
Pin Sampling Rate ($\overline{INT0}$, $\overline{INT1}$, T0, T1, T2, T2EX)	Prescaler Rate	System Clock
Minimum RST input pulse in System Clocks	12	2

3. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 3-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

Table 3-1. Atmel AT89LP51RD2/ED2/ID2 SFR Map and Reset Values

	8	9	A	B	C	D	E	F	
0F8H		CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		0FFH
0F0H	B 0000 0000		RL0 0000 0000	RL1 0000 0000	RH0 0000 0000	RH1 0000 0000	PAGE 0000 0000	BX 0000 0000	0F7H
0E8H		CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000	SPX xxxx x000	0EFH
0E0H	ACC 0000 0000	AX 0000 0000	DSPR 0000 0000	FIRD 0000 0000	MACL 0000 0000	MACH 0000 0000	P0M0 (2)	P0M1 0000 0000	0E7H
0D8H	CCON 00x0 0000	CMOD 00xx x000	CCAPM0 x000 0000	CCAPM1 x000 0000	CCAPM2 x000 0000	CCAPM3 x000 0000	CCAPM4 x000 0000		0DFH
0D0H	PSW 0000 0000	FCON xxxx 0000	EECON 0000 0000		DPLB 0000 0000	DPHB 0000 0000	P1M0 (2)	P1M1 0000 0000	0D7H
0C8H	T2CON 0000 0000	T2MOD 0000 0000	RCAP2L 0000 000	RCAP2H 0000 0000	TL2 0000 000	TH2 0000 0000	P2M0 (2)	P2M1 0000 0000	0CFH
0C0H	P4 1111 1111			SPCON 0001 0100	SPSTA 0000 0000	SPDAT xxxx xxxx	P3M0 (2)	P3M1 0000 0000	0C7H
0B8H	IPL0 xx00 0000	SADEN 0000 0000				AREF 0000 0000	P4M0 (2)	P4M1 0000 0000	0BFH
0B0H	P3 1111 1111	IEN1 xxxx 0000	IPL1 xxxx 0000	IPH1 xxxx 0000				IPH0 xx00 0000	0B7H
0A8H	IEN0 0x00 0000	SADDR 0000 0000		ACSRB 0000 0000	DADL 0000 0000	DADH 0000 0000	CLKREG 0101 xxxx	CKCON1 xxxx xxx0	0AFH
0A0H	P2 1111 1111	DPCF 0000 0000	AUXR1 0000 00x0	ACSRA 0000 0000	DADC 0000 0000	DADI 0000 0000	WDTRST (write-only)	WDTPRG 0000 0xx0	0A7H
98H	SCON 0000 0000	SBUF xxxx xxxx	BRL 0000 0000	BDRCON xxx0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000	KBMOD 0000 0000	9FH
90H	P1 1111 1111	TCONB 0010 0100	BMSEL xxxx xxx0	SSCON 0000 0000	SSCS 1111 1000	SSDAT 1111 1111	SSADR 1111 1110	CKRL 1111 1111	97H
88H	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 0000 0000	CKCON0 0000 0000	8FH
80H	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000		CKSEL xxxx xxx0	OSCCON xxxx x001	PCON 000x 0000	87H
	0	1	2	3	4	5	6	7	

Notes: 1. All SFRs in the left-most column are bit-addressable.

2. Reset value is 1111 1111B when Tristate-Port Fuse is enabled and 0000 0000B when disabled.

3. Reset value is 0101 0010B when Compatibility mode is enabled and 0000 0000B when disabled.

Table 3-2. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer								
SPX	EFh	Extended Stack Pointer	–	–	–	–	SP11	SP10	SP9	SP8
DPL	82h	Data Pointer Low Byte								
DPH	83h	Data Pointer High Byte								
DPLB	D4h	Alternate Data Pointer Low Byte								
DPHB	D5h	Alternate Data Pointer High Byte								
PAGE	F6h	ERAM Page Register	–	–	–	–				

Table 3-3. Digital Signal Processing SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
AX	E1h	Extended Accumulator								
BX	F7h	Extended B Register								
DSPR	E2h	DSP Control Register	MRW1	MRW0	SMLB	SMLA	CBE1	CBE0	MVCD	DPRB
FIRD	E3h	FIFO Depth								
MACL	E4h	MAC Low Byte								
MACH	E5h	MAC High Byte								

Table 3-4. System Management SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	PWDEX	POF	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	DPU	WS1	WS0/M0	XRS2	XRS1	XRS0	EXTRAM	AO
AUXR1	A2h	Auxiliary Register 1	–	–	ENBOOT	XSTK	GF3	0	–	DPS
DPCR	A3h	Datapointer Config Register	DPU1	DPU0	DPD1	DPD0	–	–	–	–
CKRL	97h	Clock Reload Register								
CKCKON0	8Fh	Clock Control Register 0	TWIX2	WDTX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2
CKCKON1	AFh	Clock Control Register 1	–	–	–	–	–	–	–	SPIX2
CKSEL[1]	85h	Clock Selection Register	–	–	–	–	–	–	–	CKS
CLKREG	AEh	Clock Register	TPS3	TPS2	TPS1	TPS0	–	–	–	–
OSCCON[1]	85h	Oscillator Control Register	–	–	–	–	–	SCLKT0	OscBEn	OscAEn

Note: 1. Present on AT89LP51ID2 Only

Table 3-5. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	–	–	EADC	ECMP	–	ESPI	ETWI	EKB
IPH0	B7h	Interrupt Priority Control High 0	IP1D	PPCH	PT2H	PHS	PT1H	PX1H	PT0H	PX0H
IPL0	B8h	Interrupt Priority Control Low 0	IP0D	PPCL	PT2L	PLS	PT1L	PX1L	PT0L	PX0L
IPH1	B3h	Interrupt Priority Control High 1	IP3D	–	PADL	PCMPL	–	SPIH	PTWL	PKBH
IPL1	B2h	Interrupt Priority Control Low 1	IP2D	–	PADH	PCMPH	–	SPIL	PTWH	PKBL

Table 3-6. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0								
P1	90h	8-bit Port 1								
P2	A0h	8-bit Port 2								
P3	B0h	8-bit Port 3								
P4	C0h	8-bit Port 4								
P0M0	E6h	Port 0 Mode 0								
P0M1	E7h	Port 0 Mode 1								
P1M0	D6h	Port 1 Mode 0								
P1M1	D7h	Port 1 Mode 1								
P2M0	CEh	Port 2 Mode 0								
P2M1	CFh	Port 2 Mode 1								
P3M0	C6h	Port 3 Mode 0								
P3M1	C7h	Port 3 Mode 1								
P4M0	BEh	Port 4 Mode 0								
P4M1	BFh	Port 4 Mode 1								

Table 3-7. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								
BDRCON	9Bh	Baud Rate Control	–	–	–	BRR	TBCK	RBCK	SPD	SRC
BRL	9Ah	Baud Rate Reload								

Table 3-15. PCA SFRs (Continued)

Mnemo -nic	Add	Name	7	6	5	4	3	2	1	0
CCAPM3	DDh	PCA Timer/Counter Mode 3		ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
CCAPM4	DEh	PCA Timer/Counter Mode 4		ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4
CCAP0H	FAh	PCA Compare Capture Module 0 H	CCAP0H7	CCAP0H6	CCAP0H5	CCAP0H4	CCAP0H3	CCAP0H2	CCAP0H1	CCAP0H0
CCAP1H	FBh	PCA Compare Capture Module 1 H	CCAP1H7	CCAP1H6	CCAP1H5	CCAP1H4	CCAP1H3	CCAP1H2	CCAP1H1	CCAP1H0
CCAP2H	FCh	PCA Compare Capture Module 2 H	CCAP2H7	CCAP2H6	CCAP2H5	CCAP2H4	CCAP2H3	CCAP2H2	CCAP2H1	CCAP2H0
CCAP3H	FDh	PCA Compare Capture Module 3 H	CCAP3H7	CCAP3H6	CCAP3H5	CCAP3H4	CCAP3H3	CCAP3H2	CCAP3H1	CCAP3H0
CCAP4H	FEh	PCA Compare Capture Module 4 H	CCAP4H7	CCAP4H6	CCAP4H5	CCAP4H4	CCAP4H3	CCAP4H2	CCAP4H1	CCAP4H0
CCAP0L	EAh	PCA Compare Capture Module 0 L	CCAP0L7	CCAP0L6	CCAP0L5	CCAP0L4	CCAP0L3	CCAP0L2	CCAP0L1	CCAP0L0
CCAP1L	EBh	PCA Compare Capture Module 1 L	CCAP1L7	CCAP1L6	CCAP1L5	CCAP1L4	CCAP1L3	CCAP1L2	CCAP1L1	CCAP1L0
CCAP2L	ECh	PCA Compare Capture Module 2 L	CCAP2L7	CCAP2L6	CCAP2L5	CCAP2L4	CCAP2L3	CCAP2L2	CCAP2L1	CCAP2L0
CCAP3L	EDh	PCA Compare Capture Module 3 L	CCAP3L7	CCAP3L6	CCAP3L5	CCAP3L4	CCAP3L3	CCAP3L2	CCAP3L1	CCAP3L0
CCAP4L	EEh	PCA Compare Capture Module 4 L	CCAP4L7	CCAP4L6	CCAP4L5	CCAP4L4	CCAP4L3	CCAP4L2	CCAP4L1	CCAP4L0

4.2 Cross Reference with AT89C51RD2/ED2/ID2

Table 4-1. Ordering Cross Reference AT89C51RD2/ED2/ID2 to AT89LP51RD2/ED2/ID2

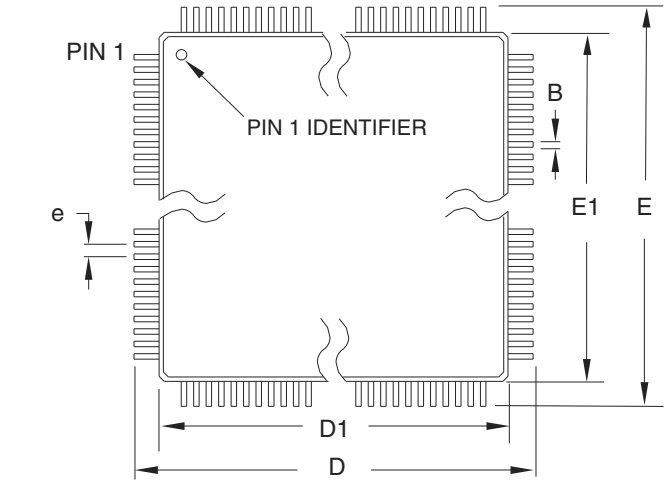
Device Migration	Package	Packing	Previous Ordering Code	New Ordering Code
AT89C51RD2 to AT89LP51RD2	PLCC44	Stick	AT89C51RD2-SLSUM	AT89LP51RD2-20JU
		Reel	AT89C51RD2-SLRUM	AT89LP51RD2-20JUR
	VQFP44	Tray	AT89C51RD2-RLTUM	AT89LP51RD2-20AAU
		Reel	AT89C51RD2-RLRUM	AT89LP51RD2-20AAUR
AT89C51ED2 to AT89LP51ED2	PLCC44	Stick	AT89C51ED2-SLSUM	AT89LP51ED2-20JU
		Reel	AT89C51ED2-SLRUM	AT89LP51ED2-20JUR
	VQFP44	Tray	AT89C51ED2-RLTUM	AT89LP51ED2-20AAU
		Reel	AT89C51ED2-RLRUM	AT89LP51ED2-20AAUR
AT89C51ID2 to AT89LP51ID2	PLCC44	Stick	AT89C51ID2-SLSUM	AT89LP51ID2-20JU
		Reel	AT89C51ID2-SLRUM	AT89LP51ID2-20JUR
	VQFP44	Tray	AT89C51ID2-RLTUM	AT89LP51ID2-20AAU
		Reel	AT89C51ID2-RLRUM	AT89LP51ID2-20AAUR

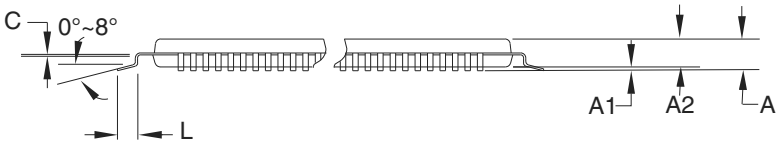
Table 4-2. Packages Not Found in AT89C51RD2/ED2/ID2

Device	Package	Packing	Ordering Code
AT89C51RD2 to AT89LP51RD2	PDIP40	Stick	AT89LP51RD2-20PU
	TQFP44	Tray	AT89LP51RD2-20AU
		Reel	AT89LP51RD2-20AUR
	VQFN44	Tray	AT89LP51RD2-20MU
		Reel	AT89LP51RD2-20MUR
AT89C51ED2 to AT89LP51ED2	PDIP40	Stick	AT89LP51ED2-20PU
	TQFP44	Tray	AT89LP51ED2-20AU
		Reel	AT89LP51ED2-20AUR
	VQFN44	Tray	AT89LP51ED2-20MU
		Reel	AT89LP51ED2-20MUR
AT89C51ID2 to AT89LP51ID2	PDIP40	Stick	AT89LP51ID2-20PU
	TQFP44	Tray	AT89LP51ID2-20AU
		Reel	AT89LP51ID2-20AUR
	VQFN44	Tray	AT89LP51ID2-20MU
		Reel	AT89LP51ID2-20MUR

5. Packaging Information

5.1 44AA – VQFP/LQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

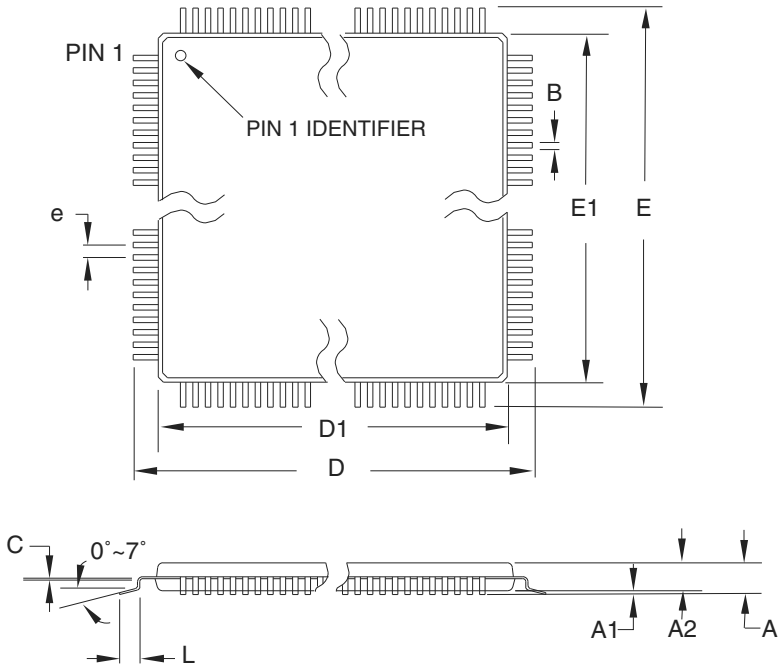
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	0.95	1.40	1.05	
D	11.9	12.00	12.10	
D1	9.90	10.00	10.10	Note 2
E	11.9	12.00	12.10	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.102 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44AA,** 44-lead, 10 x 10 mm Body Size, 1.4 mm Body Thickness, 0.8 mm Lead Pitch, Low Profile Plastic Quad Flat Package (VQFP)	44AA	B

5.2 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

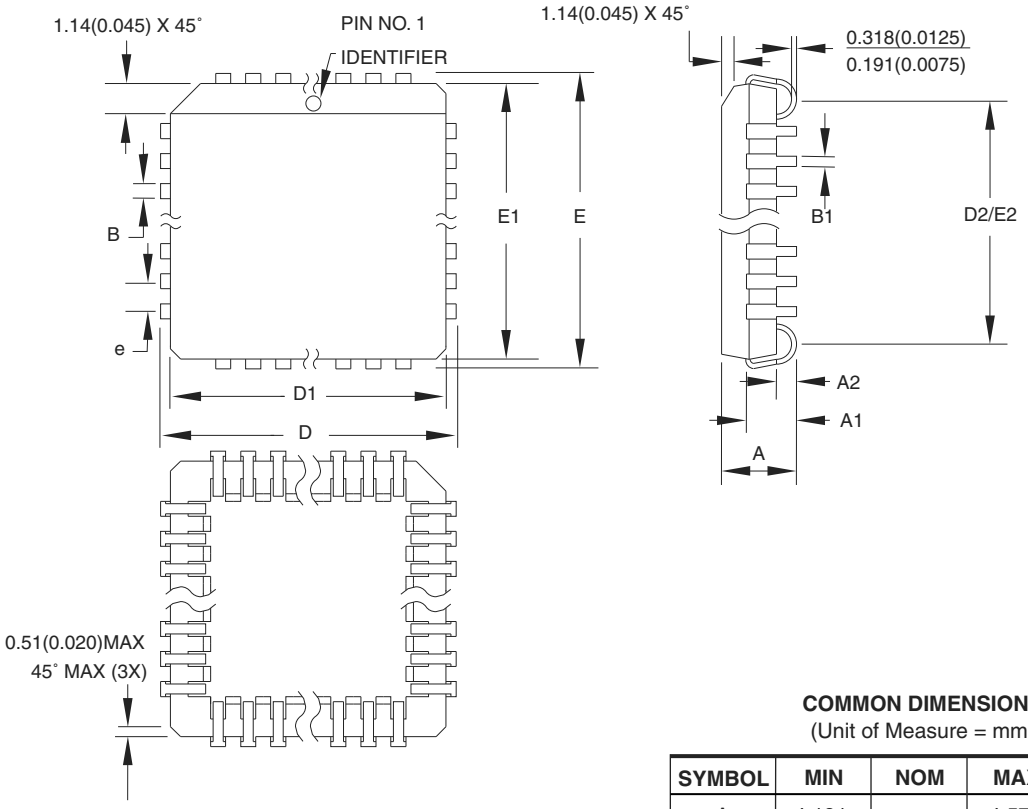
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

5.3 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

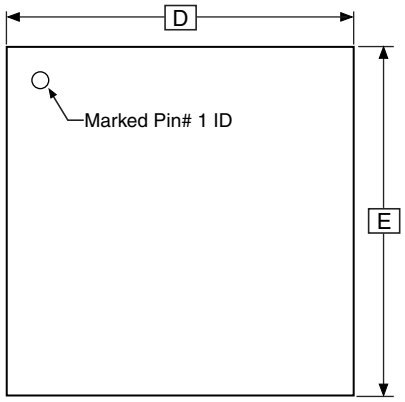
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

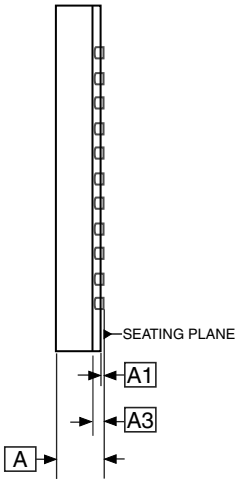
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

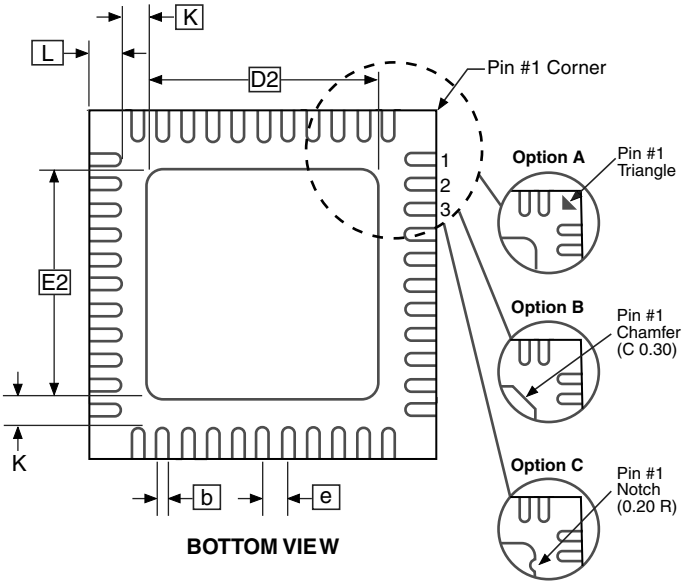
5.4 44M1 – VQFN/MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

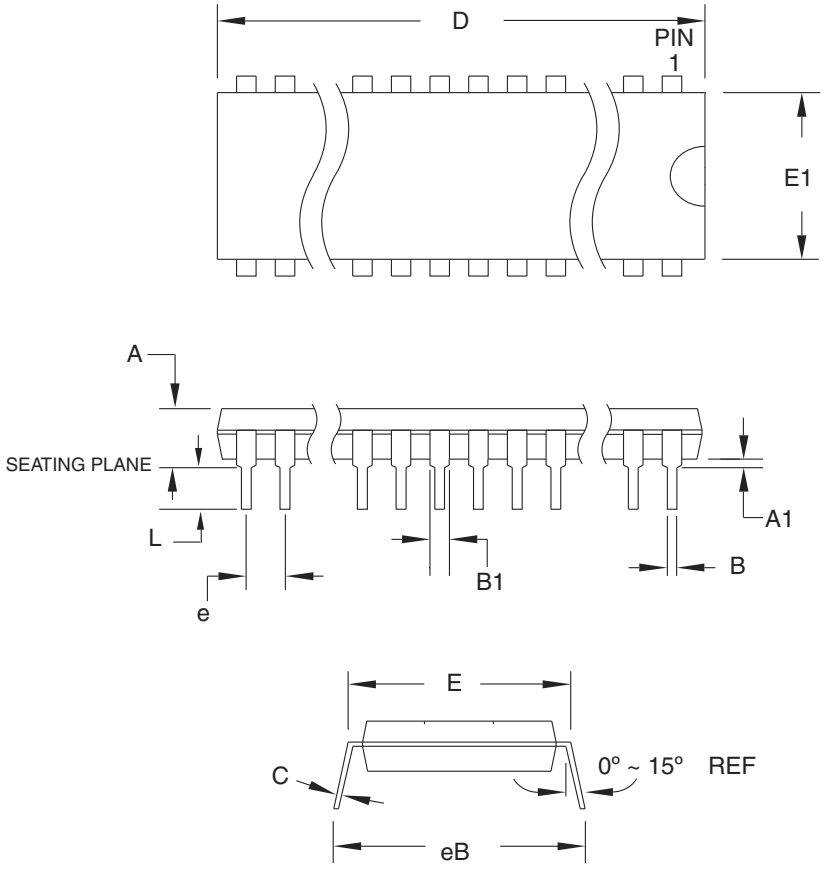
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

9/26/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**44M1,** 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	ZWS	44M1	H

5.5 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

6. Revision History

Revision No.	History
Revision A – July 2011	• Initial Release

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