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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gp502-h-ss

FIGURE 3-2: PROGRAMMER'S MODEL

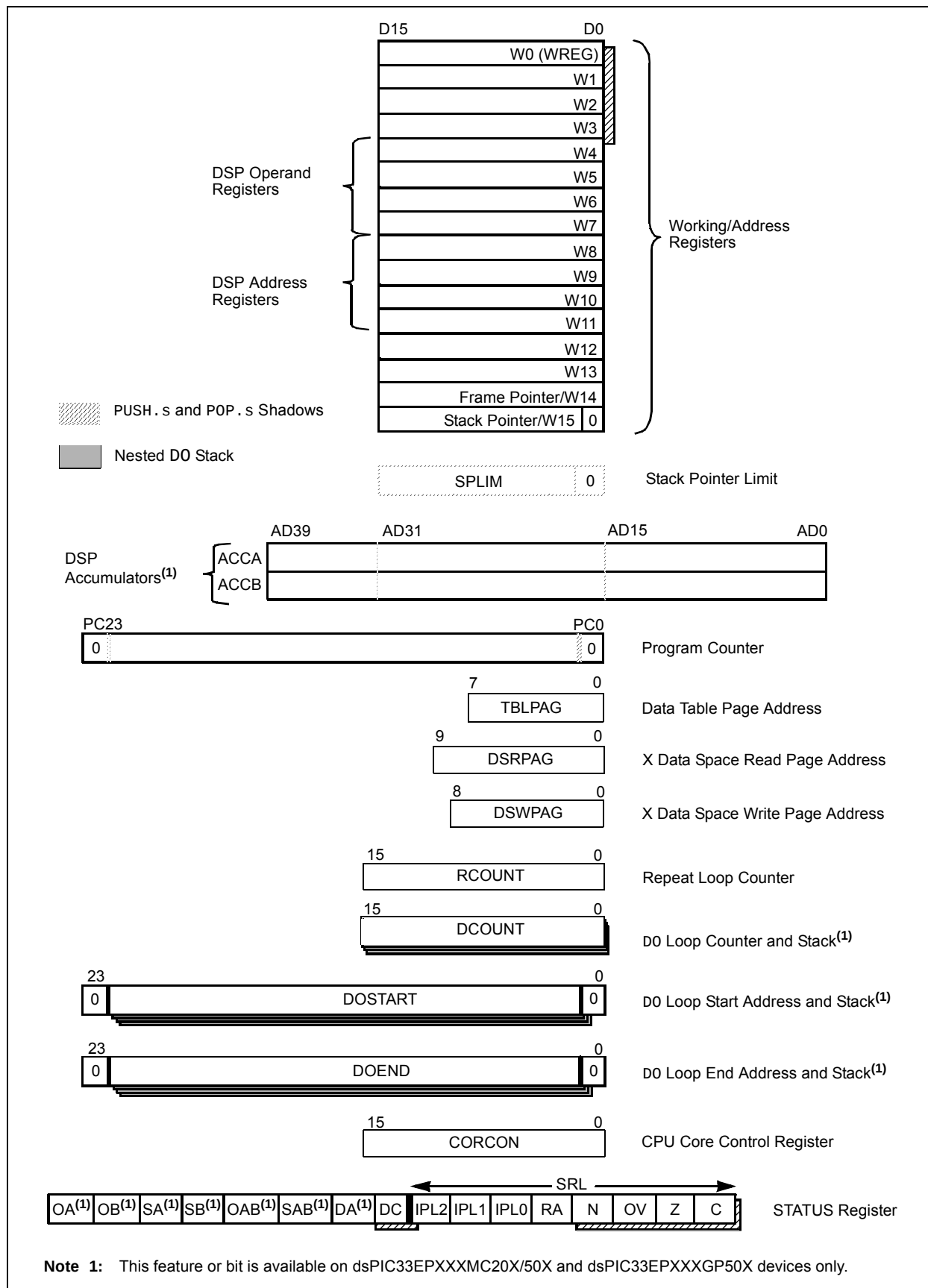


TABLE 4-9: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
IC1CON1	0140	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000	
IC1CON2	0142	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D	
IC1BUF	0144	Input Capture 1 Buffer Register																	xxxx
IC1TMR	0146	Input Capture 1 Timer																	0000
IC2CON1	0148	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000	
IC2CON2	014A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D	
IC2BUF	014C	Input Capture 2 Buffer Register																	xxxx
IC2TMR	014E	Input Capture 2 Timer																	0000
IC3CON1	0150	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000	
IC3CON2	0152	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D	
IC3BUF	0154	Input Capture 3 Buffer Register																	xxxx
IC3TMR	0156	Input Capture 3 Timer																	0000
IC4CON1	0158	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000	
IC4CON2	015A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D	
IC4BUF	015C	Input Capture 4 Buffer Register																	xxxx
IC4TMR	015E	Input Capture 4 Timer																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	—	—	—
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
Reserved	29-31	21-23	0x00003E-0x000042	—	—	—
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready ⁽¹⁾	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event ⁽¹⁾	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47-56	39-48	0x000062-0x000074	—	—	—
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
Reserved	59-64	51-56	0x00007A-0x000084	—	—	—
PSEM – PWM Special Event Match ⁽²⁾	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

Note 2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work-arounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, “RPn” or “RPI n”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions, while “RPI” indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C™ and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

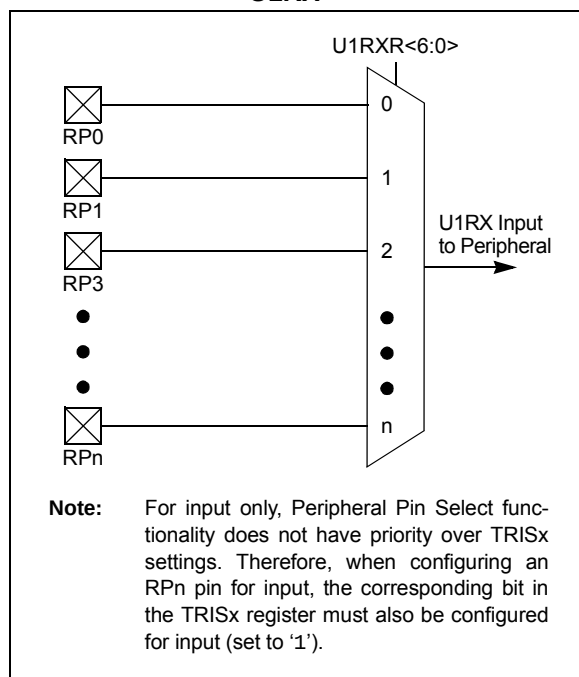
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPNR_x registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPN pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 “Op Amp/Comparator Module”**), and the PTG module (see **Section 24.0 “Peripheral Trigger Generator (PTG) Module”**).

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QE1 module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 “Quadrature Encoder Interface (QE1) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”**).

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPNR12 register to the value of 'b00000001', the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QE1 module allows peripherals to be connected to the QE1 digital filter input. To utilize this filter, the QE1 module must be enabled and its inputs must be connected to a physical RPN pin. Example 11-2 illustrates how the input capture module can be connected to the QE1 digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QE1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

```

RPNR15 = 0x2500;    /* Connect the QE1 HOME1 input to RP37 (pin 43) */
RPNR7  = 0x009;    /* Connect the IC1 input to the digital filter on the FHOME1 input */

QE1IIOC = 0x4000;   /* Enable the QE1 digital filter */
QE1ICON = 0x8000;   /* Enable the QE1 module */

```

16.3 PWMx Control Registers

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU ⁽¹⁾	SYNCPOL ⁽¹⁾	SYNCOEN ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN ⁽¹⁾	SYNCSRC2 ⁽¹⁾	SYNCSRC1 ⁽¹⁾	SYNCSRC0 ⁽¹⁾	SEVTPS3 ⁽¹⁾	SEVTPS2 ⁽¹⁾	SEVTPS1 ⁽¹⁾	SEVTPS0 ⁽¹⁾
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15 **PTEN:** PWMx Module Enable bit
1 = PWMx module is enabled
0 = PWMx module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PTSIDL:** PWMx Time Base Stop in Idle Mode bit
1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode
- bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending
- bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled
- bit 10 **EIPU:** Enable Immediate Period Updates bit⁽¹⁾
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWMx cycle boundaries
- bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit⁽¹⁾
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
0 = SYNCI1/SYNCO1 is active-high
- bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit⁽¹⁾
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled
- bit 7 **SYNCEN:** External Time Base Synchronization Enable bit⁽¹⁾
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

2: See Section 24.0 “Peripheral Trigger Generator (PTG) Module” for information on this selection.

REGISTER 17-10: INDX1HLD: INDEX COUNTER 1 HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INDXHLD<15:0>**: Hold Register for Reading and Writing INDX1CNTH bits

REGISTER 17-11: QE11ICH: QE11 INITIALIZATION/CAPTURE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QE11IC<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QE11IC<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **QE11IC<31:16>**: High Word Used to Form 32-Bit Initialization/Capture Register (QE11IC) bits

REGISTER 17-12: QE11ICL: QE11 INITIALIZATION/CAPTURE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QE11IC<15:8>							
bit 15				bit 8			

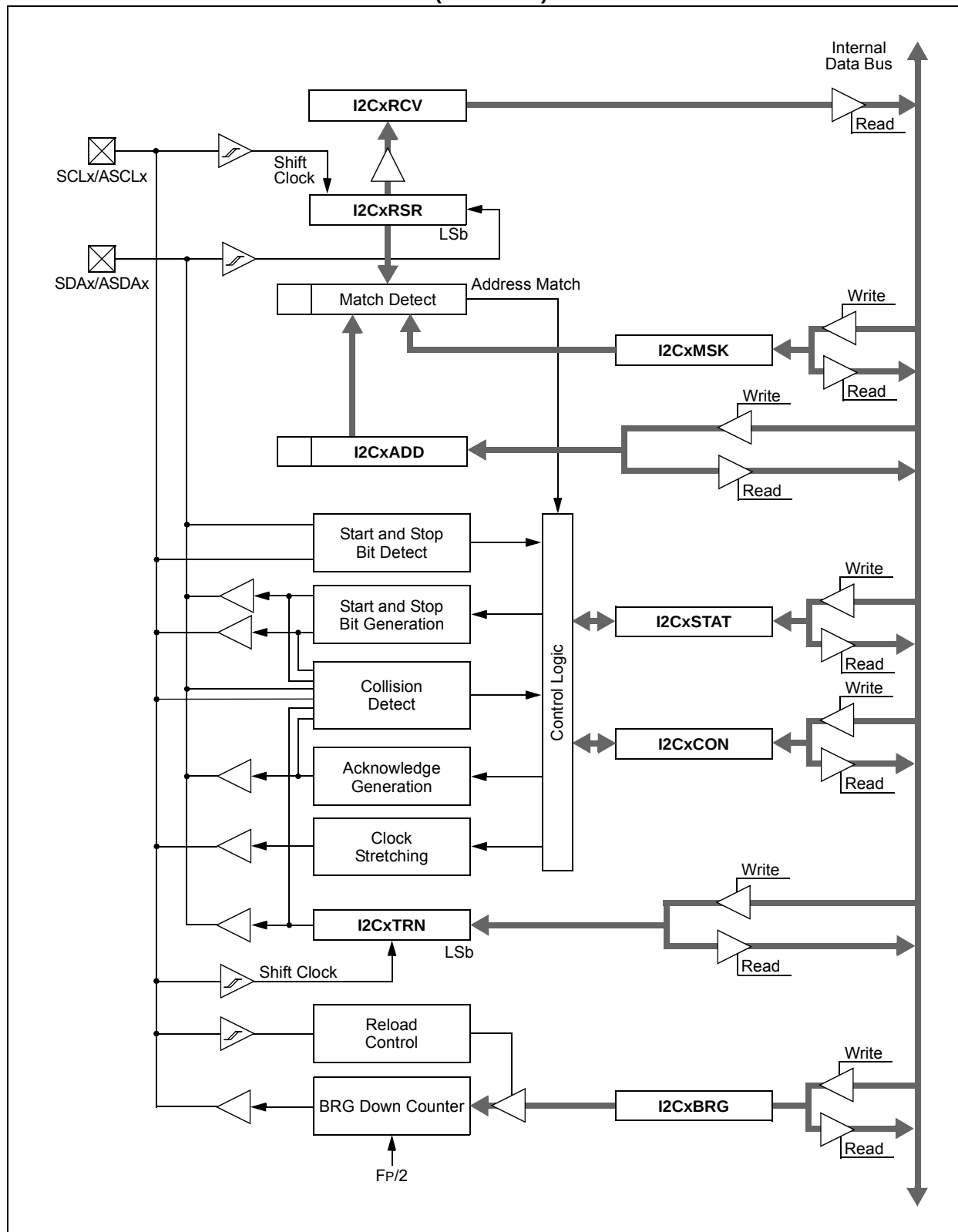
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QE11IC<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **QE11IC<15:0>**: Low Word Used to Form 32-Bit Initialization/Capture Register (QE11IC) bits

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)



REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit						
R = Readable bit	W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
 1 = Module attempted to write to a full buffer (set by module)
 0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit						
R = Readable bit	W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
 1 = Module attempted to write to a full buffer (set by module)
 0 = No overflow condition (cleared by user software)

**REGISTER 25-4: CMxMSKSRG: COMPARATOR x MASK SOURCE SELECT
CONTROL REGISTER (CONTINUED)**

bit 3-0 **SELSRCA<3:0>**: Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	CVR2OE ⁽¹⁾	—	—	—	VREFSEL	—	—
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVR1OE ⁽¹⁾	CVRR	CVRSS ⁽²⁾	CVR3	CVR2	CVR1	CVR0
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **CVR2OE:** Comparator Voltage Reference 2 Output Enable bit⁽¹⁾
 1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin
 0 = (AVDD – AVSS)/2 is disconnected from the CVREF2O pin
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **VREFSEL:** Comparator Voltage Reference Select bit
 1 = CVREFIN = VREF+
 0 = CVREFIN is generated by the resistor network
- bit 9-8 **Unimplemented:** Read as '0'
- bit 7 **CVREN:** Comparator Voltage Reference Enable bit
 1 = Comparator voltage reference circuit is powered on
 0 = Comparator voltage reference circuit is powered down
- bit 6 **CVR1OE:** Comparator Voltage Reference 1 Output Enable bit⁽¹⁾
 1 = Voltage level is output on the CVREF1O pin
 0 = Voltage level is disconnected from then CVREF1O pin
- bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
 1 = CVRSRC/24 step-size
 0 = CVRSRC/32 step-size
- bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit⁽²⁾
 1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)
 0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS
- bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection $0 \leq \text{CVR<3:0>} \leq 15$ bits
 When CVRR = 1:
 $\text{CVREFIN} = (\text{CVR<3:0>}/24) \cdot (\text{CVRSRC})$
 When CVRR = 0:
 $\text{CVREFIN} = (\text{CVRSRC}/4) + (\text{CVR<3:0>}/32) \cdot (\text{CVRSRC})$

Note 1: CVR_xOE overrides the TRIS_x and the ANSEL_x bit settings.

2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
9	BTG	BTG f, #bit4	Bit Toggle f	1	1	None
		BTG ws, #bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC f, #bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC ws, #bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS f, #bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS ws, #bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST f, #bit4	Bit Test f	1	1	Z
		BTST.C ws, #bit4	Bit Test Ws to C	1	1	C
		BTST.Z ws, #bit4	Bit Test Ws to Z	1	1	Z
		BTST.C ws, Wb	Bit Test Ws<Wb> to C	1	1	C
		BTST.Z ws, Wb	Bit Test Ws<Wb> to Z	1	1	Z
13	BTSTS	BTSTS f, #bit4	Bit Test then Set f	1	1	Z
		BTSTS.C ws, #bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z ws, #bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL lit23	Call subroutine	2	4	SFA
		CALL Wn	Call indirect subroutine	1	4	SFA
		CALL.L Wn	Call indirect subroutine (long address)	1	4	SFA
15	CLR	CLR f	f = 0x0000	1	1	None
		CLR WREG	WREG = 0x0000	1	1	None
		CLR ws	Ws = 0x0000	1	1	None
		CLR Acc, Wx, Wxd, Wy, Wyd, AWB ⁽¹⁾	Clear Accumulator	1	1	OA, OB, SA, SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO, Sleep
17	COM	COM f	f = $\bar{f}$	1	1	N, Z
		COM f, WREG	WREG = $\bar{f}$	1	1	N, Z
		COM ws, Wd	Wd = $\overline{Ws}$	1	1	N, Z
18	CP	CP f	Compare f with WREG	1	1	C, DC, N, OV, Z
		CP Wb, #lit8	Compare Wb with lit8	1	1	C, DC, N, OV, Z
		CP Wb, Ws	Compare Wb with Ws (Wb – Ws)	1	1	C, DC, N, OV, Z
19	CP0	CP0 f	Compare f with 0x0000	1	1	C, DC, N, OV, Z
		CP0 ws	Compare Ws with 0x0000	1	1	C, DC, N, OV, Z
20	CPB	CPB f	Compare f with WREG, with Borrow	1	1	C, DC, N, OV, Z
		CPB Wb, #lit8	Compare Wb with lit8, with Borrow	1	1	C, DC, N, OV, Z
		CPB Wb, Ws	Compare Wb with Ws, with Borrow (Wb – Ws – C)	1	1	C, DC, N, OV, Z
21	CPSEQ	CPSEQ Wb, Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ Wb, Wn, Expr	Compare Wb with Wn, branch if =	1	1 (5)	None
22	CPSGT	CPSGT Wb, Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT Wb, Wn, Expr	Compare Wb with Wn, branch if >	1	1 (5)	None
23	CPSLT	CPSLT Wb, Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
	CPBLT	CPBLT Wb, Wn, Expr	Compare Wb with Wn, branch if <	1	1 (5)	None
24	CPSNE	CPSNE Wb, Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
	CPBNE	CPBNE Wb, Wn, Expr	Compare Wb with Wn, branch if ≠	1	1 (5)	None

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

30.1 DC Characteristics

TABLE 30-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Maximum MIPS
			dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X
—	3.0V to 3.6V ⁽¹⁾	-40°C to +85°C	70
—	3.0V to 3.6V ⁽¹⁾	-40°C to +125°C	60

Note 1: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $I/O = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	$(T_J - T_A)/\theta_{JA}$			W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin QFN	θ_{JA}	28.0	—	°C/W	1
Package Thermal Resistance, 64-Pin TQFP 10x10 mm	θ_{JA}	48.3	—	°C/W	1
Package Thermal Resistance, 48-Pin UQFN 6x6 mm	θ_{JA}	41	—	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θ_{JA}	29.0	—	°C/W	1
Package Thermal Resistance, 44-Pin TQFP 10x10 mm	θ_{JA}	49.8	—	°C/W	1
Package Thermal Resistance, 44-Pin VTLA 6x6 mm	θ_{JA}	25.2	—	°C/W	1
Package Thermal Resistance, 36-Pin VTLA 5x5 mm	θ_{JA}	28.5	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θ_{JA}	30.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θ_{JA}	71.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	69.7	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	60.0	—	°C/W	1

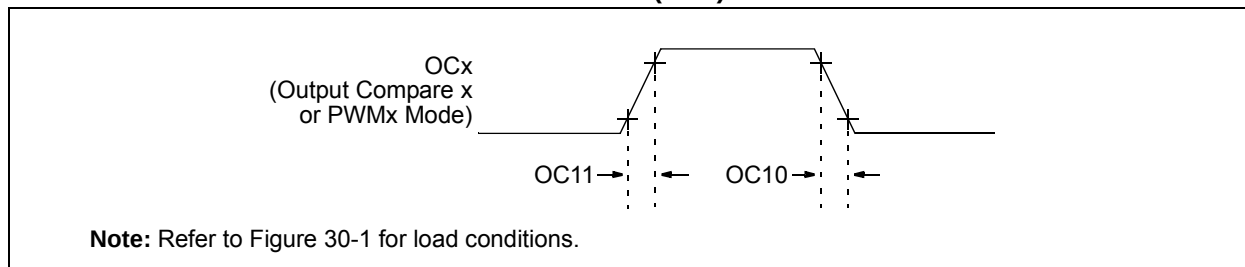
Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended	
Parameter No.	Typ.	Max.	Units	Conditions
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X and PIC24EP32GP/MC20X				
DC60d	30	100	μA	-40°C
DC60a	35	100	μA	+25°C
DC60b	150	200	μA	+85°C
DC60c	250	500	μA	+125°C
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X and PIC24EP64GP/MC20X				
DC60d	25	100	μA	-40°C
DC60a	30	100	μA	+25°C
DC60b	150	350	μA	+85°C
DC60c	350	800	μA	+125°C
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X and PIC24EP128GP/MC20X				
DC60d	30	100	μA	-40°C
DC60a	35	100	μA	+25°C
DC60b	150	350	μA	+85°C
DC60c	550	1000	μA	+125°C
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X and PIC24EP256GP/MC20X				
DC60d	35	100	μA	-40°C
DC60a	40	100	μA	+25°C
DC60b	250	450	μA	+85°C
DC60c	1000	1200	μA	+125°C
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X and PIC24EP512GP/MC20X				
DC60d	40	100	μA	-40°C
DC60a	45	100	μA	+25°C
DC60b	350	800	μA	+85°C
DC60c	1100	1500	μA	+125°C

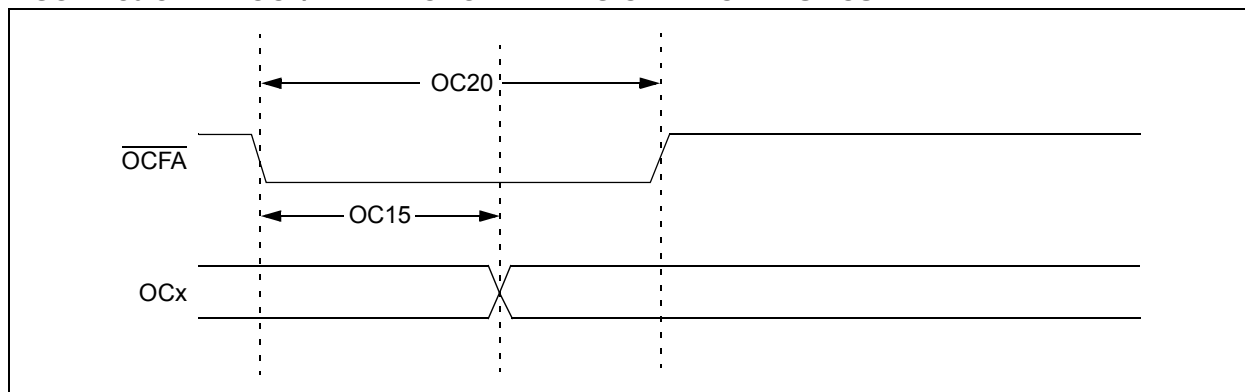
Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- MCLR = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS**TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS**TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	—	$T_{CY} + 20$	ns	
OC20	TFLT	Fault Input Pulse Width	$T_{CY} + 20$	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

**TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesser of FP or 15	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

Revision C (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see **Section 20.1 “UART Helpful Tips”** and **Section 3.6 “CPU Resources”**.

All occurrences of TLA were updated to VTLA throughout the document, with the exception of the pin diagrams (updated diagrams were not available at time of publication).

A new chapter, **Section 31.0 “DC and AC Device Characteristics Graphs”**, was added.

All other major changes are referenced by their respective section in Table A-2.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
“16-bit Microcontrollers and Digital Signal Controllers (up to 256-Kbyte Flash and 32-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog”	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an “at-a-glance” format.
Section 1.0 “Device Overview”	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X Block Diagram (see Figure 1-1), which now contains a CPU block and a reference to the CPU diagram. Updated the description and Note references in the Pinout I/O Descriptions for these pins: C1IN2-, C2IN2-, C3IN2-, OA1OUT, OA2OUT, and OA3OUT (see Table 1-1).
Section 2.0 “Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers”	Updated the Recommended Minimum Connection diagram (see Figure 2-1).
Section 3.0 “CPU”	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU Block Diagram (see Figure 3-1). Updated the Status register definition in the Programmer’s Model (see Figure 3-2).
Section 4.0 “Memory Organization”	Updated the Data Memory Maps (see Figure 4-6 and Figure 4-11). Removed the DCB<1:0> bits from the OC1CON2, OC2CON2, OC3CON2, and OC4CON2 registers in the Output Compare 1 Through Output Compare 4 Register Map (see Table 4-10). Added the TRIG1 and TRGCON1 registers to the PWM Generator 1 Register Map (see Table 4-13). Added the TRIG2 and TRGCON2 registers to the PWM Generator 2 Register Map (see Table 4-14). Added the TRIG3 and TRGCON3 registers to the PWM Generator 3 Register Map (see Table 4-15). Updated the second note in Section 4.7.1 “Bit-Reversed Addressing Implementation” .
Section 8.0 “Direct Memory Access (DMA)”	Updated the DMA Controller diagram (see Figure 8-1).
Section 14.0 “Input Capture”	Updated the bit values for the ICx clock source of the ICTSEL<12:10> bits in the ICxCON1 register (see Register 14-1).
Section 15.0 “Output Compare”	Updated the bit values for the OCx clock source of the OCTSEL<2:0> bits in the OCxCON1 register (see Register 15-1). Removed the DCB<1:0> bits from the Output Compare x Control Register 2 (see Register 15-2).

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