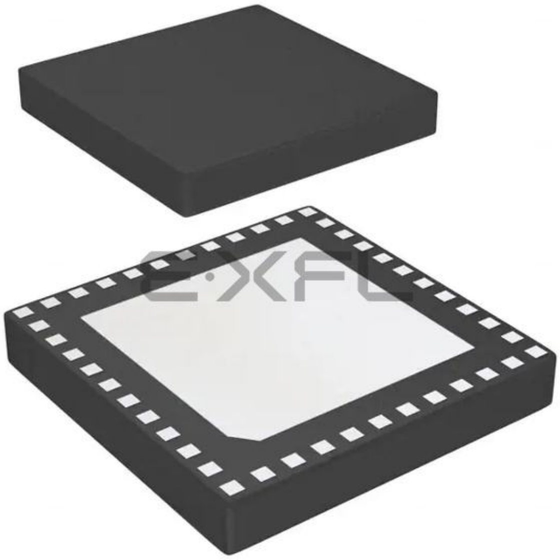
Microchip Technology - DSPIC33EP128GP504T-I/TL Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gp504t-i-tl

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)

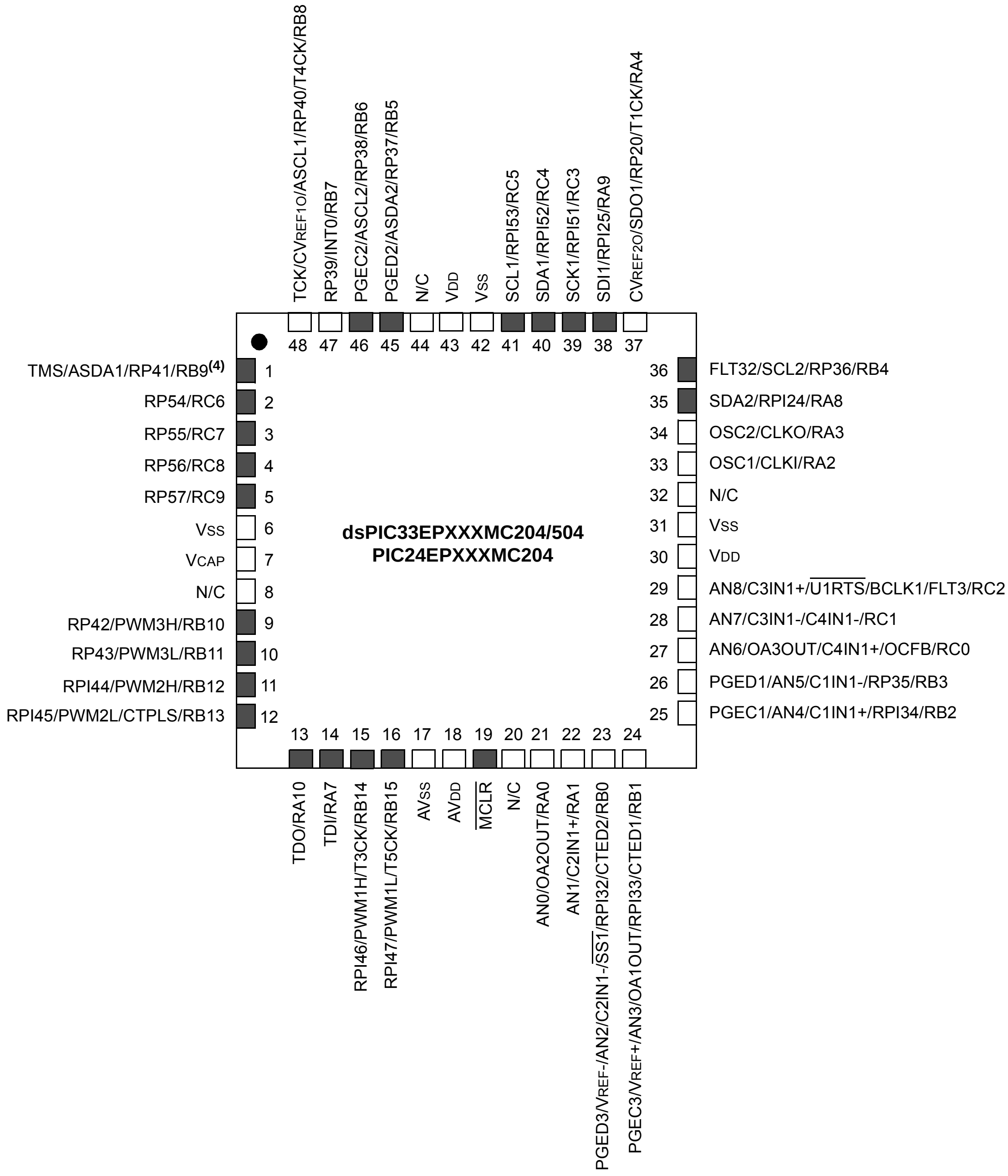
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals									I^2C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM(4) (Channels)	Quadrature Encoder Interface	UART	SPI(2)	ECAN™ Technology	External Interrupts(3)									
dsPIC33EP32MC504	512	32	4	5	4	4	6	1	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA(5), TQFP, QFN, UQFN
dsPIC33EP64MC504	1024	64	8																		
dsPIC33EP128MC504	1024	128	16																		
dsPIC33EP256MC504	1024	256	32																		
dsPIC33EP512MC504	1024	512	48																		
dsPIC33EP64MC506	1024	64	8	5	4	4	6	1	2	2	1	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP128MC506	1024	128	16																		
dsPIC33EP256MC506	1024	256	32																		
dsPIC33EP512MC506	1024	512	48																		

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 “Op Amp/Comparator Module”** for details.
2: Only SPI2 is remappable.
3: INT0 is not remappable.
4: Only the PWM Faults are remappable.
5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

Pin Diagrams (Continued)

48-Pin UQFN(1,2,3)

■ = Pins are up to 5V tolerant



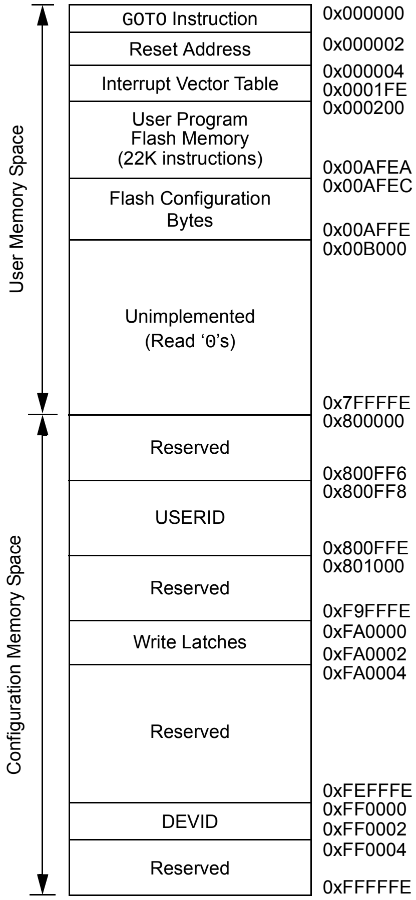
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 “I/O Ports”** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, which apply to dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the `MOV` instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 `MAC` INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MPY`, `MPY.N`, `MOVSAC` and `MSC`), also referred to as `MAC` instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the `MAC` class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, `BRA` (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the `DISI` instruction uses a 14-bit unsigned literal field. In some instructions, such as `ULNK`, the source of an operand or result is implied by the opcode itself. Certain operations, such as a `NOP`, do not have any operands.

REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	AMODE1	AMODE0	—	—	MODE1	MODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CHEN:** DMA Channel Enable bit
`1` = Channel is enabled
`0` = Channel is disabled

bit 14 **SIZE:** DMA Data Transfer Size bit
`1` = Byte
`0` = Word

bit 13 **DIR:** DMA Transfer Direction bit (source/destination bus select)
`1` = Reads from RAM address, writes to peripheral address
`0` = Reads from peripheral address, writes to RAM address

bit 12 **HALF:** DMA Block Transfer Interrupt Select bit
`1` = Initiates interrupt when half of the data has been moved
`0` = Initiates interrupt when all of the data has been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
`1` = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
`0` = Normal operation

bit 10-6 **Unimplemented:** Read as ‘`0`’

bit 5-4 **AMODE<1:0>:** DMA Channel Addressing Mode Select bits
`11` = Reserved
`10` = Peripheral Indirect Addressing mode
`01` = Register Indirect without Post-Increment mode
`00` = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as ‘`0`’

bit 1-0 **MODE<1:0>:** DMA Channel Operating Mode Select bits
`11` = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
`10` = Continuous, Ping-Pong modes are enabled
`01` = One-Shot, Ping-Pong modes are disabled
`00` = Continuous, Ping-Pong modes are disabled

9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2(2)	NOSC1(2)	NOSC0(2)
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF(3)	—	—	OSWEN
bit 7							bit 0

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘`0`’

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)

`111` = Fast RC Oscillator (FRC) with Divide-by-n
`110` = Fast RC Oscillator (FRC) with Divide-by-16
`101` = Low-Power RC Oscillator (LPRC)
`100` = Reserved
`011` = Primary Oscillator (XT, HS, EC) with PLL
`010` = Primary Oscillator (XT, HS, EC)
`001` = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
`000` = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as ‘`0`’

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)

`111` = Fast RC Oscillator (FRC) with Divide-by-n
`110` = Fast RC Oscillator (FRC) with Divide-by-16
`101` = Low-Power RC Oscillator (LPRC)
`100` = Reserved
`011` = Primary Oscillator (XT, HS, EC) with PLL
`010` = Primary Oscillator (XT, HS, EC)
`001` = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
`000` = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit

`1` = If (FCKSM0 = `1`), then clock and PLL configurations are locked; if (FCKSM0 = `0`), then clock and PLL configurations may be modified
`0` = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit

`1` = I/O lock is active
`0` = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)

`1` = Indicates that PLL is in lock or PLL start-up timer is satisfied
`0` = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1: Writes to this register require an unlock sequence. Refer to **“Oscillator”** (DS70580) in the *“dsPIC33/PIC24 Family Reference Manual”* (available from the Microchip web site) for details.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: This bit should only be cleared in software. Setting the bit in software (= `1`) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 "Peripheral Module Disable"**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the `PWRSAV` instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSAV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

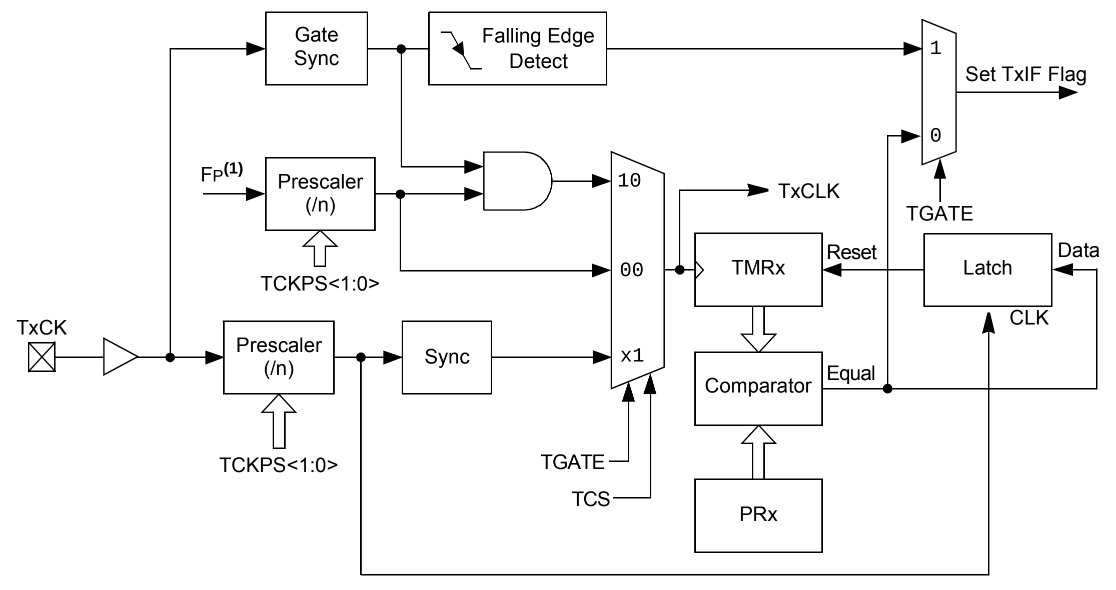
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC2R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC1R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

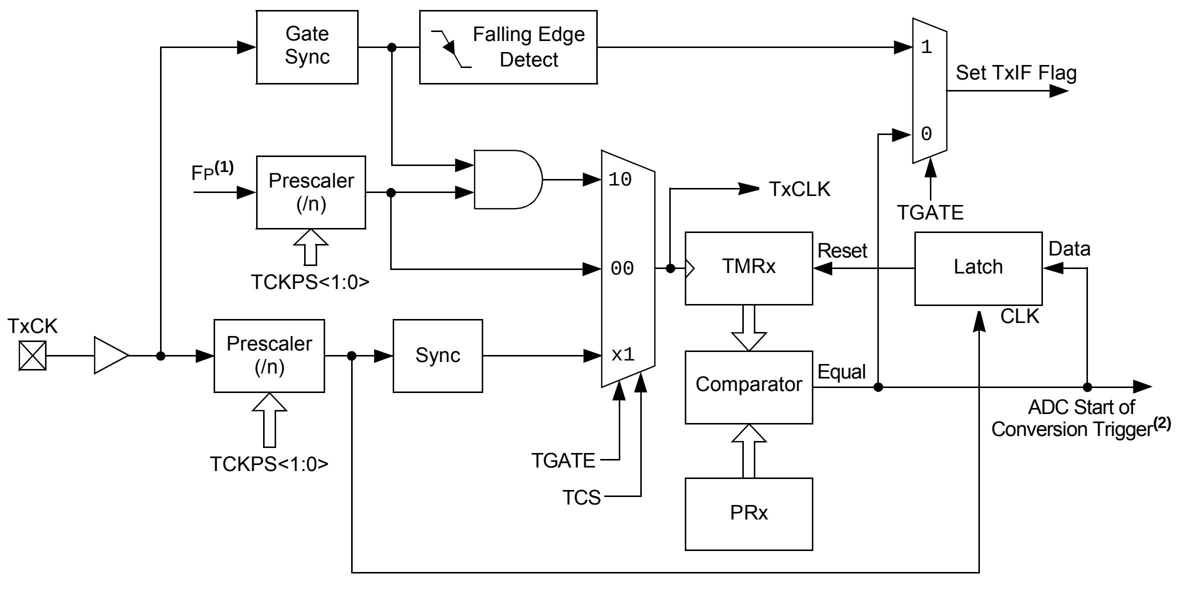
bit 15	**Unimplemented:** Read as ‘`0`’
bit 14-8	**IC2R<6:0>:** Assign Input Capture 2 (IC2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) `1111001` = Input tied to RPI121 . . . `0000001` = Input tied to CMP1 `0000000` = Input tied to VSS
bit 7	**Unimplemented:** Read as ‘`0`’
bit 6-0	**IC1R<6:0>:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) `1111001` = Input tied to RPI121 . . . `0000001` = Input tied to CMP1 `0000000` = Input tied to VSS

FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)



Note 1: FP is the peripheral clock.

FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)



Note 1: FP is the peripheral clock.
2: The ADC trigger is available on TMR3 and TMR5 only.

19.2 I²C Control Registers

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN[1]	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15	**I2CEN:** I2Cx Enable bit `1` = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins `0` = Disables the I2Cx module; all I²C™ pins are controlled by port functions
bit 14	**Unimplemented:** Read as ‘`0`’
bit 13	**I2CSIDL:** I2Cx Stop in Idle Mode bit `1` = Discontinues module operation when device enters an Idle mode `0` = Continues module operation in Idle mode
bit 12	**SCLREL:** SCLx Release Control bit (when operating as I²C slave) `1` = Releases SCLx clock `0` = Holds SCLx clock low (clock stretch) If STREN = `1`: Bit is R/W (i.e., software can write ‘`0`’ to initiate stretch and write ‘`1`’ to release clock). Hardware is clear at the beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception. Hardware is clear at the end of every slave data byte reception. If STREN = `0`: Bit is R/S (i.e., software can only write ‘`1`’ to release clock). Hardware is clear at the beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception.
bit 11	**IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit[1] `1` = IPMI mode is enabled; all addresses are Acknowledged `0` = IPMI mode disabled
bit 10	**A10M:** 10-Bit Slave Address bit `1` = I2CxADD is a 10-bit slave address `0` = I2CxADD is a 7-bit slave address
bit 9	**DISSLW:** Disable Slew Rate Control bit `1` = Slew rate control is disabled `0` = Slew rate control is enabled
bit 8	**SMEN:** SMBus Input Levels bit `1` = Enables I/O pin thresholds compliant with SMBus specification `0` = Disables SMBus input thresholds
bit 7	**GCEN:** General Call Enable bit (when operating as I²C slave) `1` = Enables interrupt when a general call address is received in I2CxRSR (module is enabled for reception) `0` = General call address disabled

Note 1: When performing master operations, ensure that the IPMIEN bit is set to ‘`0`’.

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT(2)	PTGSSEN(3)	PTGIVIS
bit 15							bit 8

R/W-0	HS-0	U-0	U-0	U-0	U-0	R/W-0	
PTGSTRT	PTGWDTO	—	—	—	—	PTGITM1(1)	PTGITM0(1)
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PTGEN:** Module Enable bit

1 = PTG module is enabled
0 = PTG module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **PTGSIDL:** PTG Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **PTGTOGL:** PTG TRIG Output Toggle Mode bit

1 = Toggle state of the PTGOx for each execution of the `PTGTRIG` command
0 = Each execution of the `PTGTRIG` command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits

bit 11 **Unimplemented:** Read as ‘0’

bit 10 **PTGSWT:** PTG Software Trigger bit(2)

1 = Triggers the PTG module
0 = No action (clearing this bit will have no effect)

bit 9 **PTGSSEN:** PTG Enable Single-Step bit(3)

1 = Enables Single-Step mode
0 = Disables Single-Step mode

bit 8 **PTGIVIS:** PTG Counter/Timer Visibility Control bit

1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers

bit 7 **PTGSTRT:** PTG Start Sequencer bit

1 = Starts to sequentially execute commands (Continuous mode)
0 = Stops executing commands

bit 6 **PTGWDTO:** PTG Watchdog Timer Time-out Status bit

1 = PTG Watchdog Timer has timed out
0 = PTG Watchdog Timer has not timed out.

bit 5-2 **Unimplemented:** Read as ‘0’

Note 1: These bits apply to the `PTGWHI` and `PTGWLO` commands only.
2: This bit is only used with the `PTGCTRL` step command software trigger option.
3: Use of the PTG Single-Step mode is reserved for debugging tools only.

REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **HLMS:** High or Low-Level Masking Select bits
`1` = The masking (blanking) function will prevent any asserted (‘`0`’) comparator signal from propagating
`0` = The masking (blanking) function will prevent any asserted (‘`1`’) comparator signal from propagating

bit 14 **Unimplemented:** Read as ‘`0`’

bit 13 **OCEN:** OR Gate C Input Enable bit
`1` = MCI is connected to OR gate
`0` = MCI is not connected to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
`1` = Inverted MCI is connected to OR gate
`0` = Inverted MCI is not connected to OR gate

bit 11 **OBEN:** OR Gate B Input Enable bit
`1` = MBI is connected to OR gate
`0` = MBI is not connected to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
`1` = Inverted MBI is connected to OR gate
`0` = Inverted MBI is not connected to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
`1` = MAI is connected to OR gate
`0` = MAI is not connected to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
`1` = Inverted MAI is connected to OR gate
`0` = Inverted MAI is not connected to OR gate

bit 7 **NAGS:** AND Gate Output Inverted Enable bit
`1` = Inverted ANDI is connected to OR gate
`0` = Inverted ANDI is not connected to OR gate

bit 6 **PAGS:** AND Gate Output Enable bit
`1` = ANDI is connected to OR gate
`0` = ANDI is not connected to OR gate

bit 5 **ACEN:** AND Gate C Input Enable bit
`1` = MCI is connected to AND gate
`0` = MCI is not connected to AND gate

bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
`1` = Inverted MCI is connected to AND gate
`0` = Inverted MCI is not connected to AND gate

TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit `1` = 1:128 `0` = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits `1111` = 1:32,768 `1110` = 1:16,384 • • • `0001` = 1:2 `0000` = 1:1
WDTWIN<1:0>	Watchdog Window Select bits `11` = WDT window is 25% of WDT period `10` = WDT window is 37.5% of WDT period `01` = WDT window is 50% of WDT period `00` = WDT window is 75% of WDT period
ALTI2C1	Alternate I2C1 pin `1` = I2C1 is mapped to the SDA1/SCL1 pins `0` = I2C1 is mapped to the ASDA1/ASCL1 pins
ALTI2C2	Alternate I2C2 pin `1` = I2C2 is mapped to the SDA2/SCL2 pins `0` = I2C2 is mapped to the ASDA2/ASCL2 pins
JTAGEN[2]	JTAG Enable bit `1` = JTAG is enabled `0` = JTAG is disabled
ICS<1:0>	ICD Communication Channel Select bits `11` = Communicate on PGEC1 and PGED1 `10` = Communicate on PGEC2 and PGED2 `01` = Communicate on PGEC3 and PGED3 `00` = Reserved, do not use

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = `1`, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = `1`. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS(3)	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V(3)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V(3)	-0.3V to +3.6V
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin(2)	300 mA
Maximum current sunk/sourced by any 4x I/O pin	15 mA
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports(2,4)	200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: See the **“Pin Diagrams”** section for the 5V tolerant pins.

4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

TABLE 30-14: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.[1]**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	3.0	—	3.6	V	
D132b	VPEW	VDD for Self-Timed Write	3.0	—	3.6	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current during Programming[2]	—	10	—	mA	
D136	IPEAK	Instantaneous Peak Current During Start-up	—	—	150	mA	
D137a	TPE	Page Erase Time	17.7	—	22.9	ms	TPE = 146893 FRC cycles, TA = +85°C (See **Note 3)**
D137b	TPE	Page Erase Time	17.5	—	23.1	ms	TPE = 146893 FRC cycles, TA = +125°C (See **Note 3)**
D138a	TWW	Word Write Cycle Time	41.7	—	53.8	µs	TWW = 346 FRC cycles, TA = +85°C (See **Note 3)**
D138b	TWW	Word Write Cycle Time	41.2	—	54.4	µs	TWW = 346 FRC cycles, TA = +125°C (See **Note 3)**

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: Parameter characterized but not tested in manufacturing.

3: Other conditions: FRC = 7.37 MHz, TUN<5:0> = `011111` (for Minimum), TUN<5:0> = `100000` (for Maximum). This parameter depends on the FRC accuracy (see Table 30-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see **Section 5.3 “Programming Operations”**.

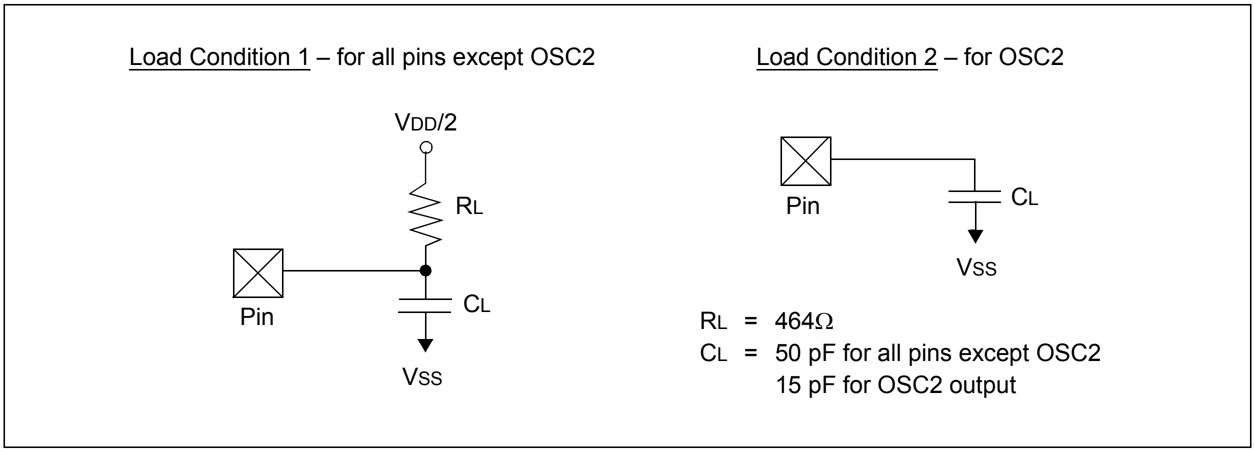
30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters.

TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V** **(unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Operating voltage V_{DD} range as described in **Section 30.1 "DC Characteristics"**.

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



R_L = 464Ω

C_L = 50 pF for all pins except OSC2
15 pF for OSC2 output

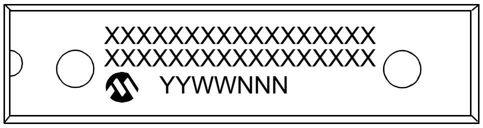
TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	C_{OSCO}	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	C_{IO}	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	C_B	SCLx, SDAx	—	—	400	pF	In I^2C™ mode

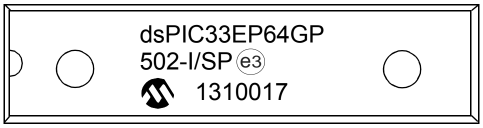
33.0 PACKAGING INFORMATION

33.1 Package Marking Information

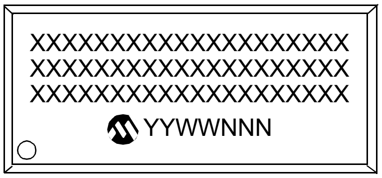
28-Lead SPDIP



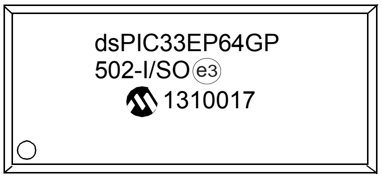
Example



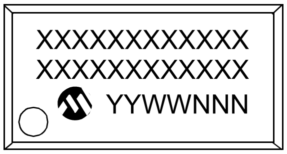
28-Lead SOIC (.300”)



Example

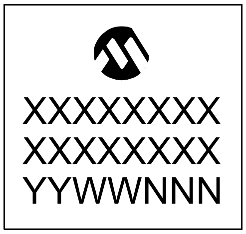


28-Lead SSOP



Example

28-Lead QFN-S (6x6x0.9 mm)



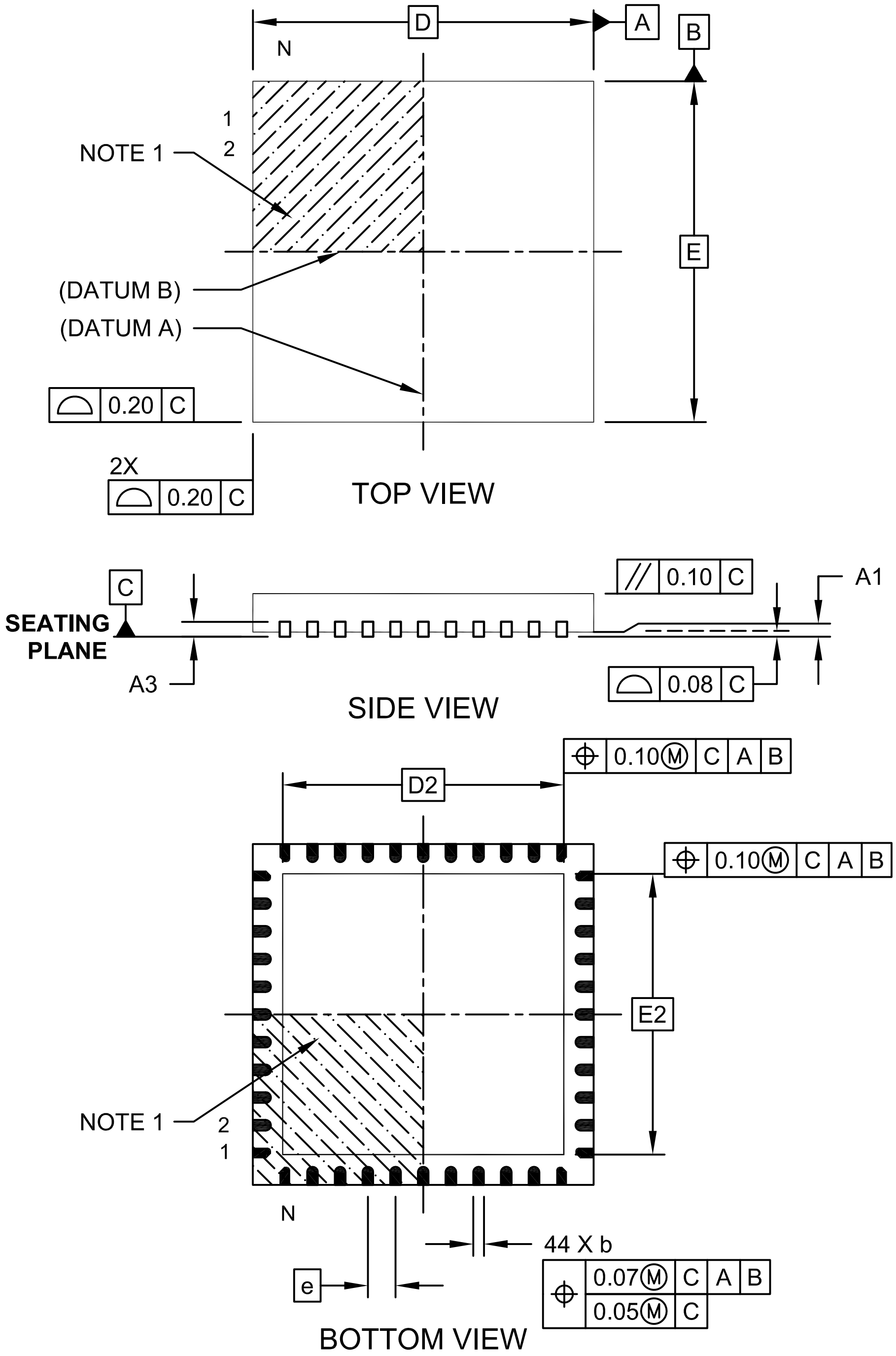
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

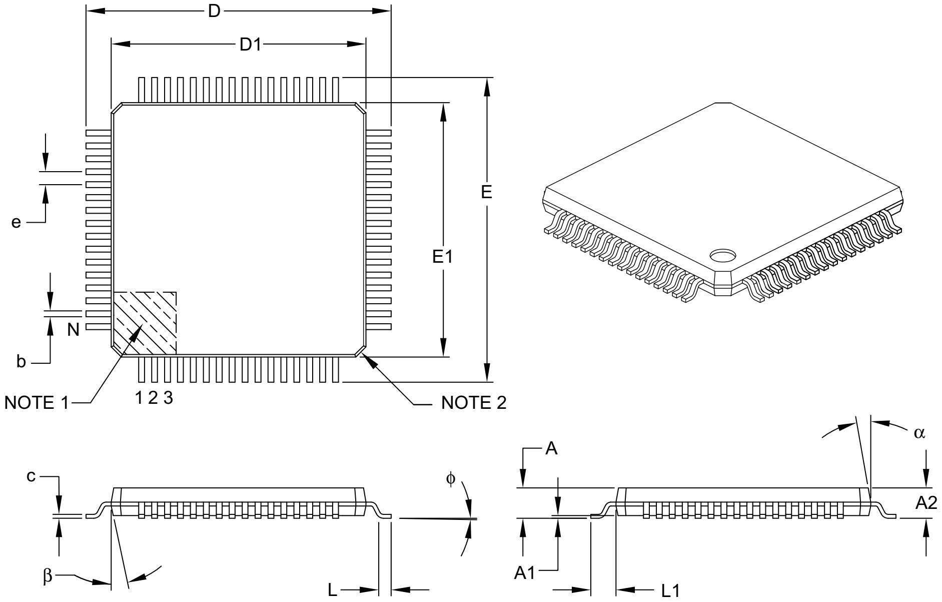
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-103C Sheet 1 of 2

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Leads	N	64		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

NOTES: