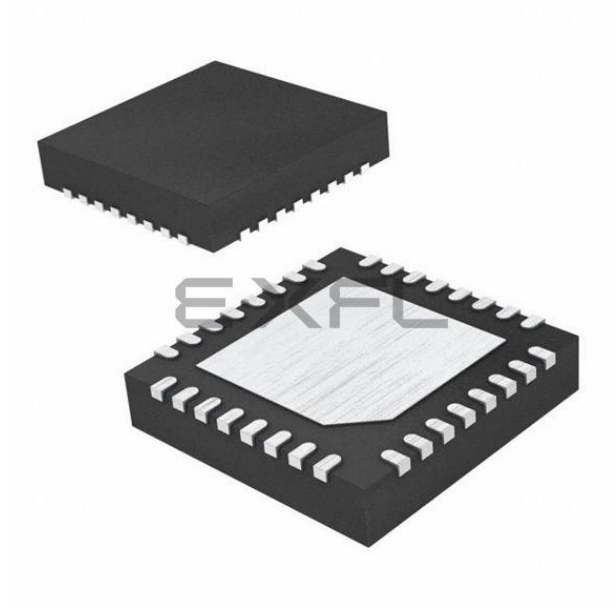
# Microchip Technology - DSPIC33EP128MC202-H/MM Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 150°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN-S (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc202-h-mm |

**TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES**

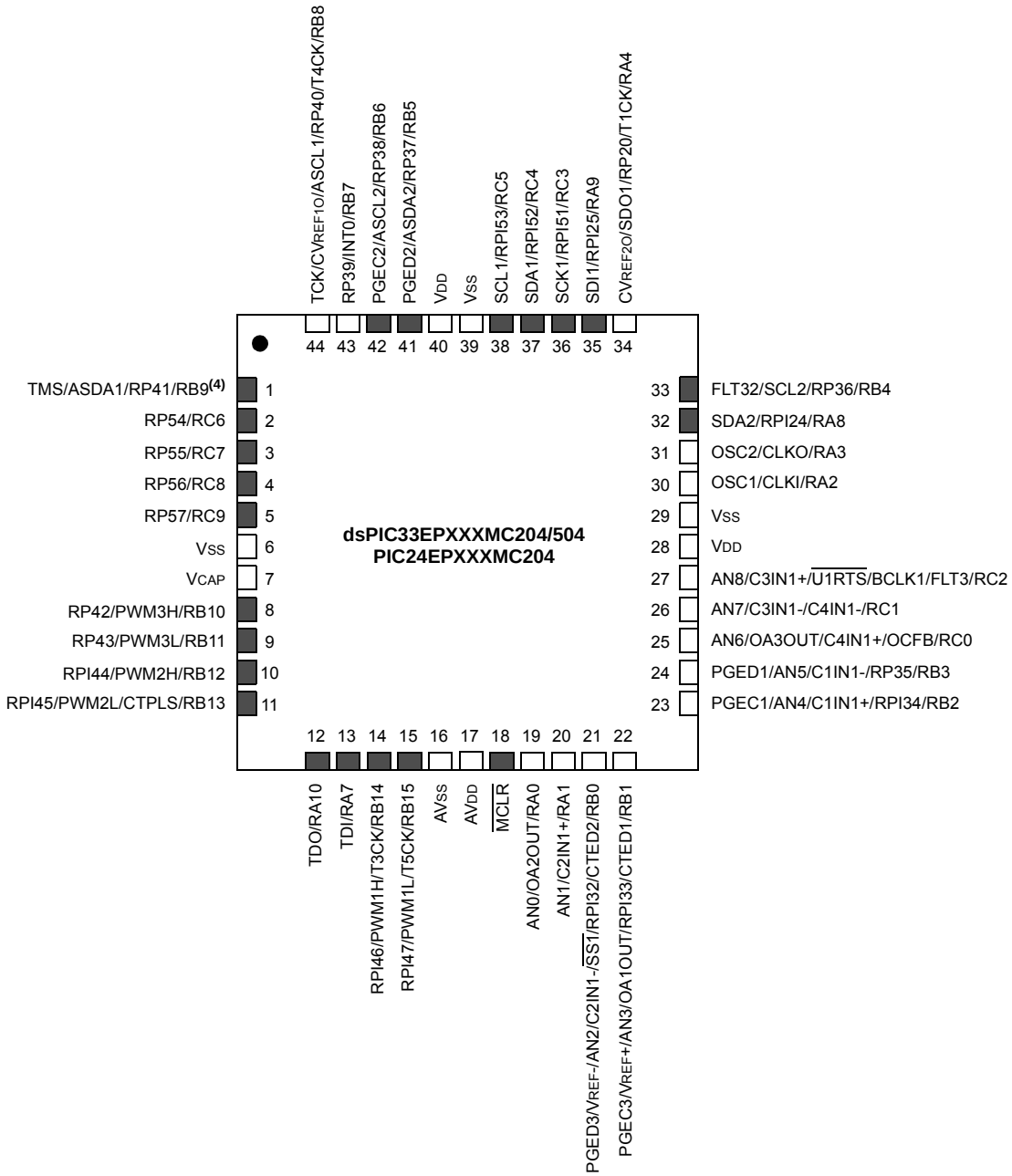
| Device | Page Erase Size (Instructions) | Program Flash Memory (Kbytes) | RAM (Kbytes) | Remappable Peripherals | | | | | | | | | $I^2C$™ | CRC Generator | 10-Bit/12-Bit ADC (Channels) | Op Amps/Comparators | CTMU | PTG | I/O Pins | Pins | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 16-Bit/32-Bit Timers | Input Capture | Output Compare | Motor Control PWM(4) (Channels) | Quadrature Encoder Interface | UART | SPI(2) | ECAN™ Technology | External Interrupts(3) | | | | | | | | | |
| PIC24EP32MC202 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 6 | 2/3(1) | Yes | Yes | 21 | 28 | SPDIP, SOIC, SSOP(5), QFN-S |
| PIC24EP64MC202 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| PIC24EP128MC202 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| PIC24EP256MC202 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| PIC24EP512MC202 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| PIC24EP32MC203 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 8 | 3/4 | Yes | Yes | 25 | 36 | VTLA |
| PIC24EP64MC203 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| PIC24EP32MC204 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 9 | 3/4 | Yes | Yes | 35 | 44/48 | VTLA(5), TQFP, QFN, UQFN |
| PIC24EP64MC204 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| PIC24EP128MC204 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| PIC24EP256MC204 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| PIC24EP512MC204 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| PIC24EP64MC206 | 1024 | 64 | 8 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 16 | 3/4 | Yes | Yes | 53 | 64 | TQFP, QFN |
| PIC24EP128MC206 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| PIC24EP256MC206 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| PIC24EP512MC206 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC202 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 6 | 2/3(1) | Yes | Yes | 21 | 28 | SPDIP, SOIC, SSOP(5), QFN-S |
| dsPIC33EP64MC202 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP128MC202 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC202 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC202 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC203 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 8 | 3/4 | Yes | Yes | 25 | 36 | VTLA |
| dsPIC33EP64MC203 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC204 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 9 | 3/4 | Yes | Yes | 35 | 44/48 | VTLA(5), TQFP, QFN, UQFN |
| dsPIC33EP64MC204 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP128MC204 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC204 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC204 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP64MC206 | 1024 | 64 | 8 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 16 | 3/4 | Yes | Yes | 53 | 64 | TQFP, QFN |
| dsPIC33EP128MC206 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC206 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC206 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC502 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | 1 | 3 | 2 | 1 | 6 | 2/3(1) | Yes | Yes | 21 | 28 | SPDIP, SOIC, SSOP(5), QFN-S |
| dsPIC33EP64MC502 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP128MC502 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC502 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC502 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC503 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | 1 | 3 | 2 | 1 | 8 | 3/4 | Yes | Yes | 25 | 36 | VTLA |
| dsPIC33EP64MC503 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |

**Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 "Op Amp/Comparator Module"** for details.
**2:** Only SPI2 is remappable.
**3:** INT0 is not remappable.
**4:** Only the PWM Faults are remappable.
**5:** The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

## Pin Diagrams (Continued)

**44-Pin QFN(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

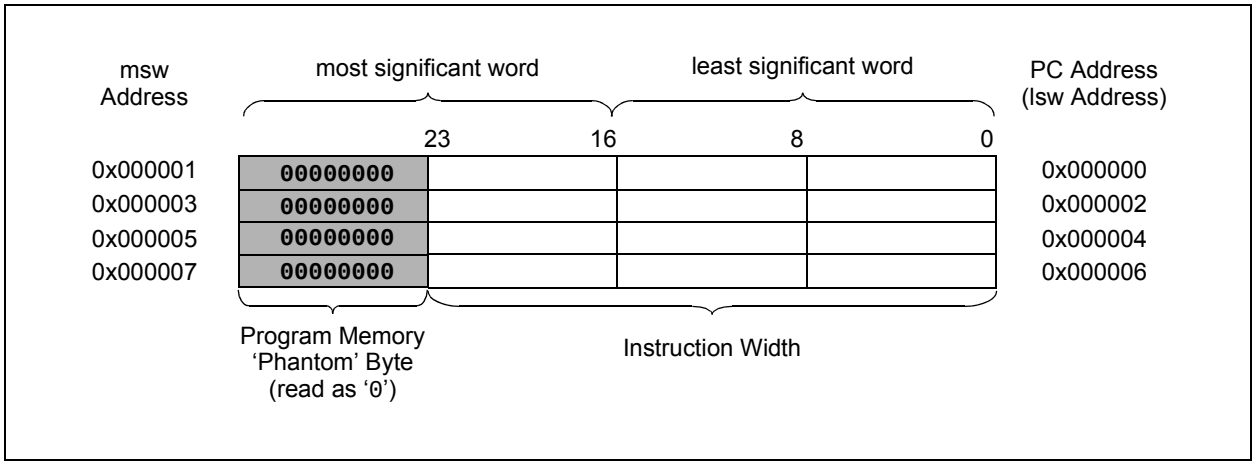
Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1 "Interrupt Vector Table"**.

**FIGURE 4-6: PROGRAM MEMORY ORGANIZATION**



### 4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

**Note 1:** DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.

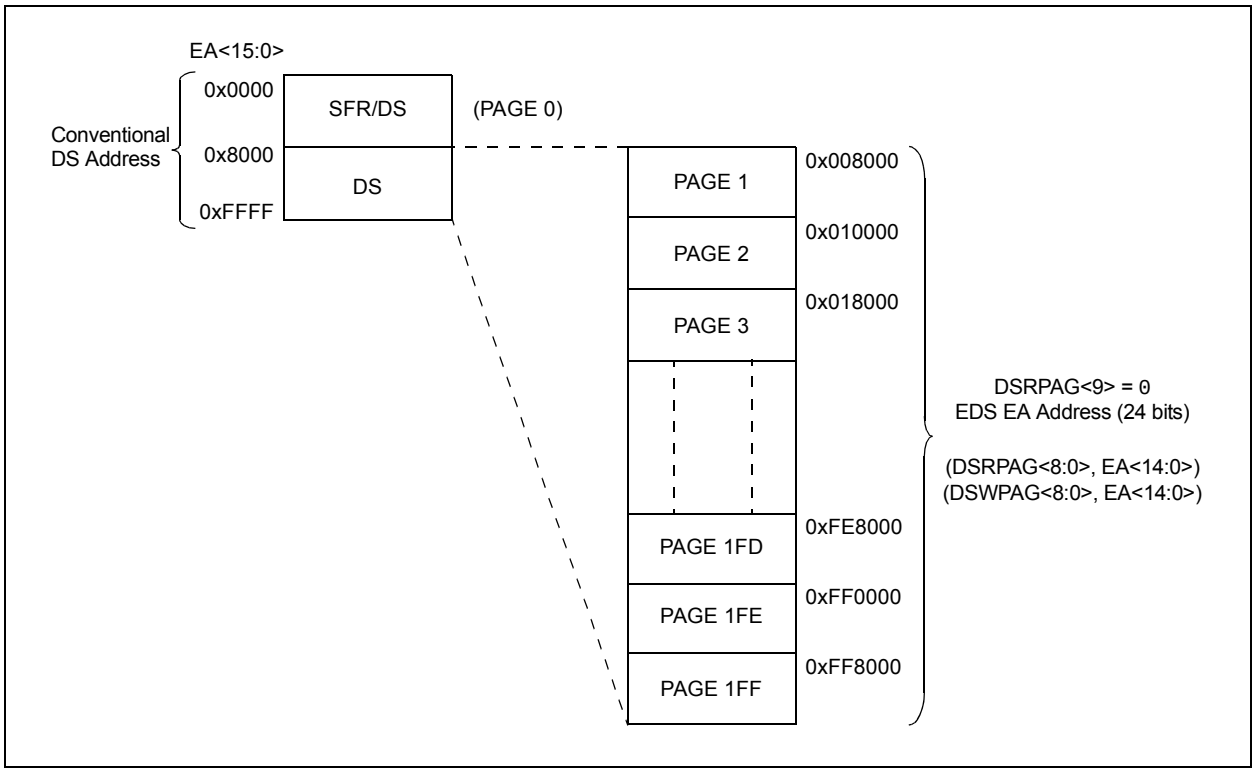
**2:** Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-17.

For more information on the PSV page access using Data Space Page registers, refer to the **"Program Space Visibility from Data Space"** section in **"Program Memory"** (DS70613) of the *"dsPIC33/PIC24 Family Reference Manual"*.

**FIGURE 4-17: EDS MEMORY MAP**



**REGISTER 5-2: NVMADRH: NONVOLATILE MEMORY ADDRESS REGISTER HIGH**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMADR<23:16>:** Nonvolatile Memory Write Address High bits

Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-3: NVMADRL: NONVOLATILE MEMORY ADDRESS REGISTER LOW**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Write Address Low bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
|---|---|---|---|---|---|---|---|
| NVMKEY<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

**NOTES:**

**REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DMA0MD(1)<br>DMA1MD(1)<br>DMA2MD(1)<br>DMA3MD(1) | PTGMD | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **DMA0MD:** DMA0 Module Disable bit(1)
1 = DMA0 module is disabled
0 = DMA0 module is enabled

**DMA1MD:** DMA1 Module Disable bit(1)
1 = DMA1 module is disabled
0 = DMA1 module is enabled

**DMA2MD:** DMA2 Module Disable bit(1)
1 = DMA2 module is disabled
0 = DMA2 module is enabled

**DMA3MD:** DMA3 Module Disable bit(1)
1 = DMA3 module is disabled
0 = DMA3 module is enabled

bit 3 **PTGMD:** PTG Module Disable bit
1 = PTG module is disabled
0 = PTG module is enabled

bit 2-0 **Unimplemented:** Read as '0'

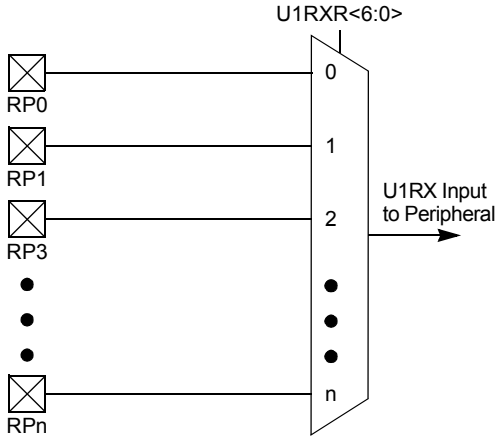
**Note 1:** This single bit enables and disables all four DMA channels.

### 11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

**FIGURE 11-2: REMAPPABLE INPUT FOR U1RX**




**Note:** For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

#### 11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 "Op Amp/Comparator Module"**), and the PTG module (see **Section 24.0 "Peripheral Trigger Generator (PTG) Module"**).

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"**.

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

**EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE**

```
RPINR15 = 0x2500;      /* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7  = 0x009;       /* Connect the IC1 input to the digital filter on the FHOME1 input */

QEI1IOC = 0x4000;      /* Enable the QEI digital filter */
QEI1CON = 0x8000;      /* Enable the QEI module */
```

**TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES**

| Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment | Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment |
|---|---|---|---|---|---|
| 000 0000 | I | Vss | 010 1101 | I | RPI45 |
| 000 0001 | I | C1OUT(1) | 010 1110 | I | RPI46 |
| 000 0010 | I | C2OUT(1) | 010 1111 | I | RPI47 |
| 000 0011 | I | C3OUT(1) | 011 0000 | — | — |
| 000 0100 | I | C4OUT(1) | 011 0001 | — | — |
| 000 0101 | — | — | 011 0010 | — | — |
| 000 0110 | I | PTGO30(1) | 011 0011 | I | RPI51 |
| 000 0111 | I | PTGO31(1) | 011 0100 | I | RPI52 |
| 000 1000 | I | FINDX1(1,2) | 011 0101 | I | RPI53 |
| 000 1001 | I | FHOME1(1,2) | 011 0110 | I/O | RP54 |
| 000 1010 | — | — | 011 0111 | I/O | RP55 |
| 000 1011 | — | — | 011 1000 | I/O | RP56 |
| 000 1100 | — | — | 011 1001 | I/O | RP57 |
| 000 1101 | — | — | 011 1010 | I | RPI58 |
| 000 1110 | — | — | 011 1011 | — | — |
| 000 1111 | — | — | 011 1100 | — | — |
| 001 0000 | — | — | 011 1101 | — | — |
| 001 0001 | — | — | 011 1110 | — | — |
| 001 0010 | — | — | 011 1111 | — | — |
| 001 0011 | — | — | 100 0000 | — | — |
| 001 0100 | I/O | RP20 | 100 0001 | — | — |
| 001 0101 | — | — | 100 0010 | — | — |
| 001 0110 | — | — | 100 0011 | — | — |
| 001 0111 | — | — | 100 0100 | — | — |
| 001 1000 | I | RPI24 | 100 0101 | — | — |
| 001 1001 | I | RPI25 | 100 0110 | — | — |
| 001 1010 | — | — | 100 0111 | — | — |
| 001 1011 | I | RPI27 | 100 1000 | — | — |
| 001 1100 | I | RPI28 | 100 1001 | — | — |
| 001 1101 | — | — | 100 1010 | — | — |
| 001 1110 | — | — | 100 1011 | — | — |
| 001 1111 | — | — | 100 1100 | — | — |
| 010 0000 | I | RPI32 | 100 1101 | — | — |
| 010 0001 | I | RPI33 | 100 1110 | — | — |
| 010 0010 | I | RPI34 | 100 1111 | — | — |
| 010 0011 | I/O | RP35 | 101 0000 | — | — |
| 010 0100 | I/O | RP36 | 101 0001 | — | — |
| 010 0101 | I/O | RP37 | 101 0010 | — | — |
| 010 0110 | I/O | RP38 | 101 0011 | — | — |
| 010 0111 | I/O | RP39 | 101 0100 | — | — |

**Legend:** Shaded rows indicate PPS Input register values that are unimplemented.

**Note 1:** See **Section 11.4.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

**2:** These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

**REGISTER 11-17: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP3R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP2R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP3R<6:0>:** Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP2R<6:0>:** Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QCAPEN | FLTREN | QFDIV2 | QFDIV1 | QFDIV0 | OUTFNC1 | OUTFNC0 | SWPAB |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| HOMPOL | IDXPOL | QEBPOL | QEAPOL | HOME | INDEX | QEB | QEA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **QCAPEN:** QEI Position Counter Input Capture Enable bit
1 = Index match event triggers a position capture event
0 = Index match event does not trigger a position capture event

bit 14 **FLTREN:** QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit
1 = Input pin digital filter is enabled
0 = Input pin digital filter is disabled (bypassed)

bit 13-11 **QFDIV<2:0>:** QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits
111 = 1:128 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 10-9 **OUTFNC<1:0>:** QEI Module Output Function Mode Select bits
11 = The CTNCMPx pin goes high when QEI1LEC ≥ POS1CNT ≥ QEI1GEC
10 = The CTNCMPx pin goes high when POS1CNT ≤ QEI1LEC
01 = The CTNCMPx pin goes high when POS1CNT ≥ QEI1GEC
00 = Output is disabled

bit 8 **SWPAB:** Swap QEA and QEB Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped

bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

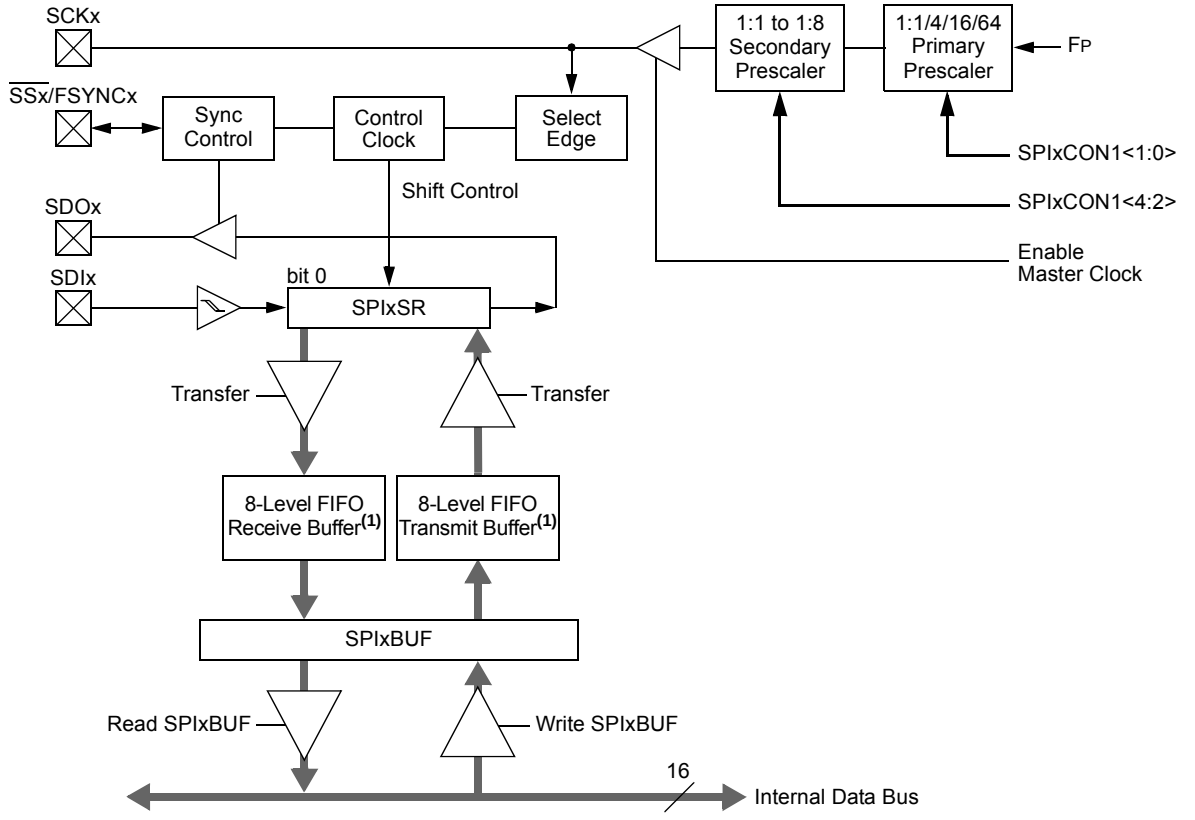
bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control
1 = Pin is at logic '1'
0 = Pin is at logic '0'

**FIGURE 18-1: SPIx MODULE BLOCK DIAGRAM**




**Note 1:** In Standard mode, the FIFO is only one level deep.

**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0, HC | R/W-0 | R-0 | R-1 |
|---|---|---|---|---|---|---|---|
| UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN(1) | UTXBF | TRMT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/C-0 | R-0 |
|---|---|---|---|---|---|---|---|
| URXISEL1 | URXISEL0 | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | C = Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA encoded, UxTX Idle state is '1'
- 0 = IrDA encoded, UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

**Note 1:** Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

**TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)**

| Bit Field | Description |
|---|---|
| WDTPRE | Watchdog Timer Prescaler bit<br>1 = 1:128<br>0 = 1:32 |
| WDTPOST<3:0> | Watchdog Timer Postscaler bits<br>1111 = 1:32,768<br>1110 = 1:16,384<br>•<br>•<br>•<br>0001 = 1:2<br>0000 = 1:1 |
| WDTWIN<1:0> | Watchdog Window Select bits<br>11 = WDT window is 25% of WDT period<br>10 = WDT window is 37.5% of WDT period<br>01 = WDT window is 50% of WDT period<br>00 = WDT window is 75% of WDT period |
| ALTI2C1 | Alternate I2C1 pin<br>1 = I2C1 is mapped to the SDA1/SCL1 pins<br>0 = I2C1 is mapped to the ASDA1/ASCL1 pins |
| ALTI2C2 | Alternate I2C2 pin<br>1 = I2C2 is mapped to the SDA2/SCL2 pins<br>0 = I2C2 is mapped to the ASDA2/ASCL2 pins |
| JTAGEN(2) | JTAG Enable bit<br>1 = JTAG is enabled<br>0 = JTAG is disabled |
| ICS<1:0> | ICD Communication Channel Select bits<br>11 = Communicate on PGEC1 and PGED1<br>10 = Communicate on PGEC2 and PGED2<br>01 = Communicate on PGEC3 and PGED3<br>00 = Reserved, do not use |

**Note 1:** This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

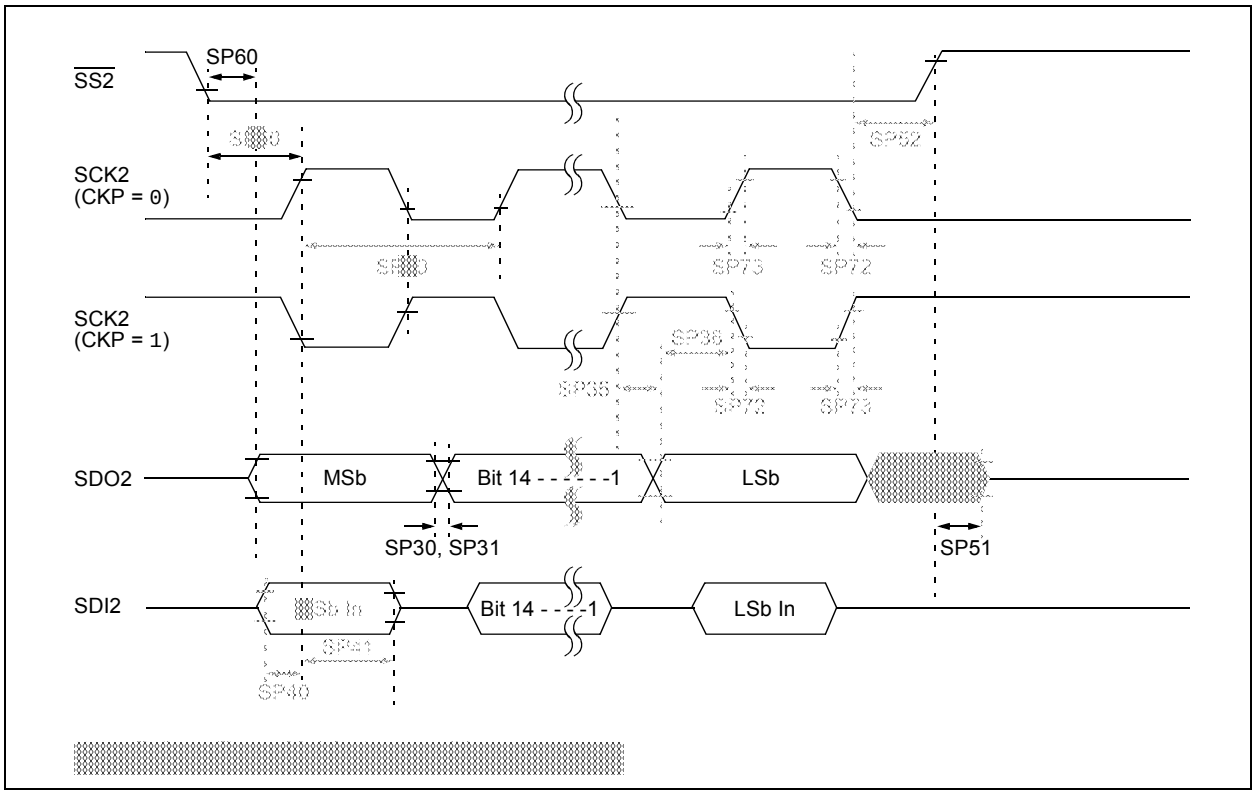
**TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current (IIDLE)(1)** | | | | | | |
| DC40d | 3 | 8 | mA | -40°C | 3.3V | 10 MIPS |
| DC40a | 3 | 8 | mA | +25°C | | |
| DC40b | 3 | 8 | mA | +85°C | | |
| DC40c | 3 | 8 | mA | +125°C | | |
| DC42d | 6 | 12 | mA | -40°C | 3.3V | 20 MIPS |
| DC42a | 6 | 12 | mA | +25°C | | |
| DC42b | 6 | 12 | mA | +85°C | | |
| DC42c | 6 | 12 | mA | +125°C | | |
| DC44d | 11 | 18 | mA | -40°C | 3.3V | 40 MIPS |
| DC44a | 11 | 18 | mA | +25°C | | |
| DC44b | 11 | 18 | mA | +85°C | | |
| DC44c | 11 | 18 | mA | +125°C | | |
| DC45d | 17 | 27 | mA | -40°C | 3.3V | 60 MIPS |
| DC45a | 17 | 27 | mA | +25°C | | |
| DC45b | 17 | 27 | mA | +85°C | | |
| DC45c | 17 | 27 | mA | +125°C | | |
| DC46d | 20 | 35 | mA | -40°C | 3.3V | 70 MIPS |
| DC46a | 20 | 35 | mA | +25°C | | |
| DC46b | 20 | 35 | mA | +85°C | | |

**Note 1:** Base Idle current (IIDLE) is measured as follows:

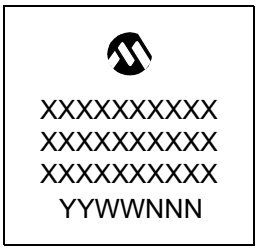
- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

**FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**



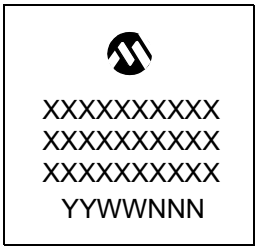
## 33.1 Package Marking Information (Continued)

36-Lead VTLA (TLA)



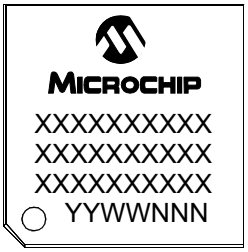

Example


44-Lead VTLA (TLA)



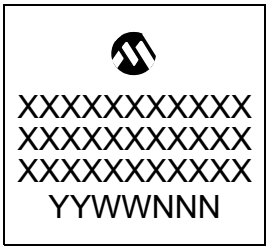

Example


44-Lead TQFP




Example

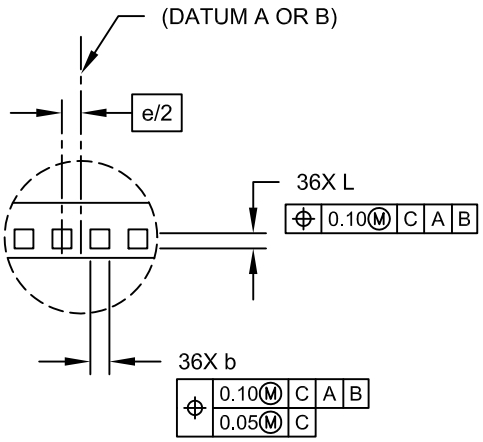

44-Lead QFN (8x8x0.9 mm)



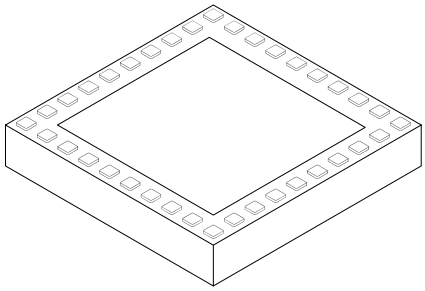

Example

## 36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL A**



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension | Limits | MIN | NOM | MAX |
| Number of Pins | N | | 36 | |
| Number of Pins per Side | ND | | 10 | |
| Number of Pins per Side | NE | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.025 | - | 0.075 |
| Overall Width | E | | 5.00 BSC | |
| Exposed Pad Width | E2 | 3.60 | 3.75 | 3.90 |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 3.60 | 3.75 | 3.90 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.25 | 0.30 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2

**TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** | Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2).<br>Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively). |
| **Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"** | Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1). |
| **Section 22.0 "Charge Time Measurement Unit (CTMU)"** | Updated the IRNG<1:0> bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3). |
| **Section 25.0 "Op amp/ Comparator Module"** | Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1).<br>Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3).<br>Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4).<br>Added **Section 25.1 "Op amp Application Considerations"**.<br>Added Note 2 to the Comparator Control Register (see Register 25-2).<br>Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5). |
| **Section 27.0 "Special Features"** | Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1).<br>Added **Section 27.2 "User ID Words"**. |
| **Section 30.0 "Electrical Characteristics"** | Updated the following Absolute Maximum Ratings:<br>• Maximum current out of $V_{SS}$ pin<br>• Maximum current into $V_{DD}$ pin<br>Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1).<br>Updated all Idle Current ($I_{IDLE}$) Typical and Maximum DC Characteristics values (see Table 30-7).<br>Updated all Doze Current ($I_{DOZE}$) Typical and Maximum DC Characteristics values (see Table 30-9).<br>Added Note 2, removed Parameter CM24, updated the Typical values Parameters CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).<br>Updated Note 2 and the Typical value for Parameter VR310 in the Op amp/ Comparator Reference Voltage Settling Time Specifications (see Table 30-15).<br>Added Note 1, removed Parameter VRD312, and added Parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).<br>Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22).<br>Updated the Minimum, Typical, and Maximum values for Parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24).<br>The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35) |

## Revision D (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog"** | Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2. |
| **Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"** | Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1). |
| **Section 30.0 "Electrical Characteristics"** | Updated the $V_{BOR}$ specifications and/or its related note in the following electrical characteristics tables:<br>• Table 30-1<br>• Table 30-4<br>• Table 30-12<br>• Table 30-14<br>• Table 30-15<br>• Table 30-16<br>• Table 30-56<br>• Table 30-57<br>• Table 30-58<br>• Table 30-59<br>• Table 30-60 |