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What is "Embedded - Microcontrollers"?

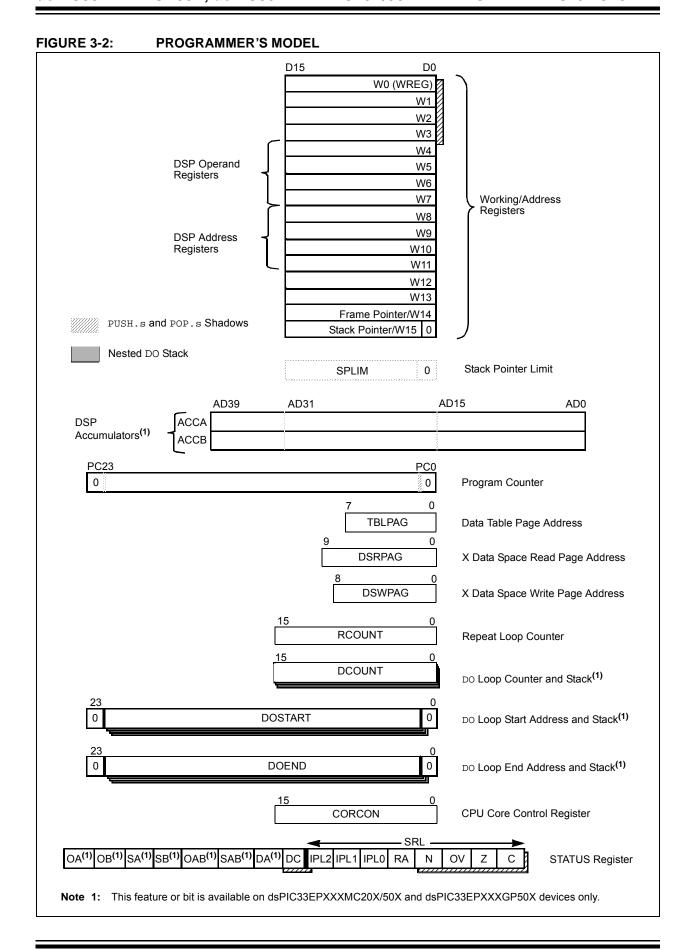
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc204-h-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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#### TABLE 4-12: PWM REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	PTEN - PTSIDL SESTAT SEIEN EIPU SYNCPOL SYNCOEN SYNCEN SYNCSRC<2:0> SEVTPS<3:0>									0000						
PTCON2	0C02	_	PCLKDIV<2:0>								0000							
PTPER	0C04		PTPER<15:0>								00F8							
SEVTCMP	0C06								SEVTCMP<1	5:0>								0000
MDC	0C0A								MDC<15:0	)>								0000
CHOP	0C1A	CHPCLKEN	PCLKEN — — — — CHOPCLK<9:0>								0000							
PWMKEY	0C1E	PWMKEY<15:0>							0000									

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY

													. —					
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<	:1:0>	DTCP	_	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD	<1:0>	OVRENH	OVRENL	OVRDA	T<1:0>	FLTDA	AT<1:0>	CLDA	T<1:0>	SWAP	OSYNC	C000
FCLCON1	0C24	-		(	CLSRC<4:	0>		CLPOL	CLMOD		FL	TSRC<4:0	)>		FLTPOL	FLTMO	D<1:0>	0000
PDC1	0C26				PDC1<15:0>						FFF8							
PHASE1	0C28				PHASE1<15:0>									0000				
DTR1	0C2A	-	_							DTR1<13:	0>							0000
ALTDTR1	0C2C	-	_						Д	LTDTR1<1	3:0>							0000
TRIG1	0C32								TRGCMP<1	5:0>								0000
TRGCON1	0C34		TRGDI	V<3:0>		_	_	_	_	_	_			TRG	STRT<5:0	>		0000
LEBCON1	0C3A	PHR	PHF	PLR	PLR PLF FLTLEBEN CLLEBEN — — — BCH BCL BPHH BPHL BPLH BPLL						BPLL	0000						
LEBDLY1	0C3C	_	_	_	LEB<11:0> 0							0000						
AUXCON1	0C3E	_	_	_	- — BLANKSEL<3:0> — — CHOPSEL<3:0> CHOPHEN CHOPLE						CHOPLEN	0000						

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### REGISTER 5-2: NVMADRH: NONVOLATILE MEMORY ADDRESS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
			NVMADF	R<23:16>					
bit 7									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 NVMADR<23:16>: Nonvolatile Memory Write Address High bits

Selects the upper 8 bits of the location to program or erase in program Flash memory. This register

may be read or written by the user application.

#### REGISTER 5-3: NVMADRL: NONVOLATILE MEMORY ADDRESS REGISTER LOW

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMAD	R<15:8>			
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMAD	)R<7:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Write Address Low bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register

may be read or written by the user application.

## REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0		
			NVMKE	Y<7:0>					
bit 7									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

#### 6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:

In the event you are not able to access the product page using the link above, enter this URL in your browser:

http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

#### 6.1.1 KEY RESOURCES

- "Reset" (DS70602) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- · Development Tools

#### 11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

#### 11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

#### 11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include  $I^2C^{\,\text{TM}}$  and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

# 11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheralselectable pin is handled in two different ways, depending on whether an input or output is being mapped.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pi Select Input Register Valu	Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss	010 1101	ı	RPI45
000 0001	1	C1OUT <sup>(1)</sup>	010 1110	I	RPI46
000 0010	1	C2OUT <sup>(1)</sup>	010 1111	I	RPI47
000 0011	1	C3OUT <sup>(1)</sup>	011 0000	_	<del>_</del>
000 0100	I	C4OUT <sup>(1)</sup>	011 0001	_	<del>_</del>
000 0101	_	_	011 0010	_	<del>-</del>
000 0110	I	PTGO30 <sup>(1)</sup>	011 0011	I	RPI51
000 0111	I	PTGO31 <sup>(1)</sup>	011 0100	I	RPI52
000 1000	I	FINDX1 <sup>(1,2)</sup>	011 0101	I	RPI53
000 1001	I	FHOME1 <sup>(1,2)</sup>	011 0110	I/O	RP54
000 1010	_	_	011 0111	I/O	RP55
000 1011	_		011 1000	I/O	RP56
000 1100	_		011 1001	I/O	RP57
000 1101	_	_	011 1010	I	RPI58
000 1110	_	_	011 1011	_	_
000 1111	_		011 1100	_	_
001 0000	_	_	011 1101	_	_
001 0001	_		011 1110	_	_
001 0010	_	_	011 1111	_	_
001 0011	_	_	100 0000	_	_
001 0100	I/O	RP20	100 0001	_	_
001 0101	_	_	100 0010	_	_
001 0110	_	_	100 0011	_	_
001 0111	_	_	100 0100	_	
001 1000	1	RPI24	100 0101	_	_
001 1001	1	RPI25	100 0110	_	_
001 1010	_	_	100 0111	_	
001 1011	I	RPI27	100 1000	_	<u> </u>
001 1100	I	RPI28	100 1001	_	_
001 1101	_	_	100 1010	_	_
001 1110	_	_	100 1011	_	<u> </u>
001 1111	_	_	100 1100	_	_
010 0000	I	RPI32	100 1101	_	_
010 0001	I	RPI33	100 1110	_	<u> </u>
010 0010	I	RPI34	100 1111	_	_
010 0011	I/O	RP35	101 0000	_	_
010 0100	I/O	RP36	101 0001	_	_
010 0101	I/O	RP37	101 0010	_	_
010 0110	I/O	RP38	101 0011	_	_
010 0111	I/O	RP39	101 0100		_

**Legend:** Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See Section 11.4.4.1 "Virtual Connections" for more information on selecting this pin assignment.

**2:** These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

#### REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I<sup>2</sup>C<sup>™</sup> master, applicable to master transmit operation)
  - 1 = NACK received from slave
  - 0 = ACK received from slave

Hardware is set or clear at the end of slave Acknowledge.

- bit 14 TRSTAT: Transmit Status bit (when operating as I<sup>2</sup>C master, applicable to master transmit operation)
  - 1 = Master transmit is in progress (8 bits + ACK)
  - 0 = Master transmit is not in progress

Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.

- bit 13-11 Unimplemented: Read as '0'
- bit 10 BCL: Master Bus Collision Detect bit
  - 1 = A bus collision has been detected during a master operation
  - 0 = No bus collision detected

Hardware is set at detection of a bus collision.

- bit 9 GCSTAT: General Call Status bit
  - 1 = General call address was received
  - 0 = General call address was not received

Hardware is set when address matches general call address. Hardware is clear at Stop detection.

- bit 8 ADD10: 10-Bit Address Status bit
  - 1 = 10-bit address was matched
  - 0 = 10-bit address was not matched

Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.

- bit 7 IWCOL: I2Cx Write Collision Detect bit
  - 1 = An attempt to write to the I2CxTRN register failed because the I<sup>2</sup>C module is busy
  - 0 = No collision

Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).

- bit 6 I2COV: I2Cx Receive Overflow Flag bit
  - 1 = A byte was received while the I2CxRCV register was still holding the previous byte
  - 0 = No overflow

Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

- bit 5 **D\_A:** Data/Address bit (when operating as I<sup>2</sup>C slave)
  - 1 = Indicates that the last byte received was data
  - 0 = Indicates that the last byte received was a device address

Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

- bit 4 **P:** Stop bit
  - 1 = Indicates that a Stop bit has been detected last
  - 0 = Stop bit was not detected last

Hardware is set or clear when a Start, Repeated Start or Stop is detected.

#### REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3 S: Start bit

1 = Indicates that a Start (or Repeated Start) bit has been detected last

0 = Start bit was not detected last

Hardware is set or clear when a Start, Repeated Start or Stop is detected.

bit 2 **R\_W:** Read/Write Information bit (when operating as I<sup>2</sup>C slave)

1 = Read – Indicates data transfer is output from the slave

0 = Write - Indicates data transfer is input to the slave

Hardware is set or clear after reception of an I<sup>2</sup>C device address byte.

bit 1 RBF: Receive Buffer Full Status bit

1 = Receive is complete, I2CxRCV is full

0 = Receive is not complete, I2CxRCV is empty

Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads

I2CxRCV.

bit 0 TBF: Transmit Buffer Full Status bit

1 = Transmit in progress, I2CxTRN is full

0 = Transmit is complete, I2CxTRN is empty

Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

#### REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
_	_	_	_	_	_	AMSK9	AMSK8
bit 15							bit 8

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| AMSK7 | AMSK6 | AMSK5 | AMSK4 | AMSK3 | AMSK2 | AMSK1 | AMSK0 |
| bit 7 |       |       |       |       |       |       | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

#### REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F15BP	<3:0>		F14BP<3:0>				
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F13BP	<3:0>		F12BP<3:0>				
bit 7							bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 F15BP<3:0>: RX Buffer Mask for Filter 15 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bits<15:12>)

bit 7-4 **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bits<15:12>)

bit 3-0 **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bits<15:12>)

### 23.4 ADC Control Registers

#### REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	_	ADSIDL	ADDMABM	_	AD12B	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE <sup>(3)</sup>
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 ADON: ADC1 Operating Mode bit

1 = ADC module is operating

0 = ADC is off

bit 14 **Unimplemented:** Read as '0'

bit 13 ADSIDL: ADC1 Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12 ADDMABM: DMA Buffer Build Mode bit

1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer

0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.

bit 11 **Unimplemented:** Read as '0'

bit 10 AD12B: ADC1 10-Bit or 12-Bit Operation Mode bit

1 = 12-bit, 1-channel ADC operation

0 = 10-bit, 4-channel ADC operation

bit 9-8 **FORM<1:0>:** Data Output Format bits

For 10-Bit Operation:

11 = Signed fractional (Dout = sddd dddd dd00 0000, where s = .NOT.d<9>)

10 = Fractional (Dout = dddd dddd dd00 0000)

01 = Signed integer (Dout = ssss sssd dddd dddd, where s = .NOT.d<9>)

00 = Integer (Dout = 0000 00dd dddd dddd)

For 12-Bit Operation:

11 = Signed fractional (Dout = sddd dddd dddd 0000, where s = .NOT.d<11>)

10 = Fractional (Dout = dddd dddd dddd 0000)

01 = Signed integer (Dout = ssss sddd dddd, where s = .NOT.d<11>)

00 = Integer (Dout = 0000 dddd dddd dddd)

Note 1: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

3: Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

# REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGADJ<15:8>								
bit 15								

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGADJ<7:0>								
bit 7							bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits

This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

# REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGL0<15:8>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PTGL0<7:0>									
bit 7							bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGL0<15:0>:** PTG Literal 0 Register bits

This register holds the 16-bit value to be written to the AD1CHS0 register with the PTGCTRL Step command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

TABLE 24-2: PTG OUTPUT DESCRIPTIONS

PTG Output Number	PTG Output Description
PTGO0	Trigger/Synchronization Source for OC1
PTGO1	Trigger/Synchronization Source for OC2
PTGO2	Trigger/Synchronization Source for OC3
PTGO3	Trigger/Synchronization Source for OC4
PTGO4	Clock Source for OC1
PTGO5	Clock Source for OC2
PTGO6	Clock Source for OC3
PTGO7	Clock Source for OC4
PTGO8	Trigger/Synchronization Source for IC1
PTGO9	Trigger/Synchronization Source for IC2
PTGO10	Trigger/Synchronization Source for IC3
PTGO11	Trigger/Synchronization Source for IC4
PTGO12	Sample Trigger for ADC
PTGO13	Sample Trigger for ADC
PTGO14	Sample Trigger for ADC
PTGO15	Sample Trigger for ADC
PTGO16	PWM Time Base Synchronous Source for PWM <sup>(1)</sup>
PTGO17	PWM Time Base Synchronous Source for PWM <sup>(1)</sup>
PTGO18	Mask Input Select for Op Amp/Comparator
PTGO19	Mask Input Select for Op Amp/Comparator
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	Reserved
PTGO27	Reserved
PTGO28	Reserved
PTGO29	Reserved
PTGO30	PTG Output to PPS Input Selection
PTGO31	PTG Output to PPS Input Selection

Note 1: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

dsPIC33EPXXXGP5	0X, dsPIC33EPXXX	(MC20X/50X ANI	O PIC24EPXXX(	GP/MC20X
NOTES:				

FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

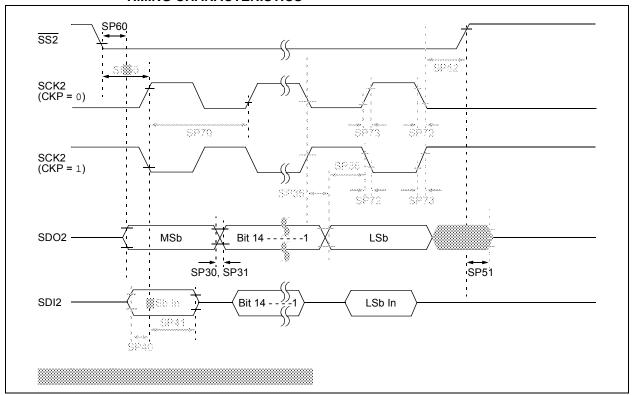


TABLE 30-39: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for Extended					
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	_	_	15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	_	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	_	_	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	_	_	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	_	_	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	_	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	SS2 ↓ to SCK2 ↑ or SCK2 ↓ Input	120	_	_	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

- **2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.
- 4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-59: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) <sup>(1)</sup> Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{Ta} \le +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic	Min.	Min. Typ. Max. Units Condition			Conditions
		ADC A	ccuracy (	10-Bit N	lode)		
AD20b	Nr	Resolution	10	Data B	its	bits	
AD21b	INL	Integral Nonlinearity	-0.625	_	0.625	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1.5		1.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD22b	DNL	Differential Nonlinearity	-0.25	-	0.25	LSb	$-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ (Note 2)
			-0.25	-	0.25	LSb	$+85^{\circ}C < TA \le +125^{\circ}C$ (Note 2)
AD23b	GERR	Gain Error	-2.5	_	2.5	LSb	$-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ (Note 2)
			-2.5	_	2.5	LSb	$+85^{\circ}C < TA \le +125^{\circ}C$ (Note 2)
AD24b	Eoff	Offset Error	-1.25	_	1.25	LSb	$-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ (Note 2)
			-1.25	_	1.25	LSb	$+85^{\circ}C < TA \le +125^{\circ}C$ (Note 2)
AD25b	_	Monotonicity	_	_			Guaranteed
		Dynamic P	erforman	ce (10-E	Bit Mode)		
AD30b	THD	Total Harmonic Distortion <sup>(3)</sup>	_	64	_	dB	
AD31b	SINAD	Signal to Noise and Distortion <sup>(3)</sup>	_	57	_	dB	
AD32b	SFDR	Spurious Free Dynamic Range <sup>(3)</sup>	_	72	_	dB	
AD33b	FNYQ	Input Signal Bandwidth <sup>(3)</sup>	_	550		kHz	
AD34b	ENOB	Effective Number of Bits <sup>(3)</sup>	_	9.4	_	bits	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.
- 3: Parameters are characterized but not tested in manufacturing.

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