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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc204-i-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)

(suc	~	s)	-			Rer	nappa	ble P	eriphe	erals								1			
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbyte	RAM (Kbytes)	16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM <sup>(4)</sup> (Channels)	Quadrature Encoder Interface	UART	SPI <sup>(2)</sup>	ECAN™ Technology	External Interrupts <sup>(3)</sup>	I <sup>2</sup> C <sup>TM</sup>	<b>CRC Generator</b>	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
dsPIC33EP32MC504	512	32	4																		
dsPIC33EP64MC504	1024	64	8																		VTLA <sup>(5)</sup> ,
dsPIC33EP128MC504	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/ 48	TQFP, OEN
dsPIC33EP256MC504	1024	256	32																	40	UQFN
dsPIC33EP512MC504	1024	512	48																		
dsPIC33EP64MC506	1024	64	8																		
dsPIC33EP128MC506	1024	128	16	5	4	4	6	1	2	2	1	2	2	1	16	2/4	Vaa	Voo	52	64	TQFP,
dsPIC33EP256MC506	1024	256	32	э	4	4	0	1	2	2	1	3	2		10	3/4	res	res	53	04	QFN
dsPIC33EP512MC506	1024	512	48																		

 Note 1:
 On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op Amp/Comparator Module" for details.

 2:
 Only SPI2 is remappable.

3: INT0 is not remappable.

4: Only the PWM Faults are remappable.

5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

### **Pin Diagrams**



### **Pin Diagrams (Continued)**



### **Pin Diagrams (Continued)**



# Pin Diagrams (Continued)



# 1.0 DEVICE OVERVIEW

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com)
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

#### FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM



# TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL		0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	_		_	_	_	_	_	_	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	_	_	_	_		_	_	_	_	DAE	DOOVR	_	_	_	_	0000
INTCON4	08C6					_	_			_				_	—		SGHT	0000
INTTREG	08C8						ILR<	3:0>		VECNUM<7:0> 00						0000		

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30			_	_	—			TRISD8	_	TRISD6	TRISD5	_					0160
PORTD	0E32	_	_	_	_	_	_	_	RD8	_	RD6	RD5		_	_	_	_	xxxx
LATD	0E34	_	_	_	_	_	_	_	LATD8	_	LATD6	LATD5		_	_	_	_	xxxx
ODCD	0E36	_	_	_	_	_	_	_	ODCD8	_	ODCD6	ODCD5		_	_	_	_	0000
CNEND	0E38	_	_	_	_	_	_	_	CNIED8	_	CNIED6	CNIED5		_	_	_	_	0000
CNPUD	0E3A	_	_	_	_	_	_	_	CNPUD8	_	CNPUD6	CNPUD5	_	_	_	_	_	0000
CNPDD	0E3C	_	_	_	_	_	_	_	CNPDD8	_	CNPDD6	CNPDD5		_	_	_	_	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE15	TRISE14	TRISE13	TRISE12	-	_	_	—	_	-	-	_	—	—	—	—	F000
PORTE	0E42	RE15	RE14	RE13	RE12	—	_	_	_	—	_		_	—	—	_	_	xxxx
LATE	0E44	LATE15	LATE14	LATE13	LATE12	—	_	_	_	_	_	_	_		—	_	_	xxxx
ODCE	0E46	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—		—	—	—	-	—	—	—	0000
CNENE	0E48	CNIEE15	CNIEE14	CNIEE13	CNIEE12	—	_	_	_	—	_		_	—	—	_	_	0000
CNPUE	0E4A	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	_	_	_	—	_	_	_	_	—	_	_	0000
CNPDE	0E4C	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	_	_	—	—	_	_	_	—	—	—	_	0000
ANSELE	0E4E	ANSE15	ANSE14	ANSE13	ANSE12	—	_	—	_	_	—	_	—	—	_	_		F000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	_	—	—	_	—	_	—	_	—	_	_	_	TRISF1	TRISF0	0003
PORTF	0E52	—	—	—	_	—	_	_	_	—	_	—	_	_	_	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	_	_	—	—	—	—	_	_	LATF1	LATF0	xxxx
ODCF	0E56	_	—	-	-	—	_	_	_	—		—		_	_	ODCF1	ODCF0	0000
CNENF	0E58		—		-	—	—	_	—	—	-	—		—	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	_	_	—	—	—	—	_	_	CNPUF1	CNPUF0	0000
CNPDF	0E5C	_	—	-	-	—	_	_	_	—		—		_	_	CNPDF1	CNPDF0	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)

- **Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
  - $\label{eq:constraint} \textbf{2:} \quad \text{This bit is cleared when the ROI bit is set and an interrupt occurs.}$
  - **3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	-	_	_	—	_	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				OCFAR<6:0>	>		
bit 7	-						bit 0
Legend:							

## REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0'

bit 6-0 OCFAR<6:0>: Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

> . 0000001 = Input tied to CMP1 0000000 = Input tied to Vss

# 16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of Tcy/2 (7.14 ns at Fcy = 70MHz)
- Independent Fault and current-limit inputs for six PWM outputs
- · Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

**Note:** In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNC01 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

# 16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are remappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

## 16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the highspeed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>), regardless of the state of FLT32.

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	WAKFIL		—		SEG2PH2	SEG2PH1	SEG2PH0
bit 15			•	•			bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15	Unimplemen	nted: Read as '	0'				
bit 14	WAKFIL: Sel	lect CAN Bus L	ine Filter for V	Vake-up bit			
	1 = Uses CAI	N bus line filter	for wake-up	a-un			
bit 13-11		ted. Pead as '		e-up			
bit 10-8	SEG2PH-2.0		u nent 2 hits				
bit 10-0	111 = 1 enoth	is 8 x To					
	•						
	•						
	•						
	000 = Length	n is 1 x Tq					
bit 7	SEG2PHTS:	Phase Segmer	nt 2 Time Sele	ect bit			
	1 = Freely pro	ogrammable					-4
hit C		1 OF SEGIPHX	Dits or informa	ation Processin	g Time (IPT), w	nicnever is gre	eater
DIL 6	J = Rus lino i	e of the CAN B	us Line bit a timos at tha	complo point			
	0 = Bus line i	s sampled once	e at the sampl	e point			
bit 5-3	SEG1PH<2:0	<b>)&gt;:</b> Phase Segr	nent 1 bits	•			
	111 = Length	n is 8 x Tq					
	•						
	•						
	•						
	000 = Length	n is 1 x Tq					
bit 2-0	PRSEG<2:0>	>: Propagation	Time Segmen	t bits			
	111 = Length	n is 8 x TQ					
	•						
	•						
	-						

# REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, reac	l as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15-13 bit 12-8	PTGCLK<2:0 111 = Reserv 110 = Reserv 101 = PTG m 010 = PTG m 011 = PTG m 010 = PTG m 001 = PTG m 000 = PTG m PTGDIV<4:02	<ul> <li>Select PTG</li> <li>red</li> <li>odule clock so</li> </ul>	Module Clock urce will be T3 urce will be T2 urce will be T1 urce will be T4 urce will be F6 urce will be F6 Clock Presca	Source bits CLK CLK CLK D SSC S ler (divider) bi	ts		
	11111 = Divic 11110 = Divic • • • • • • • • • • • • • • • • • • •	de-by-32 de-by-31 de-by-2 de-by-1					
bit 7-4	PTGPWD<3:0	<b>0&gt;:</b> PTG Trigge	er Output Pulse	e-Width bits			
	1111 = All trig 1110 = All trig • • • • • • • • • • • • • • • • • • •	gger outputs ar gger outputs ar gger outputs ar gger outputs ar	e 16 PTG cloc e 15 PTG cloc e 2 PTG clock e 1 PTG clock	k cycles wide k cycles wide cycles wide cycles wide			
bit 3	Unimplemen	ted: Read as '	0'				
bit 2-0	PTGWDT<2:0	0>: Select PTG	Watchdog Tir	mer Time-out	Count Value bits	3	
	111 = Watcho 110 = Watcho 101 = Watcho 100 = Watcho 011 = Watcho 010 = Watcho 001 = Watcho 000 = Watcho	dog Timer will t dog Timer is dis	ime-out after 5 ime-out after 2 ime-out after 1 ime-out after 3 ime-out after 3 ime-out after 1 ime-out after 8 sabled	512 PTG clock 256 PTG clock 28 PTG clock 54 PTG clocks 54 PTG clocks 6 PTG clocks 5 PTG clocks	S S S		

# REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

# REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
			PTGA	DJ<15:8>							
bit 15							bit 8				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
			PTGA	DJ<7:0>							
bit 7							bit 0				
Legend:											
R = Readable I	bit	W = Writable I	bit	U = Unimpler	nented bit, rea	d as '0'					
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown							

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

# REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0							
			PTGL0	<15:8>										
bit 15	bit 15 bit 8													

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<7:0>							
bit 7						bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

### bit 15-0 PTGL0<15:0>: PTG Literal 0 Register bits

This register holds the 16-bit value to be written to the AD1CHS0 register with the  ${\tt PTGCTRL}$  Step command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-5:	CMxMSKCON: COMPARATOR x MASK GATING				
	CONTROL REGISTER				

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS		OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15 bit							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0
Legend							
R = Readable	e hit	W = Writable	hit	II = Unimple	mented hit read	l as 'N'	
n = Value at		'1' = Rit is set		(0) = Bit is cluster	eared	x = Ritis unk	nown
	1010	1 - Dit 13 3C			carca		nown
bit 15	HLMS: Hiah	or Low-Level	/asking Select	bits			
	1 = The mask	king (blanking)	function will pre	event any asse	erted ('0') compa	rator signal fro	m propagating
	0 = The mas	king (blanking)	function will pre	event any asse	erted ('1') compa	rator signal fro	m propagating
bit 14	Unimpleme	nted: Read as	'0'				
bit 13	OCEN: OR (	Gate C Input Er	nable bit				
	1 = MCI is co	onnected to OF	t gate				
	0 = MCI is no	ot connected to	OR gate				
bit 12	OCNEN: OR Gate C Input Inverted Enable bit						
	1 = Inverted	MCI is connect	ed to OR gate	ate			
hit 11	OBEN: OR Gate B Input Enable bit						
Sit II	1 = MBI is connected to OR gate						
	0 = MBI is not connected to OR gate						
bit 10	OBNEN: OR Gate B Input Inverted Enable bit						
	1 = Inverted MBI is connected to OR gate						
	0 = Inverted	MBI is not con	nected to OR g	jate			
bit 9	OAEN: OR (	Gate A Input Er	nable bit				
	1 = MAI is co	onnected to OF	l gate				
hit 8	0 – MALIS HOLCOMMECTED TO OR Gate						
DILO	1 = Inverted MAI is connected to OR gate						
	0 = Inverted	MAI is not con	nected to OR g	jate			
bit 7	NAGS: AND	Gate Output In	nverted Enable	bit			
	1 = Inverted	ANDI is conne	cted to OR gat	e			
	0 = Inverted	ANDI is not co	nnected to OR	gate			
bit 6		Gate Output E	nable bit				
	0 = ANDI is r	not connected to O	o OR gate				
bit 5	ACEN: AND	Gate C Input E	Enable bit				
	1 = MCI is co	onnected to AN	D gate				
	0 = MCI is no	ot connected to	AND gate				
bit 4	ACNEN: AN	D Gate C Input	Inverted Enab	ole bit			
	1 = Inverted	MCI is connect	ed to AND gat	e			
	0 = Inverted	MCI is not con	nected to AND	gate			

Field	Description					
Wm,Wn	Dividend, Divisor working register pair (direct addressing)					
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}					
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}					
Wn	One of 16 working registers ∈ {W0W15}					
Wnd	One of 16 destination working registers ∈ {W0W15}					
Wns	One of 16 source working registers ∈ {W0W15}					
WREG	W0 (working register used in file register instructions)					
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }					
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }					
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}					
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}					
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}					
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}					

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS (	(CONTINUED)

# 29.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM<sup>™</sup> and dsPICDEM<sup>™</sup> demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ<sup>®</sup> security ICs, CAN, IrDA<sup>®</sup>, PowerSmart battery management, SEEVAL<sup>®</sup> evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

# 29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent<sup>®</sup> and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika<sup>®</sup>



### FIGURE 30-20: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated) <sup>(1)</sup> Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic	Min.	Тур. <sup>(2)</sup>	Max.	Units	Conditions
Op Am	p DC Chara	cteristics					
CM40	VCMR	Common-Mode Input Voltage Range	AVss	_	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio <sup>(3)</sup>	—	40	—	db	Vсм = AVdd/2
CM42	VOFFSET	Op Amp Offset Voltage <sup>(3)</sup>	—	±5	—	mV	
CM43	Vgain	Open-Loop Voltage Gain <sup>(3)</sup>	—	90		db	
CM44	los	Input Offset Current	—	_	_		See pad leakage currents in Table 30-11
CM45	Ів	Input Bias Current	—	—	_	_	See pad leakage currents in Table 30-11
CM46	Ιουτ	Output Current	—	_	420	μA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	-	_	kΩ	
CM49a	VOADC	Output Voltage Measured at OAx Using ADC <sup>(3,4)</sup>	AVss + 0.077 AVss + 0.037 AVss + 0.018		AVDD – 0.077 AVDD – 0.037 AVDD – 0.018	V V V	Ιουτ = 420 μΑ Ιουτ = 200 μΑ Ιουτ = 100 μΑ
CM49b	Vout	Output Voltage Measured at OAxOUT Pin <sup>(3,4,5)</sup>	AVss + 0.210 AVss + 0.100 AVss + 0.050		AVDD - 0.210 AVDD - 0.100 AVDD - 0.050	V V V	Ιουτ = 420 μΑ Ιουτ = 200 μΑ Ιουτ = 100 μΑ
CM51	RINT1 <sup>(6)</sup>	Internal Resistance 1 (Configuration A and B) <sup>(3,4,5)</sup>	198	264	317	Ω	Min = -40°C Typ = +25°C Max = +125°C

### TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS (CONTINUED)

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- **3:** Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.

Section Name	Update Description				
Section 30.0 "Electrical	These SPI2 Timing Requirements were updated:				
Characteristics" (Continued)	<ul> <li>Maximum value for Parameter SP10 and the minimum clock period value for SCKx in Note 3 (see Table 30-36, Table 30-37, and Table 30-38)</li> </ul>				
	Maximum value for Parameter SP70 and the minimum clock period value for SCKx in Note 3 (see Table 30-40 and Table 30-42)				
	The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-43)				
	These SPI1 Timing Requirements were updated:				
	Maximum value for Parameters SP10 and the minimum clock period value for SCKx in Note 3 (see Table 30-44, Table 30-45, and Table 30-46)				
	<ul> <li>Maximum value for Parameters SP70 and the minimum clock period value for SCKx in Note 3 (see Table 30-47 through Table 30-50)</li> </ul>				
	<ul> <li>Minimum value for Parameters SP40 and SP41 see Table 30-44 through Table 30-50)</li> </ul>				
	Updated all Typical values for the CTMU Current Source Specifications (see Table 30-55).				
	Updated Note1, the Maximum value for Parameter AD06, the Minimum value for AD07, and the Typical values for AD09 in the ADC Module Specifications (see Table 30-56).				
	Added Note 1 to the ADC Module Specifications (12-bit Mode) (see Table 30-57).				
	Added Note 1 to the ADC Module Specifications (10-bit Mode) (see Table 30-58).				
	Updated the Minimum and Maximum values for Parameter AD21b in the 10-bit Mode ADC Module Specifications (see Table 30-58).				
	Updated Note 2 in the ADC Conversion (12-bit Mode) Timing Requirements (see Table 30-59).				
	Updated Note 1 in the ADC Conversion (10-bit Mode) Timing Requirements (see Table 30-60).				

### TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)