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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
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3.7 CPU Control Registers

R/W-0) R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0			
0A ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC			
bit 15							bit 8			
R/W-0 ⁽²	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0			
IPL2	IPL1	IPL0	RA	N	OV	Z	С			
bit 7							bit 0			
Legend:		C = Clearable	bit							
R = Reada	able bit	W = Writable	able bit U = Unimplemented bit, read as '0'							
-n = Value	e at POR	'1'= Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown			
bit 15	OA: Accumu	lator A Overflow	v Status bit ⁽¹⁾							
	1 = Accumula	ator A has over	flowed							
	0 = Accumula	ator A has not c	verflowed							
bit 14	OB: Accumulator B Overflow Status bit ⁽¹⁾									
	1 = Accumulator B has overflowed									
hit 13		0 = Accumulator B flas not overnowed								
DIL 15	$1 = \Delta c cumula$	ator A is saturat	ed or has her	n saturated at	some time					
	0 = Accumula	ator A is not sat	urated		Some time					
bit 12	SB: Accumu	lator B Saturatio	on 'Sticky' Sta	tus bit ^(1,4)						
	1 = Accumula	ator B is satura	ed or has bee	en saturated at	some time					
	0 = Accumula	ator B is not sat	urated							
bit 11	OAB: OA (OB Combined A	ccumulator O	verflow Status	bit ⁽¹⁾					
	1 = Accumula	ators A or B have	ve overflowed							
	0 = Neither A	Accumulators A	or B have ove	erflowed	(1)					
bit 10	SAB: SA S	B Combined A	cumulator 'Si	icky Status bit		1				
	1 = Accumula 0 = Neither A	ators A or B are	or B are satur	nave been sat	urated at some	time				
hit 9		Active hit(1)		alou						
bit 0	1 = DO loop is	s in progress								
	0 = DO loop is	s not in progres	S							
bit 8	DC: MCU AL	U Half Carry/Bo	orrow bit							
	1 = A carry-o	out from the 4th	low-order bit (for byte-sized o	data) or 8th low-	order bit (for wo	ord-sized data)			
	of the re	sult occurred								
	0 = No carry	-out from the 4	th low-order t	bit (for byte-siz	ed data) or 8th	low-order bit (1	for word-sized			
	uala) U									
Note 1:	This bit is availabl	e on dsPIC33E	PXXXMC20X	/50X and dsPl	C33EPXXXGP	50X devices on	ly.			
2:	The IPL<2:0> bits	are concatenat	ed with the IF	PL<3> bit (COR	RCON<3>) to fo	rm the CPU Inte	errupt Priority			
	Level. The value I IPL< $3 > = 1$.	n parentheses i	naicates the I	PL, IT IPL<3> =	= ⊥. User interru	ipts are disable	a wnen			

REGISTER 3-1: SR: CPU STATUS REGISTER

- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- **4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2	SFA: Stack Frame Active Status bit
	1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and
	DSWPAG values
	0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space
hit 1	PND: Dounding Mode Select hit(1)

- bit 1 **RND:** Rounding Mode Select bit⁽¹⁾
 - 1 = Biased (conventional) rounding is enabled
 - 0 = Unbiased (convergent) rounding is enabled

bit 0 IF: Integer or Fractional Multiplier Mode Select bit⁽¹⁾ 1 = Integer mode is enabled for DSP multiply 0 = Fractional mode is enabled for DSP multiply

- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
 - **2:** This bit is always read as '0'.
 - 3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.



FIGURE 4-7: DATA MEMORY MAP FOR dsPIC33EP32MC20X/50X AND dsPIC33EP32GP50X DEVICES

TABLE 4-17: I2C1 AND I2C2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	_	—	_	_	– – I2C1 Receive Register								0000	
I2C1TRN	0202	_	_	_	_	_	_	_	I2C1 Transmit Register								00FF	
I2C1BRG	0204	_	_	_	_	_	_	_	Baud Rate Generator								0000	
I2C1CON	0206	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	_	—	_	—		I2C1 Address Register								0000		
I2C1MSK	020C	—	_	—	_	—						I2C1 Ad	dress Mask					0000
I2C2RCV	0210	_	_	_	_	_	_	_	_				I2C2 Recei	ve Register				0000
I2C2TRN	0212	_	_		—	—		_	—				I2C2 Trans	mit Register				00FF
I2C2BRG	0214	—	_	—	_	—		—				Bau	d Rate Gen	erator				0000
I2C2CON	0216	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2STAT	0218	ACKSTAT	TRSTAT		—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
I2C2ADD	021A	_		_	_	_	_					I2C2 Addr	ess Registe	r				0000
I2C2MSK	021C	_		_	_	_	_					I2C2 Ad	dress Mask					0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<	<1:0>	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT URXISEL<1:0> ADDEN RIDLE PERR FERR OER				OERR	URXDA	0110			
U1TXREG	0224	_	_	—	_	_	_	_	- UART1 Transmit Register xx								xxxx	
U1RXREG	0226	_	_	—	_	_	_	_	UART1 Receive Register							0000		
U1BRG	0228							Baud	Rate Gen	erator Pre	scaler							0000
U2MODE	0230	UARTEN	_	USIDL	IREN	RTSMD	_	UEN<	<1:0>	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXI	SEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	_	_	—	_	_	_	_				UART	2 Transmit F	Register				xxxx
U2RXREG	0236	_	_	—	_	_	_	_				UART	2 Receive F	Register				0000
U2BRG	Baud Rate Generator Prescaler 000									0000								
			- ·															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

FIGURE 4-18: ARBITER ARCHITECTURE

that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62:	DATA MEMORY BUS
	ARBITER PRIORITY

Briority	MSTRPR<15:0> Bit Setting ⁽¹⁾						
Phoney	0x0000	0x0020					
M0 (highest)	CPU	DMA					
M1	Reserved	CPU					
M2	Reserved	Reserved					
M3	DMA	Reserved					
M4 (lowest)	ICD	ICD					

Note 1: All other values of MSTRPR<15:0> are reserved.



Internut Course	Vector	IRQ		Interrupt Bit Location			
Interrupt Source	#	#	IVI Address	Flag	Enable	Priority	
	Highe	est Natura	al Order Priority				
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>	
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>	
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>	
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>	
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>	
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>	
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>	
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>	
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>	
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>	
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>	
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>	
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>	
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>	
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>	
Reserved	23	15	0x000032	_	_	_	
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>	
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>	
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>	
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>	
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>	
Reserved	29-31	21-23	0x00003E-0x000042	_	_	_	
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>	
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>	
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>	
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>	
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>	
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>	
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>	
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>	
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>	
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>	
C1RX – CAN1 RX Data Ready ⁽¹⁾	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>	
C1 – CAN1 Event ⁽¹⁾	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>	
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>	
IC3 – Input Capture 3	3 – Input Capture 3 45 37 0x00005E		0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>	
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>	
Reserved	47-56	39-48	0x000062-0x000074	—	—	_	
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>	
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>	
Reserved	59-64	51-56	0x00007A-0x000084				
PSEM – PWM Special Event Match ⁽²⁾	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>	

TABLE 7-1: INTERRUPT VECTOR DETAILS

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0		
CHEN	SIZE	DIR	HALF	NULLW	_	—	—		
bit 15							bit 8		
U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0		
		AMODE1	AMODE0			MODE1	MODE0		
bit 7							bit 0		
Legend:			,			(0)			
R = Readable	bit	W = Writable	bit		mented bit, read	as '0'			
-n = Value at F	POR	'1' = Bit is set		0^{\prime} = Bit is cle	eared	x = Bit is unkn	IOWN		
bit 15		Channel Enabl	o hit						
bit 15	1 = Channel	is enabled							
	0 = Channel is disabled								
bit 14 SIZE: DMA Data Transfer Size bit									
	1 = Byte								
	0 = Word								
bit 13	DIR: DMA Transfer Direction bit (source/destination bus select)								
	1 = Reads from 0 = Reads from 1	om RAM addre	ddress. writes to p	s to RAM addr	ess ess				
bit 12	HALF: DMA	Block Transfer	Interrupt Sele	ct bit					
	1 = Initiates i	nterrupt when I	nalf of the dat	a has been mo	oved				
	0 = Initiates i	nterrupt when a	all of the data	has been mov	ved				
bit 11	NULLW: Null	Data Periphera	al Write Mode	Select bit					
	1 = Null data	write to periph	eral in additio	n to RAM write	e (DIR bit must a	also be clear)			
bit 10-6	Unimplemen	ted: Read as '	ר'						
bit 5-4	AMODE<1:0	: DMA Channe	el Addressina	Mode Select	bits				
	11 = Reserve	ed							
	10 = Peripher	ral Indirect Add	ressing mode						
	01 = Register	Indirect withou	ut Post-Increm	nent mode					
hit 3 2		tod: Pood as '	ost-incremen	tmode					
bit 1_0		DMA Channel	Operating Mc	nda Salact hits					
bit 1-0	11 = One-Sh	ot. Pina-Pona r	nodes are en	abled (one blo	ck transfer from	/to each DMA b	ouffer)		
	10 = Continue	ous, Ping-Pong	modes are e	nabled					
	01 = One-Sho	ot, Ping-Pong r	nodes are dis	abled					
	00 = Continue	ous, Ping-Pong	modes are d	ISADIEO					

REGISTER 8-1: DMAXCON: DMA CHANNEL X CONTROL REGISTER

11.4.4.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-18 through Register 11-27). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



11.4.4.3 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-toone and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPxR<5:0>	Output Name
Default PORT	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
SS2	001010	RPn tied to SPI2 Slave Select
C1TX ⁽²⁾	001110	RPn tied to CAN1 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
SYNCO1 ⁽¹⁾	101101	RPn tied to PWM Primary Time Base Sync Output
QEI1CCMP ⁽¹⁾	101111	RPn tied to QEI 1 Counter Comparator Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4

Note 1: This function is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This function is available in dsPIC33EPXXXGP/MC50X devices only.

NOTES:



FIGURE 18-1: SPIX MODULE BLOCK DIAGRAM

NOTES:

24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

24.2.1 KEY RESOURCES

- "Peripheral Trigger Generator" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

- bit 5 Unimplemented: Read as '0'
- bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)⁽¹⁾
 - 1 = VIN+ input connects to internal CVREFIN voltage
 - 0 = VIN+ input connects to C4IN1+ pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Channel Select bits⁽¹⁾
 - 11 = VIN- input of comparator connects to OA3/AN6
 - 10 = VIN- input of comparator connects to OA2/AN0
 - 01 = VIN- input of comparator connects to OA1/AN3
 - 00 = VIN- input of comparator connects to C4IN1-
- Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline
 assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- · Command-line interface
- · Rich directive set
- Flexible macro language
- · MPLAB X IDE compatibility

29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming[™] (ICSP[™]).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS



TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{ll} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions	
OC10	TccF	OCx Output Fall Time	—			ns	See Parameter DO32	
OC11	TccR	OCx Output Rise Time	—	— — — ns See Parameter DO31				

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS



TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
OC15	Tfd	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns	
OC20	TFLT	Fault Input Pulse Width	Tcy + 20	_	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.



FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

NOTES:



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